Model 9615
ICB Amplifier

User's Manual

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ISO 9001
SYSTEM
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Table of Contents

List of Figures

1. Introduction

The Model 9615 represents the latest in a programmable spectroscopy amplifier design and includes all the features associated with a research grade signal processor. It joins the ICB line of programmable front end electronics as a premier amplifier featuring: differential inputs for common mode noise rejection, wide gain range, choice of semi-Gaussian or semi-Triangular pulse shaping to meet most detector applications and requirements, a flexible Baseline Restorer and an integral Pile Up Rejector and Live Time Corrector.

The 9615 features Automatic Fine Tuning (AFT), which combined with computer control, makes the unit easy to set up and use. Critical performance adjustments are automatically optimized, eliminating the subjectiveness and guess work normally associated with manual fine tuning. The results are consistent and repeatable, and nearly operator independent.

With the 9615 there is no need for an oscilloscope to optimize pole/zero (P/Z) matching. The operator simply starts the optimization process from the computer. The Busy LED lights and the P/Z matching circuit begins converging on the optimal setting required for good high count rate resolution, peak stability and overload recovery. When the process is complete, the Busy LED turns off and the computer stores the latest P/Z setting.

The Busy LED will blink and the computer will be signaled if convergence is not achieved within two minutes. When power is turned ON, the LED will blink until the computer loads the P/Z setting or initiates another convergence.

The PUR threshold is automatically set just above the system noise level, insuring PUR efficiency and minimal spectral distortion due to pile up at high count rates. The restoration rate and threshold are automatically fine tuned for all shapings, gain and count rate conditions.

The 9615 employs three active complex-pole filters for improved pulse symmetry, reduced pulse dwell time and high throughput. For additional flexibility, semi-Gaussian or semi-Triangular pulse shaping are selectable.

Triangular shaping offers superior energy resolution due to its inherently longer rise time, better signal to noise ratio and reduced sensitivity to detector rise time variations. The amplifier offers six switch-selectable shaping time constants, which effectively doubles to 12 when the choice of Gaussian and Triangular are both considered, allowing optimum matching for most detector and count rate requirements. This switch is located on the rear panel to avoid any casual operator intervention. Although a manual adjustment, the setting is read by the computer to insure proper operation.

The gated baseline restorer with automatic rate and threshold assures the best possible low and high count rate resolution performance. The flexibility of the baseline restorer is further enhanced with programmed Asymmetrical and Symmetrical restorer modes. The Asymmetrical mode virtually eliminates charge accumulation and correlated noise on the restorer holding capacitor and is especially suited for use with high resolution detector systems. The Symmetrical mode allows performance optimization for detector systems which exhibit baseline discontinuities resulting from excessive noise, microphonics, high voltage effects, and preamplifier secondary time constants.

The 9615 has a differential input stage which can be used to suppress noise caused by ground loops, laboratory environment EMI and the resultant noise pick-up on cables and so forth. It is especially useful for applications which require long cables between the detector/preamplifier and amplifier. As with most other Canberra amplifiers, cable transformers are included in the 9615 to suppress high frequency noise normally associated with personal computer and MCA raster-type displays. A Common Mode Balance (CMB) control is conveniently located on the front panel allowing common mode rejection optimization for the specific application.

The Live Time Corrector and Pile Up Rejector circuit allows quantitative gamma analysis nearly independent of system count rate. Special circuitry interrogates for pile up and permits the ADC to convert only those detector signals resulting from single energy events. To compensate for rejected pulses and pulse processing times, the 9615 generates a system dead time which extends the collection time by the appropriate amount.

The front panel Accept/Reject LED indicates pile up rejector status. As the count rate and the number of pulses rejected due to pile-up increases, the LED changes color.

The 9615 accepts programming information over an 8-bit wide Canberra bus standard called the Instrument Control Bus (ICB). ICB NIMs connect to this bus via a master module such as the Model 556 Acquisition Interface Module (AIM) as part of a hierarchy of networked acquisition and control managed by a Genie Family computing platform.

Adjustments are made through the Graphics User Interface of the Genie software environments. Equivalent batch procedure commands are also available in the environments. All ICB NIM parameters are stored in the single data file structure of the Genie Family, allowing verification of correct set up from one experiment to the next.

All ICB NIMs feature a characteristic bi-color Ready LED to indicate operational status.

2. Controls and Connectors

2.1 Front Panel

This is a brief description of the front panel connectors and indictors. For more detailed information, refer to Appendix A, Specifications.

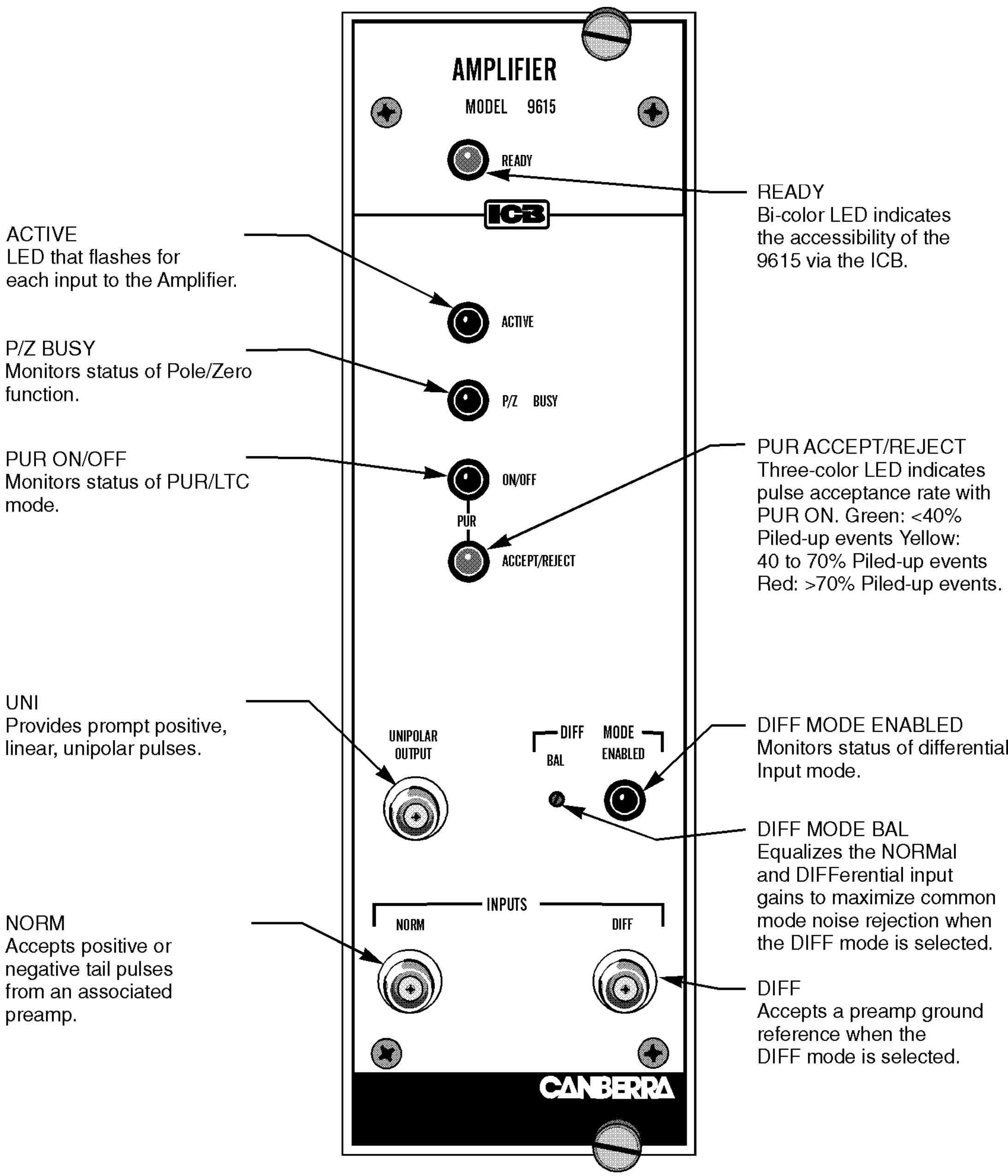

Figure 2.1 Front Panel Controls

2.2 Rear Panel

This is a brief description of the rear panel controls and connectors. For more detailed information, refer to *Appendix A, Specifications*.

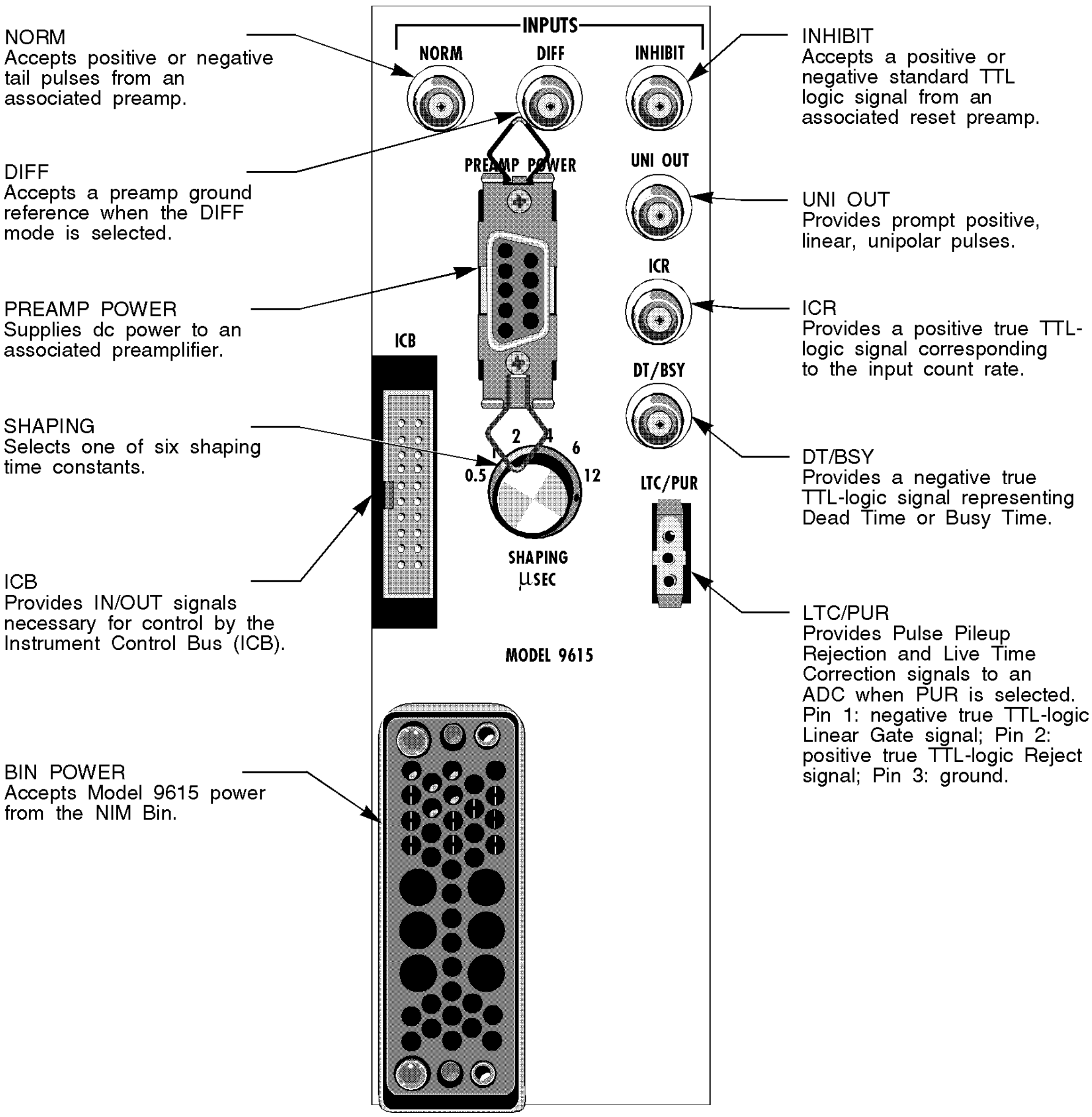

Figure 2.2 Rear Panel Controls

2.3 Internal Controls

These diagrams locate the unit's internal controls. For more information, refer to Appendix B.

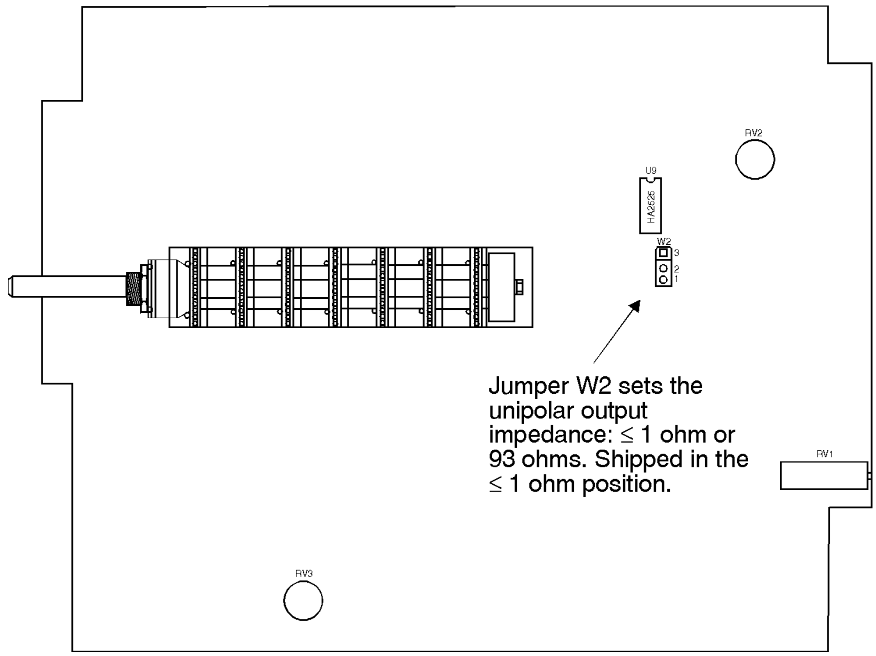

Figure 2.3 Internal Controls – Board 1

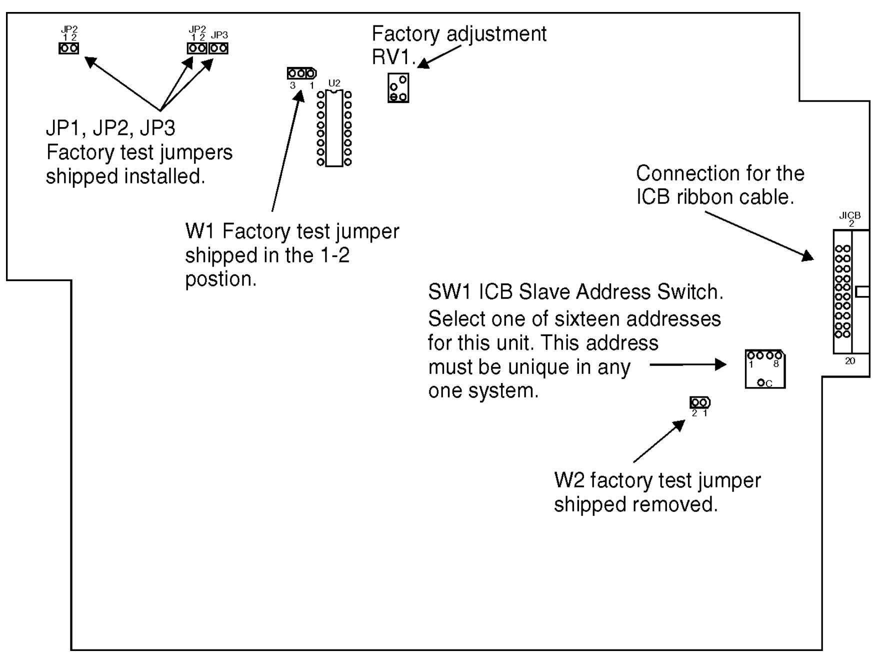

Figure 2.4 Internal Controls – Board 2

3. Amplifier Operation

This section outlines the operation of the Model 9615 Spectroscopy Amplifier. Following these procedures will make you familiar enough with the instrument to be able to use it effectively in any situation.

3.1 Installation

Refer to the Model 9600 AIM/ICB System Setup Manual for details on ICB-related requirements.

The Canberra Model 2100 Bin and Power Supply, or other bin and power supply system providing +6 volts and conforming to the mechanical and electrical standards set by DOE/ER-0457T, will accommodate the Model 9615. The 9615's right side-cover acts as a guide for insertion of the module. The module is secured in place by turning the two front panel captive screws clockwise until finger tight. It is recommended that the NIM bin power switch be *off* whenever the module is installed or removed.

The Model 9615 can be operated where the ambient air temperature is between 0 °C and +50 °C (+120 °F maximum). Perforations in the top and bottom sides permit cooling air to circulate through the module. When relay rack mounted along with other heat generating equipment, adequate clearance should be provided to allow for sufficient air flow through both the perforated top and bottom covers of the NIM bin.

3.2 Spectroscopy System Setup

Follow these steps to set up an ICB gamma spectroscopy system.

a. Preamp power is provided through a connector located on the rear panel of the amplifier. Connect the Preamp Power and NORM INPUT to your detector. Adjust the High voltage Bias voltage to the setting specified for the detector. Allow the total system to warm up and stabilize.

b. Use your software (Genie-PC for instance), to set the 9615's programmable controls:

   Coarse Gain X50
   Fine Gain 1.6X
   BLR Mode . . . . ASYM
   PUR . . . . OFF
   Preamp type . . . . TRP or RC, as required
   Shaping Mode . . . . Gaussian
   Input Mode . . . . Normal
   Input Polarity . . . . Positive or Negative, as required.*
   LTC Mode . . . . Normal
   Inhibit Polarity . . . . Positive or Negative, as required.

   *Most Canberra Preamplifiers have Positive outputs.

c. This will give approximately a 9 V output when using a preamp gain of 100 mV/MeV and a ^{60}Co radioactive source.

d. Connect the Amplifier's UNIpolar output to the ADC's INPUT. The ADC must be direct coupled for linear input signals to fully exploit the count rate capabilities of the Model 9615. All Canberra ADCs are dc coupled.

e. Set the 9615's rear panel SHAPING control to 4 µs.

3.3 Preamp Fall Time Matching

Pole/zero (P/Z) compensation is extremely critical when using resistive feedback preamplifiers and must be readjusted whenever the amplifier's shaping is changed. When a TRP type preamp is used, P/Z compensation is not required.

3.3.1 Automatic Pole/Zero Matching

The pole/zero adjustment is extremely important in obtaining best system performance. After selecting the desired Shaping Time and Gain through the software, the adjustment is made by the operator with a moderate source at the detector. The automatic adjustment requires that at least 60 counts per second be processed by the amplifer in an output window of 7 to 10 volts.

When the amplifer is first turned ON, the P/Z BUSY LED will BLINK until the P/Z cycle is started or the software reloads the previous setting.

Initiating a P/Z cycle causes the LED to be lit continuously. If convergence is achieved within two minutes, the LED will turn OFF. If proper matching cannot be achieved, the LED will BLINK and an error message will be posted by the computer. The failure may be because:

- The count rate is too low or too high.
- The signal amplitude is not within the window.
- The input tail pulse fall time constant is not within the matching range of 40 µs to infinity.
- Excessive noise or abnormal variations of the output signals baseline. This could be caused by microphonics, high voltage arcing or a damaged detector.

If the P/Z cycle is started again, it will use the result of the last cycle as a starting point. In this way with a low count rate you can eventually achieve a successful convergence.

The P/Z value is read by the computer and stored. If power to the module is interrupted, the computer can reload its stored value.

The precision of the P/Z operation can be verified by observing the trailing edge of the unipolar output signal on an oscilloscope. Set the oscilloscope vertical range to an appropriate sensitivity. A Model LB1502 Clamp Box can be used to prevent scope overload.

Auto P/Z compensation **must** be reinitialized after the following events:

- Amplifier SHAPING TIME is changed.
- The Model 9615 is connected to a different detector/preamp.

4. Operation With ADC and MCA

For a detailed discussion of tradeoffs regarding Base Line Restorer settings, Shaping Selection and Shaping Mode, please refer to Appendix C. Figure 4.1 shows a typical gamma spectroscopy system.

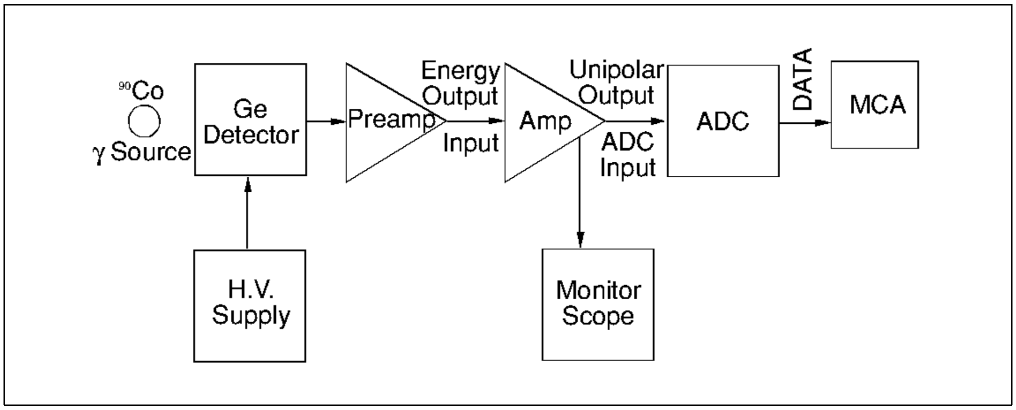

Figure 4.1 A Typical Gamma Spectroscopy System

4.1 ADC Setup

Please refer to the ADC Operator's Manual for specific ADC operating instructions.

Set the ADC GAIN and RANGE equal to the MCA memory group size. For instance, set the GAIN and RANGE to 4096 for an MCA with 4096 channel memory size.

Set the ADC controls to:

LLD . . . . 0.02 V
ULD . . . . 10.5 V
Digital Offset 0

4.2 Spectroscopy Operation

Please refer to the MCA Operator's Manual for specific operating instructions for your MCA.

Start MCA COLLECT with the ^{60}Co radioactive source previously placed near the detector. A spectrum should begin to appear on the MCA's display.

Adjust the Amplifier's GAIN so that the spectrum is positioned conveniently on the display.

Use the Amplifier's Super Fine Gain (SFG) when matching gains of several detectors, or when establishing a specific gain (energy per channel). This control provides more resolution than the Fine Gain control.

5. PUR/LTC Operation

The Model 9615 and associated ADC work together as an integral system to perform pileup rejection and live time correction. The associated ADC can be an MCA's internal ADC or any current Canberra NIM.

To compensate for dead times associated with rejected pulses and amplifier processing times, the Model 9615 generates a dead time (DT) signal which extends the collection time by the appropriate amount.

The front panel Accept/Reject LED indicates pile up rejector status. For low count rate and low losses due to pile up, the multicolor LED flashes green. As the count rate and the number of pulses rejected due to pile up increases (40-70%), the LED turns proportionately yellow. When pile up losses become significant (>70%), the LED turns red.

Note that the RED indicator is not intended to be interpreted as a safety indicator.

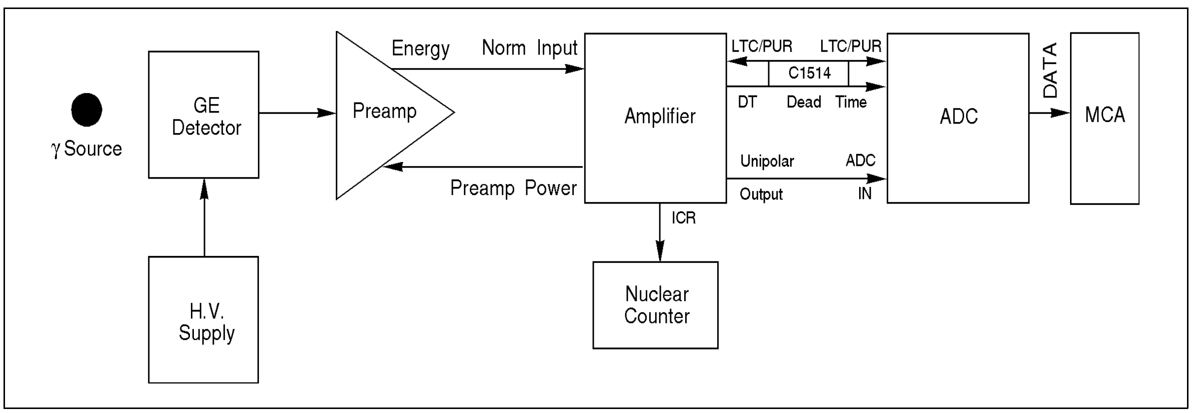

Figure 5.1 A Gamma Spectroscopy System with PUR/LTC

5.1 System Setup

With a nuclear counter connected to the 9615's rear panel ICR output and with the PUR set ON, the average total input count rate can be monitored. Connect the system as shown in Figure 5.1.

a. Set the Model 9615 as follows:

Input Mode	Normal
Shaping Time	4 µs
Shaping Mode	Gaussian
PUR On/Off	ON
BLR Mode	ASYM
LTC Mode	Normal

b. Set the ADC's controls as follows:

Conversion Gain 8K
Range . . . . Set as required by MCA
Offset 000

c. Set the MCA to acquire and adjust the amplifier's gain to allow collection of the ^{57}Co peaks at 90% of the amplifier's range.

d. If the amplifier has not been pole/zeroed (see Section 3), start a P/Z compensation sequence by selecting ADJUST then amplifier from the MCA menu.

5.2 Pileup Rejection With a Live Source

To set up the system for performing PUR with a live source, follow these steps:

a. Bring a source, such as ^{57}Co, near the detector and adjust it for an input count rate of approximately 50 kcps.

b. Reduce the COARSE GAIN to x500 and adjust the FINE GAIN to allow collection of the primary and sum peaks.

c. Set the MCA's preset to 60 seconds of Live Time.

d. Clear Data, and accumulate a spectrum.

e. Save the spectrum.

f. Now accumulate a spectrum with the Amplifier's PUR function OFF. Compare the two spectra. The two spectra should look like Figure 5.2.

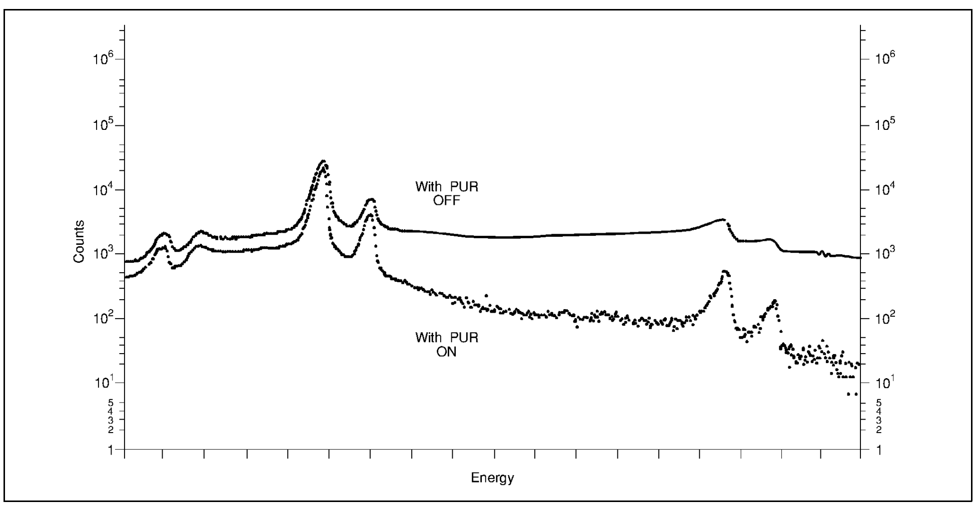

Figure 5.2 ^{60}Co at 50 kcps, 4 µs Shaping

Note the reducton in amplitude of both the sum peaks and background. Also note the improved resolution of the sum peaks. The background reduction and improved resolution are directly indicative of the Pileup Rejector's capabilities, since only sum peak pulses which are indeed 100% in coincidence should be processed.

5.3 Live Time Correction With a Live Source

THESE INSTRUCTIONS ARE FOR GENERAL USE...

a. Set up the equipment as indicated in step 5.1.

b. Set the 9615's GAIN to x100.

c. Enable the Amplifier's PUR function.

d. Position a source, such as ^{65}Zn, near the Ge detector and adjust for an incoming count rate of 1 kcps. Once in place, the source should not be moved or altered in any way for the remainder of the experiment.

e. Adjust the 9615's gain to position the ^{65}Zn peak at 90% of the active MCA memory.

f. Collect a spectrum for 500 Live seconds. Record the ^{65}Zn peak's net area.

g. To the 1 kcps of ^{65}Zn, add approximately 5 kcps of ^{137}Cs to make the total incoming count rate 6 kcps.

h. Collect a new spectrum for 500 Live seconds, and record the ^{65}Zn peak's net area.

i. Repeat steps *g* and *h* in 5 kcps increments up to 30 kcps.

j. Compare the ^{65}Zn peak net area in steps *g* through *i* to that in step *f* and compute the percentage change.

k. Set the PUR to OFF. Repeat steps *d* through *j*.

Since the detector-source (^{65}Zn) geometry was maintained and the preset Live Collection time was held constant, the ^{65}Zn net area can be used as a standard when comparing the effect of background (^{137}Cs) count rate.

NOTE Each time the background count (^{137}Cs) is changed, allow the detector to stabilize a few minutes before collecting the spectrum.

With the PUR OFF, large changes will be observed in the ^{65}Zn net peak area as a function of count rate.

With the pileup rejector set ON, changes in the ^{65}Zn peak net area will be significantly reduced. The Live Time corrector extends the collection time compensating for amplifier processing time and ^{65}Zn events rejected due to pileup.

Performance may vary and is dependent on factors such as ADC type, calibration, spectrum energy distribution and detector characteristics such as geometry, size, and ballistic deficit.

5.4 Operation with Model 599 LFC.

Refer to the Model 599's Operator's Manual for proper connection and operation. The amplifier's programmable LTC mode must be set to LFC.

6. Circuit Description

The 9615 is a signal processor which amplifies and shapes signals from conventional resistive feedback (RC) or reset type preamplifiers.

The amplifier includes a differential input stage for common mode noise suppression, followed by a differentiator, three low noise gain amplifier stages, three complex pole active filter stages (optimized for improved pulse symmetry), a gated active baseline restorer and a unipolar output amplifier providing semi-gaussian or semi-triangular output pulse shaping.

Also included is a high performance pile up rejector/live time corrector and associated fast signal recognition circuits.

AFT (automatic fine tuning) performs critical performance adjustments which automatically optimizes pole/zero compensation, baseline restoration rate and noise discriminator thresholds for the baseline restorer and pile up rejector.

The following is a description of the circuity used in the model 9615. Throughout the circuit description please refer to the specific schematic page number when noted.

6.1 Input Mode Switch

The relays K6, K7 and K8 (schematic sheet 1) selects Normal or Differential operation and input signal polarity. With NORM mode selected, the preamplifier signal is accepted by the front or rear panel NORM BNC connectors; the DIFF BNC connectors are not functional in this mode. The signal passes through the cable transformer assemblies for high frequency noise suppression. With Differential mode selected the front and rear panel DIFF input BNCs are activated for acceptance of a ground reference signal for common mode noise suppression. The differential reference signal also passes through a cable transformer for additional high frequency noise suppression. The relays routes the input signals to the appropriate input of the differential input amplifier.

6.2 Differential Input Amplifier

This amplifier (schematic sheet 1) is a discrete low noise differential amplifier comprised of transistors Q24 through Q31. This amplifier gain is a selected by coarse gain relay K5 and is X1 for a coarse gain of 5 and X2 for coarse gains of 10 and higher. With NORM input mode selected the non-driven input is terminated into 93 ohms. When used in the differential mode, the amplifier uses both the NORM and DIFF inputs and provides common mode rejection to suppress noise caused by ground loops, laboratory EMI and noise pick up induced on the input signal coax cables. The negative output signal provided by this stage drives the Auto Pole/Zero circuit and the first differentiator.

6.3 Differentiator and Gain Stages (Schematic Sheets 2 and 3)

The signal provided by the differential amplifier is differentiated by C80 through C88 and resistor R18. With RC Preamp selected, pole/zero compensation is provided by the automatic pole/zero circuit that is consistent, repeatable and nearly operator independent. With a TRP PREAMP, pole/zero compensation is automatically set to infinity as required by reset type preamps.

The differentiated and pole/zero compensated signal is next amplified by gain AMPs U2, U3 and U4 or gain AMPs U2 and U4 depending on the COARSE GAIN setting. FINE GAIN is performed in gain AMP U2. The gain adjustment range of gain AMPs U2 through U4 is continuously adjustable from X1.65 to X750. Limiters in the feedback path of each gain amplifier eliminate op-amp saturation maintaining good overload recovery. The output signal of gain AMP U4 is normally negative and drives the PUR/LTC FAST DISCriminator circuits and active filter integrators U16, U6 and U8.

6.4 Gain Stage Stabilizer (Sheet 2)

A dc stabilizer is provided around the gain stage amplifiers to maintain the dc output at gain AMP U4 near zero volts over a wide range of temperatures and count rates. Transconductance amplifier U7 monitors the output with respect to zero volts and generates a correction voltage that is summed at the input of gain AMP U2. Op-amp U5 is a high input impedance buffer. The stabilization loop time constant is determined by the transconductance current programing resistors R67 and R68 and capacitors C40 and C41 resulting in a time constant sufficiently long so as not to have an effect on the overall amplifier shaping transfer function.

6.5 Active Filters (Sheet 4)

Three active filter stages, ICs U16, U6 and U8, produce complex pole pairs providing a near gaussian pulse shape and a sharp cutoff frequency characteristic for optimal signal to noise ratio. The filter time constant is selected by the shaping switch SD1 and associated resistors and capacitors. The output signal from the third integrator is normally negative and drives the unipolar output amplifier.

6.6 Unipolar Output (Sheet 5)

The signal provided by the third complex pole integrator drives the unipolar output amplifier and associated driver, IC U9 and transistors Q4, Q5 and Q6. The unipolar output amplifier includes a single pole filter provided by feedback resistor R119 and capacitors C32 through C37; the time constant is selected by the shaping switch. For Gaussian shaping, the unipolar output provides a semi-Gaussian pulse shape. However, if Triangular shaping is selected, relays K3 and K4 are activated which allows the signals from the complex pole integrators to be summed at the input of the unipolar output amplifier, in the correct proportions to produce a semi-triangular output signal. Super Fine Gain adjustment is made using D/A Converter U25.

6.7 Baseline Restorer (Sheet 5)

The baseline restorer maintains the unipolar output signal baseline at ground reference, with precision, over a wide range of count rates. Transconductance amplifier U13 monitors the unipolar output signal and develops a correction voltage, having the correct amplitude and polarity, which is summed at the input of the unipolar output amplifier to reference the unipolar output signal baseline at zero volts. The baseline restorer is gated and operates only in the absence of or in between output pulses providing superior baseline control over a very wide range of count rates.

Restorer symmetry is selectable by the BLRSYM* signal. For the symmetrical restorer mode, positive and negative restoration slew rates are equal. When the asymmetrical is selected, the negative restorer slew rate is reduced substantially providing a softer restorer response for positive output signals.

6.8 Restorer Gate, Auto Threshold and Auto Rate (Sheet 5)

Baseline correction is prevented during unipolar output signal intervals that exceed the baseline restorer threshold. Comparators U15A and U15B monitor the unipolar output signal and disable or gate off the baseline restorer for signals that exceed the automatic positive or fixed negative thresholds.

The auto baseline restorer threshold circuit, ICs U10 and U11, peak detects the negative noise excursions of the unipolar output signal and generates a positive dc reference voltage equal to the average value of the unipolar output noise level. This voltage serves as the baseline restorer gating reference that maintains precision for a wide range of amplifier conditions and applications.

Transistors Q15, Q18, capacitor C77 and the baseline restorer gate signal (PBLR) produce a count rate dependent voltage that programs the restorer rate.

6.9 Automatic Pole/Zero (Board 2, Sheets 4, 5, 6 and 7)

For RC preamplifiers with AFT set ON, pole/zero compensation is optimized automatically. The correct pole/zero compensation signal is provided by the auto pole/zero circuit.

Basically the pole/zero potentiometer usually found in a spectroscopy amplifier is replaced by a dual digital potentiometer and operational amplifier arrangement serving as an electronic attenuator. The electronic attenuator is controlled by digital control circuitry to provide the exact proportion of pole/zero signal for precise compensation.

An integrating sample-and-hold circuit samples the tail of the unipolar output signal and a comparator compares the sampled unipolar signal with respect to ground. If the unipolar signal is properly pole/zeroed, the unipolar signal tail and the sample-and-hold circuit’s output will be at zero volts. The conditions for proper pole/zero are satisfied and the circuit needs to make no adjustments. However if the pole/zero is not correct, the sample-and-hold circuit will produce an error voltage that is proportional to the amount of miscompensation.

When an auto pole/zero sequence is initiated, the comparator interrogating the unipolar signal tail via the sample-and-hold circuit directs the digital control circuity to increment or decrement the digital potentiometer one step at a time, in the appropriate direction, until correct pole/zero compensation is achieved. Convergence is obtained and the process stops when the unipolar tail and the sample-and-hold circuit’s outputs attain zero volts.

When AFT power is turned on, the BUSY LED blinks, prompting the operator to initiate the auto pole/zero sequence. When initiated, the BUSY LED will stay on continuously for the duration of the sequence and will turn off when convergence is achieved. Normally it takes only a short period of time to achieve convergence. However if convergence requires more than two minutes, the sequence is halted and the BUSY LED will again blink, indicating convergence was not achieved. Possible causes might be: the preamp signal fall time is outside the pole/zero adjustment range (40 µs to infinity); a significant portion of the unipolar pulses are outside the 7 to 10 volt correction window; or the count rate is too low or too high.

6.10 Pile Up Rejection (Sheet 7)

The Pile Up Rejector monitors the number of amplifier input events during a pulse processing sequence, starting with an amplifier input signal and ending when the unipolar signal returns to the baseline. If two or more events occur during a processing sequence and the ADC is in the acquisition mode, Linear Gate (LG) set true, the events are piled up and any pending ADC conversion is aborted.

The signal from gain AMP 4 is differentiated by the fast differentiator C110/C111 and R178, pole/zero compensated by R151 through R155 and R179, and amplified and limited by IC U27. Amplifier/limiter U27 is baseline restored by a fast gated-baseline restorer, which is made up of transconductance amplifier U26 and transistors Q16 and Q17. The fast discriminator, U18, monitors the amplifier/limiter output signal and generates a fast timing pulse (system trigger) whenever the fast signal exceeds the fast channel noise level referenced by the PUR discriminator threshold.

The PUR threshold is optimized automatically. The AUTO PUR threshold circuit includes ICs U19B and U20. The circuit and its operation is very similar to the auto baseline restorer threshold described in section 6.8.

The system trigger simultaneously clocks the PUR/LTC PLD. For the case of no pile up, only the DT* (Busy) will get set.

However, if a subsequent amplifier input signal arrives prior to the conclusion of the processing sequence (pile up), the REJECT signal will be set true. If the ADC is in the acquisition mode (LG true), a Reject will initiate an ADC reject sequence, the pending ADC conversion will be aborted and the events thrown away. At the conclusion of the processing sequence, the unipolar output signal returns to the baseline and the trailing edge of the restorer gate signal clears the BUSY and REJECT.

6.11 **Live Time Correction** (Sheet 7)

Live time correction is accomplished by extending the collection time (stopping the MCA live time clock) for the unipolar signal processing time, as determined by the amplifier busy and the Dead Time Extension (DTE) flip-flop (U24B), to allow replacement of events thrown away in the event of pile up.

The amplifier provides a DT (dead time) signal which is received by the ADC, it in turn adds it's dead time contribution producing a composite dead time signal for gating off the MCA live time clock.

Pile up events will produce multiple system triggers within the processing sequence. As described in section 6.10, the first trigger sets the Busy, and the second trigger sets the Reject. Reject is set true and the ADC aborts the conversion in process. The ADC Linear Gate (LG) ends prematurely and its positive transition clocks the DTE (Dead Time Extension) flip-flop true.

When the unipolar output signal returns to the baseline, the Busy and Reject flip-flops are cleared as before. However, the DTE flip-flop remains set and its Dead Time contribution continues.

For the next non-piled up processing sequence, the Reject flip-flop will not be set and the positive transition of the associated ADC LG signal will clock the DTE flip-flop reset ending its dead time contribution. At the conclusion of the unipolar output signal, the sequence finishes; the DT signal goes false and the MCA LIve Time clock resumes.

6.12 **ICB Control** (Board 2; Sheets 2 and 3)

Computer control of the Model 9615 Programmable Research Amplifier is done through the interface on Board 2.

The key component of the interface is 9615 PLD (U44), a Field Programmable Gate Array. Commands are received through the 20-pin ICB connector over an 8-bit Bidirectional Address/Data Bus. The module address is determined by the position of the 16-position rotary switch. A nonvolatile RAM (U34) is factory programmed with the module's serial number. The software controlling the module uses part of the RAM to retain the Fine Gain setting.

A 10-turn precision potentiometer, controlled by a stepping motor, sets the Fine Gain. The potentiometer control was used because it does not compromise amplifier performance as would a D/A converter. The motor control circuitry resides mainly in PLD U44; the driver and index sensor are shown on sheet 3.

The pole/zero circuitry described earlier has an ICB readout and loading capability. This allows the software to store the P/Z setting for the detector and the shaping. Thus when power is turned ON, the MCA software can load these values back into the Model 9615, avoiding manual initiation of a P/Z convergence cycle. The shaping time currently selected is compared with the value associated with the P/Z setting; an error indication is given in the MCA status if the shapings are not equal. In this case, a P/Z cycle would be required.

The other programmable functions of the amplifer are set through logic from the 9615 PLD. These include:

Coarse Gain
Super Fine Gain
Polarity
Differential/Normal Modes
Baseline Restorer Mode
PUR/LTC

A. Specifications

A.1 Inputs

NORM **-** Accepts Positive or negative tail pulses; amplitude 10 V divided by the selected gain, 25 V maximum; rise time less than shaping time constant; decay time constant: 40 µs to ∞; polarity programmable; 2.1 kΩ > R_{in} > 0.5 kΩ, R_{in} changes with Gain and Polarity setting; front and rear panel BNC connectors.

DIFF **-** Accepts a preamplifier ground reference when using the differential input mode; operates only when the DIFF mode is selected; programmable; 9 V maximum common mode; 2.1 kΩ > R_{in} > 0.5 kΩ, R_{in} changes with Gain and Polarity setting.

INHIBIT **-** Accepts a standard logic signal from associated reset preamplifier; used to extend the Dead Time signal, inhibit and reset the pile up rejector and provide reject to ADC during the preamplifier's reset cycle; positive true or negative true signal polarities, programmable; loading 4.7 kΩ; logic high 3.6 V, logic low <1 V; maximum 12 V; rear panel BNC connector.

LG (LINEAR GATE) **-** Accepts a standard TTL logic signal from associated ADC. Indicates to the Model 9615 that the ADC is acquiring an event; logic low during ADC Linear Gate time, returns high at conclusion; loading; 4.7 kΩ, pull up resistor to +5 V; accessible through pin 1 of the rear panel PUR connector.

ICB **-** Provides for connection to the Instrument Control Bus. Computer control of the Model 9615 is through this interface.

A.2 Outputs

UNIPOLAR **-** Provides positive, linear actively filtered shaped pulses; amplitude linear to +10 V, 12 V max; dc restored; output dc level factory calibrated to 0±5 mV; front panel Z_{out} <1 Ω or 93 Ω, internally selectable; rear panel Z_{out} is 93 Ω; short circuit protected; front and rear panel BNC connectors.

DT/BSY **-** Rear panel BNC with two functions: Dead Time or Busy Time, programmable; TTL output with 1 kΩ pull up resistor through a 47 Ω series resistor.

DT Provides a negative true TTL logic signal and when ORed with ADC dead time, provides Live Time correction for the amplifier and pile up rejector; active only when PUR is selected.

BSY Provides a negative true TTL logic signal that represents the amplifier busy time; logic low during amplifier processing time or from external INHIBIT.

REJECT **-** Provides a positive true TTL logic signal used to initiate an ADC reject sequence for corresponding piled up events with PUR selected or reject when the preamplifier's Inhibit signal is true; logic high to reject, logic low otherwise; TTL output with 1 kΩ pull up resistor through 47 Ω series resistor; accessible through pin 2 of the rear panel PUR connector.

ICR (Incoming Count Rate) **-** Provides a standard TTL logic signal corresponding to input count rate; positive true; width nominally 150 ns, TTL output with 1 kΩ pull up resistor through 47 Ω output; rear panel BNC connector.

ICB **-** Provides feedback to the computer of the Model 9615's status.

A.3 Manual Controls

SHAPING - Rotary switch selects amplifier shaping time constants of 0.5, 1, 2, 4, 6 and 12 μs; computer able to read position; rear panel.

DIFFERENTIAL MODE BALANCE - Fifteen-turn potentiometer maximizes the common mode rejection when Differential Mode is enabled; front panel adjustment.

ADDRESS - Rotary switch selects 1 of 16 unique ICB addresses; accessible through an opening in the side cover.

A.4 ICB Programmable Controls

COARSE GAIN - C1: 1, 2; C2: 1,10; C3: 1, 2,5,10.

FINE GAIN - Range: 1 to 3.

SUPER FINE GAIN - Range: 0.998 to 1.002.

OVERALL GAIN - Product of 2.5 x C1 x C2 x C3 x fine gain x super fine gain.

INPUT POLARITY - Positive or Negative.

DIFFERENTIAL MODE - Enable or Disable.

SHAPING MODE - Gaussian or Triangular.

PREAMPLIFIER TYPE - R-C or TRP.

POLE/ZERO - Matching value.

BASELINE RESTORER - Symmetrical or Asymmetrical.

PUR MODE - On or Off.

LTC OUTPUT - Dead Time (DT) or Busy (BSY).

INHIBIT POLARITY - TTL High or TTL Low true.

A.5 Front Panel Indicators

READY - Bi-color LED; green when on-line; yellow for fault or error; off when the module is waiting for the computer to recognize it.

ACTIVE - LED; flashes for each input signal.

P/Z BUSY - LED; active if R-C Preamplifier selected: blinks at power up or if optimal P/Z setting is not achieved within 2 minutes; on continuously while Auto P/Z is attempting to match to input waveform; off when P/Z matching is achieved or TRP preamplifier selected.

PUR ON/OFF - LED; on when PUR/LTC mode enabled.

PUR ACCEPT/REJECT - Three color LED: flashes green for each nonpiled-up input; flashes red for each piled up event; green for <40% rejected events; yellow for 40 to 70% rejected events; red for >70% rejected events.

DIFFERENTIAL MODE ENABLED - LED.

A.6 Performance

GAIN RANGE - Continuously variable from X2.5 TO X1500; programmable.

OPERATING TEMPERATURE RANGE - 0 to 50 °C.

GAIN DRIFT - ≤±0.005%/°C; dc level ≤±7.5 μV/°C.

INTEGRAL NONLINEARITY - ≤±0.04% over total output range for 2 μs shaping.

OVERLOAD RECOVERY - Output recovers to within ±2% of full scale output from X1000 overload in 2.5 non-overload pulse widths at full gain, at any shaping time constant, and with preamplifier matching properly set.

NOISE CONTRIBUTION - ±4.5 μV true rms, output referred to input, 2 μs shaping, and amplifier gain ≥100.

PULSE SHAPING - Near-Gaussian or near-Triangular shape; one differentiator; three active filter integrators realizing eight-pole shaping network; shaping time parameters referenced to 1 μs are listed in the following table:

	Shaping Time Multiplier	
Parameter	**Triangular**	**Gaussian**
Time to peak	12.7	2.9
0.1% full scale output to peak	2.5	2.2
Pulse width at half maximum	2.5	2.1
Pulse width at tenth maximum	5.6	5.0
Pulse width at 1/100 maximum	6.7	6.2

RESTORER - Active gated.

SPECTRUM BROADENING - The FWHM of ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 100 kcps and a 9 V pulse height will typically change less than 6% with a 2 μs shaping; asymmetrical restorer mode; TRP preamplifier. These results may not be reproducible if the associated detector exhibits an inordinate amount of long rise time signals.

COUNT RATE STABILITY - The peak position of a ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 100 kcps and a 9 V pulse height will typically shift less than 0.02% with 2 μs shaping; asymmetrical restorer mode; TRP preamplifier.

COMMON MODE REJECTION - >60 dB at 60 Hz; >20 dB at 1 MHz; balanced lines.

A.7 Pileup Rejector/Live Time Corrector

PULSE PAIR RESOLUTION - ≤500 ns.

MINIMUM DETECTABLE SIGNAL - Limited by detector/preamplifier noise characteristics.

A.8 ICB Programming Summary

Setup Parameters	Read	Write
Preamplifier Type	X	X
Differential Mode	X	X
Input Polarity	X	X
Shaping Mode	X	X
Shaping	X	
Gain	X	X
Baseline Restorer Mode	X	X
Pole/Zero Setting	X	X
PUR On/Off	X	X
LTC Output	X	X
Inhibit Polarity	X	X
Module Status		
ICB Address	X	
Model Number	X	
Factory Serial Number	X	
Power-On Reset	X	
Pole/Zero Converging or Error	X	
Control		
Place On-Line (READY Indicator - Green)	X	X
Take Off-Line (READY Indicator - Off)	X	X
Problem Alert (READY Indicator - Yellow)	X	X
Activate Pole/Zero Convergence		X

A.9 Power Requirements

+24 V dc – 90 mA	+12 V dc – 200 mA
–24 V dc – 125 mA	–12 V dc – 120 mA
	+6 V dc – 1 A

A.10 Connectors

With the exception of the PUR, Preamplifier Power, and ICB connectors, all signal connectors are BNC type.

PUR - Rear panel, Molex plug 03-06-1031.

PREAMPLIFIER POWER - Rear panel, Amphenol, type 17-10070.

ICB - Rear panel, 20 pin ribbon.

A.11 Accessories

C1514 - LTC/PUR and DT cable.

A.12 Cables

A 12-port connecting cable is supplied with each Model 556 AIM; if the cable is ordered separately, specify Model C1560 12-port ICB Connecting Cable.

A.13 Physical

SIZE - Standard double width NIM module 6.86 x 22.12 cm (2.70 x 8.71 in.) per DOE/ER-0457T.

NET WEIGHT - 1.85 kg (4.1 lb)

SHIPPING WEIGHT - 2.94 kg (6.5 lb)

B. Internal Controls

Internal jumpers have been factory set for optimum performance in the most common spectroscopy applications, but may easily be changed for a custom application. The jumpers should be set as required before installing the 9615 in the NIM Bin.

B.1 Main Board Internal Controls

The jumpers on the main board can be changed by removing the module's left side-cover.

Output Impedance

The front panel UNIpolar Output impedance is factory set for ≤1 ohm. It can be changed to Z_{out} of 93 ohms.

Jumper W2 – Unipolar Output Impedance

Position 1/2:	≤1 ohm
Position 2/3:	93 ohms

The rear panel UNIpolar output has a fixed impedance of 93 ohms, series connected.

When using the front panel low impedance output, short lengths of interconnecting coaxial cable need not be terminated. To prevent possible oscillations, longer cable lengths should be terminated at the receiving end in a resistive load equal to the cable impedance (93 ohms for type RG-62 cable).

The 93 ohm output may be safely used with RG-62 cable up to a few hundred feet. However, the 93 ohm impedance is in series with the load impedance, and a decrease in the total signal range may occur. For example, a 50% loss will result if the load impedance is 93 ohms.

B.2 Board 2 Internal Controls

The jumpers on Board 2 are used only during factory setup and are not changed during normal operation or maintenance.

The ICB Address Selector (SW1) is a 16 position rotary switch accessible through a hole in the right side cover. Its position must be different from all other modules connected on its Instrument Control Bus (ICB).

W1 P/Z Sampling

Position 1/2:	Normal
Position 2/3:	Factory Calibration

W2 NOVRAM Setup

Jumper Removed:	Normal
Jumper Installed:	Factory Setup

C. Performance Adjustments

C.1 Baseline Restorer Mode and Rate

The baseline restorer in the Model 9615 is flexible in that both the SYMmetrical and ASYMmetrical modes are offered. In the SYMmetrical mode, the restoration currents are identical for above and below the baseline. For the ASYMmetrical mode the restorer current above the baseline (referenced to a positive output), is much less than that below the baseline.

The ASYMmetrical restorer mode offers superior high count rate performance for high resolution Ge spectroscopy. The SYMmetrical mode is used on Ge systems with low quality preamps, scintillation and proportional counting, and Si systems.

The SYMmetrical mode should always be used for detector systems which exhibit baseline discontinuities resulting from excessive noise and/or high voltage effects, preamp reset pulses and preamp secondary time constants. Secondary preamp fall time constants result in unipolar output undershoots making it difficult to optimize the amplifier preamp matching.

C.2 Amplifier Shaping Selection

Shaping time constant selection generally is a compromise between optimizing throughput and resolution.

For germanium detectors, 4 µs shaping provides optimum resolution at low count rates, but 2 µs provides better performance over a wider range of count rates and at high count rates.

For high resolution detectors, longer shaping time constants offer better signal to noise (S/N) ratio and reduced sensitivity to the effects of detector ballistic deficit. However, as the system count rate increases, resolution will degrade rapidly as a result of the amplifier's long processing time and the effects of pulse pile-up.

The optimum shaping-time constant depends on the detector characteristics (such as size, noise characteristics and collection characteristics), preamplifier and incoming count rate. Below is a list of shaping-time constant ranges for other common detectors.

Detector	Shaping (µs)
Scintillation Photomultiplier [NaI(Tl)]	0.5 or 1
Planar Implanted Passive Silicon (PIPS)	0.5, 1 or 2
Gas Proportional Counter	0.5, 1 or 2
Lithium Drifted Silicon [Si(Li)]	6 or 12
Lithium Drifted Germanium [Ge(Li)]	2 or 4
Planar Germanium	4, 6 or 12
Silicon Surface-Barrier (SSB)	0.5

Refer to the specific Detector Operator's Manual for the recommended shaping time. This will be a good starting point.

Further refinements may be realized through experimentation. Collect spectra using shaping times above and below the recommended to find the one that provides optimal resolution performance for your particular detector and application.

NOTE: The P/Z matching must be adjusted each time the shaping is changed.

C.3 Operation With Reset Preamps

The Model 9615 is fully compatible with most reset type preamps.

Reset preamps use an electronic circuit, as opposed to a feedback resistor to restore the preamp output back to a reference level. As a result, the reset preamp output is a succession of step functions that staircase or ramp up to an upper limit that initiates a preamp reset.

Since the reset preamp signal does not have the characteristic exponential fall time as with RC preamps there is no requirement for Pole/Zero compensation.

P/Z Compensation With Reset Preamps

Reset Preamps do not require pole/zero compensation. When using the Model 9615 with a reset preamp, select a preamp type of TRP which automatically will reduce the Pole/Zero compensation to zero.

Using the Reset Preamp Inhibit Signal

The preamp reset event produces a large signal to the amplifier driving it into a severe overload condition. The Model 9615 recovers from overload events rapidly and monotonically requiring approximately two non-overload pulse widths to fully recover.

Converting events during amplifier overload may produce spectral distortion and it is recommended that the ADC be gated off during this time using the preamp INHIBIT signal. The preamp INHIBIT signal width should be adjusted to encompass the full unipolar signal recovery. Please consult the Detector/Preamp Operator’s Manual for this adjustment. The INHIBIT signal from the Model 2101 Transistor Reset Preamp or Model 2008 Optical Reset Preamp is positive true.

Connect this signal to the amplifier’s INHIBIT input and set the programmable Inhibit polarity to the proper level. The REJECT signal on the PUR cable from amplifier to ADC will discard pulses during the Inhibit with PUR mode either ON or OFF.

Overload Recovery

Some preamps produce undesirable secondary effects following the preamp reset. The secondary effects may result from long time constants or non-linearities producing excessive unipolar output signal recovery time. System throughput may be compromised and in extreme cases premature baseline instability may result at high count rates.

The 9615 amplifier automatically gates off the baseline restorer (BLR) for normal detector signals and preamp reset events to maintain signal precision.

D. Rear Panel Connectors

NORM
Tail pulse input; BNC connector.

DIFF
Preamplifier Ground Reference input Differential Input mode; BNC connector.

INHIBIT
CMOS compatible input from reset preamp; programmable logic polarity; BNC connector.

PREAMP POWER (Outputs)
9-pin female D-type connector.

+24 V . . . . . . Pin 7
+12 V . . . . . . Pin 4
–12 V . . . . . . Pin 9
–24 V . . . . . . Pin 6
Ground . . . . . . Pins 1 and 2

UNI OUT
Unipolar output; 0 to >10 V; Z_{out} = 93 Ω; BNC connector.

ICR
Positive TTL output pulse generated for every preamplifier input processed; ≈150 ns width; BNC connector.

DT/BSY
Dead Time or Busy output; TTL compatible; programmable; BNC connector.

LTC/PUR
TTL Pileup Rejection and Live Time Correction signals; 3-pin Molex plug, type 03-06-1031

LG* (In) . . . . . Pin 1
REJECT (Out) . . Pin 2
Ground . . . . . . Pin 3

NIM Power (Input)
42-pin NIM standard male connector.

+12 V . . . . . . Pin 16
–12 V . . . . . . Pin 17
+24 V . . . . . . Pin 28
–24 V . . . . . . Pin 29
+6 V . . . . . . Pin 10
Ground . . . . . . Pin 34

ICB Interface Connector

This 20-pin ribbon connector (JICB in Figure 2.4) provides all the necessary signals for connecting the Instrument Control Bus (ICB). Negative true signals are shown with a trailing asterisk; Address/Data signals (LDn) are positive true.

Pin	Signal	Pin	Signal
1	GND	2	LD0
3	LD1	4	GND
5	LD2	6	LD3
7	GND	8	LD4
9	LD5	10	GND
11	LD6	12	LD7
13	GND	14	LWE*
15	GND	16	LDS*
17	GND	18	LAS*
19	GND	20	LSRQ*

Interface Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (LWE*), in which case the signal is considered to be a logic 1 for a low voltage level. The direction of the signal is referenced to the amplifier.

Signal	Pin	Direction	Description
LD0	2	Input/Output	Address/Data line 0 (LSB)
LD1	3	Input/Output	Address/Data line 1
LD2	5	Input/Output	Address/Data line 2
LD3	6	Input/Output	Address/Data line 3
LD4	8	Input/Output	Address/Data line 4
LD5	9	Input/Output	Address/Data line 5
LD6	11	Input/Output	Address/Data line 6

Signal	Pin	Direction	Description
LD7	12	Input/Output	Address/Data line 7
LWE*	14	Input	(Write Enable) This signal is active when the ICB Master is writing to the ICB.
LDS*	16	Input	(Data Strobe) Used to latch the data into a slave during a write cycle or gate the data onto the bus during a read cycle.
LAS*	18	Input	(Address Strobe) Used to latch the address which the ICB Master is accessing into the slave units.
LSRQ*	20	Output	(System Request) This signal is set when the slave requires service from the ICB Master.
GND	1, 4, 7, 10, 13, 15, 17, 19	———	DC common for all interface signals.

E. Environmental Specifications

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e., a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- a rack or tabletop enclosure fully closed on all sides with rear door access
- single point external cable access
- blank panels to cover open front panel bin areas
- compliant grounding and safety precautions for any internal power distribution
- the use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered may affect the unit's compliance to the specified EU requirements.

Operating Temperature: 0-50 degrees Centigrade
Operating Humidity: 0-80% Relative, Non-condensing
Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution degree 2

Preventative maintenance

Preventative maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap, side or rear panels.

Warranty

Canberra (we, us, our) warrants to the customer (you, your) that for a period of ninety (90) days from the date of shipment, software provided by us in connection with equipment manufactured by us shall operate in accordance with applicable specifications when used with equipment manufactured by us and that the media on which the software is provided shall be free from defects. We also warrant that (A) equipment manufactured by us shall be free from defects in materials and workmanship for a period of one (1) year from the date of shipment of such equipment, and (B) services performed by us in connection with such equipment, such as site supervision and installation services relating to the equipment, shall be free from defects for a period of one (1) year from the date of performance of such services.

If defects in materials or workmanship are discovered within the applicable warranty period as set forth above, we shall, at our option and cost, (A) in the case of defective software or equipment, either repair or replace the software or equipment, or (B) in the case of defective services, reperform such services.

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EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident, neglect or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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