Model 8713
ADC

9231459A 4/99

User's Manual

ISO 9001
SYSTEM
CERTIFIED

CE

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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

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Table of Contents

1. Description

The Model 8713, Fixed Dead Time analog-to-digital converter is designed for high resolution nuclear spectroscopy. Its fast conversion time allows it to process a full scale input pulse in less than 6 µs. Fast throughput combined with 16K Gain Range make the 8713 the best choice when speed and resolution are both critical.

The 8713 boasts differential and integral linearity performance that until now was only possible with Wilkinson ADCs, Its exceptional linearity improves peak shape and resolution, thereby improving the overall performance of your spectroscopy system.

Concentric Gain and Range controls together with Digital Offset allow the user to maximize the use of limited MCA memory by selecting only the specific energy range of interest. This can be particularly useful for multi-input applications such as alpha spectroscopy, thus eliminating the need for older biased amplifiers. These digital controls accomplish the same end more accurately and repeatably.

Conversion for the Pulse Height Analysis (PHA) mode can be initiated Automatically using an internal peak detector operating on the input pulse, or can be Delayed up to 100 µs after the leading edge of the input pulse passes the LLD. A front panel Inspect test point is provided so that the user can monitor the Linear Gate (LG) time between LLD crossing and the beginning of conversion for either mode. Conversions may be enabled/disabled by Coincidence/Anticoincidence gating applied at any time during the Linear Gate Interval.

Voltage sampling and subsequent conversion for the Sample Voltage Analysis mode is initiated by the leading and trailing edges respectively of a Gate pulse applied in the Coincidence mode. The same LLD and ULD limits are used for acceptance of the peak input during the positive gate time.

The 8713, provides front panel, screwdriver adjustable, multi-turn potentiometers for the control of the Lower and Upper Level Discriminators, as well as the ADC Zero.

The 8713 provides the connections required for use with current Canberra amplifiers that perform pileup rejection and live time correction (PUR/LTC). These ADC/amplifier interfaces are also required to use the Westphal Loss Free Counting or Precision Live Time techniques.[1]

The 8713 ADC is fully compatible with all current Canberra MCAs (with external ADC interface options), Digital Stabilizer and Analog Multiplexers.

1. G. P. Westphal, Nuclear Instruments and Methods 163 (1979) 189-196.

2. Controls and Connectors

2.1 Front Panel

This is a brief description of the 8713's front panel controls and connectors. For more detailed information, refer to Appendix A, Specifications.

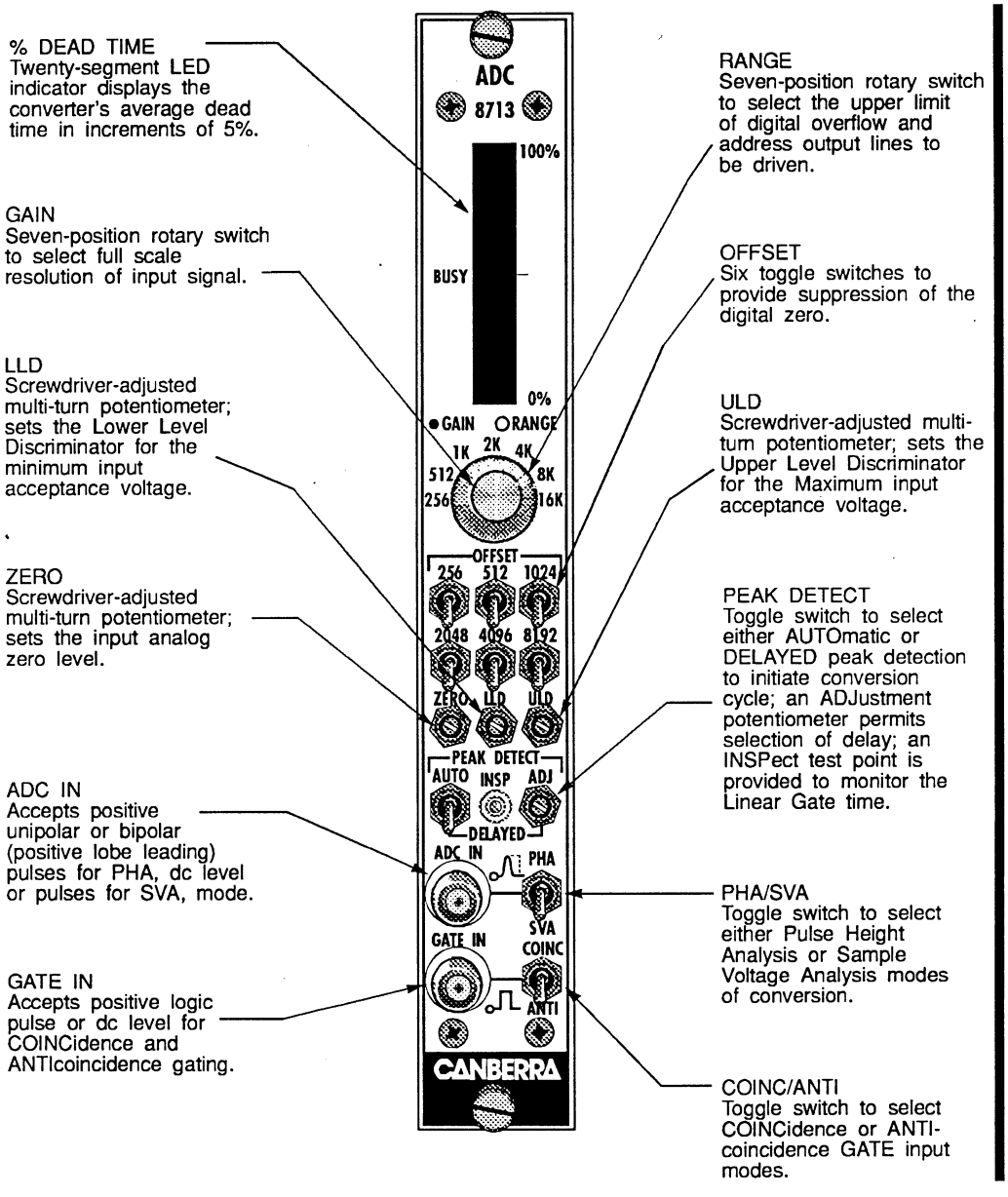

Figure 2.1 Front Panel Controls

2.2 Rear Panel

This is a brief description of the 8713's rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

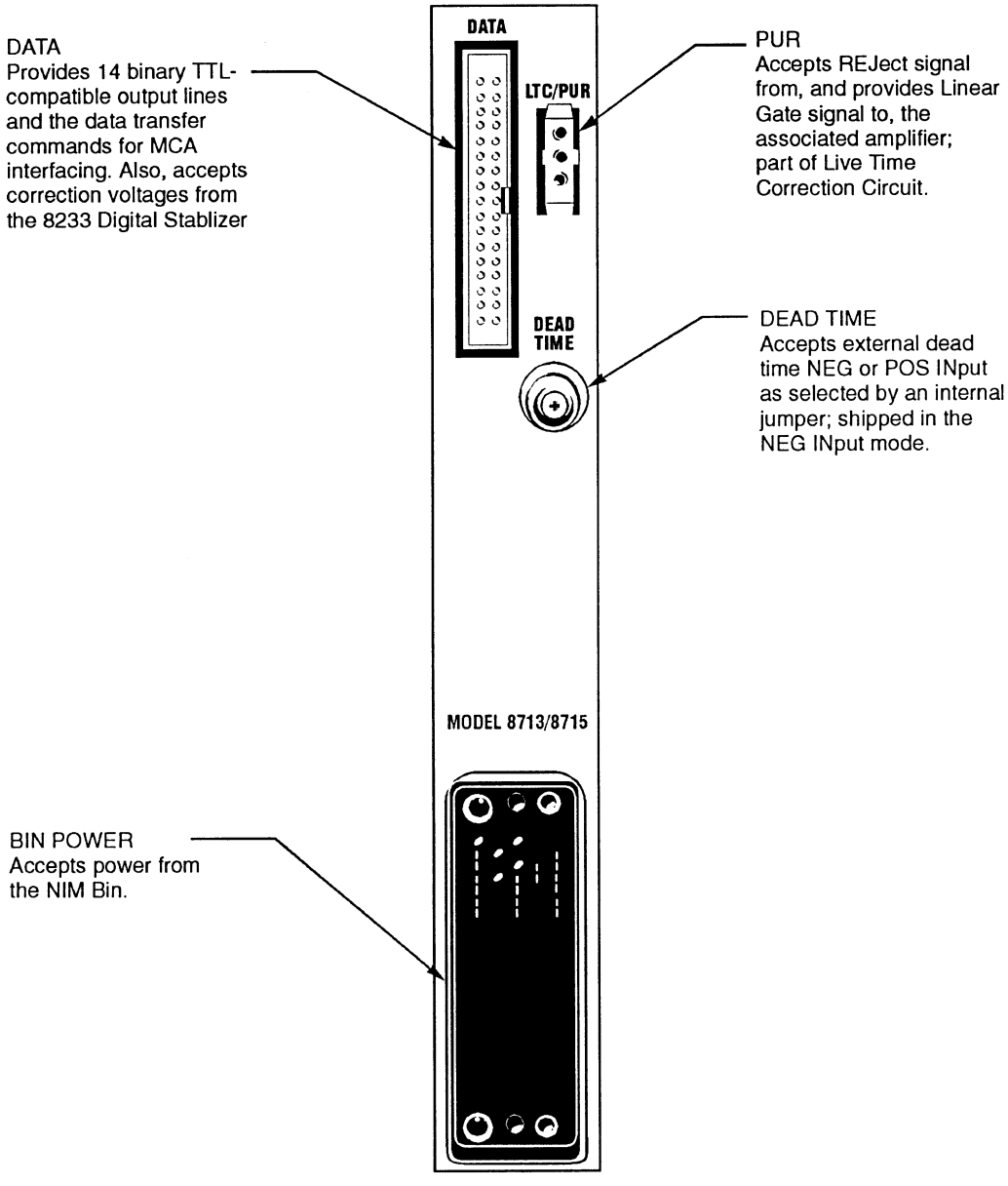

Figure 2.2 Rear Panel Controls

2.3 Internal Controls

The internal jumper plug controls should be set for your specific requirements before applying power to the module.

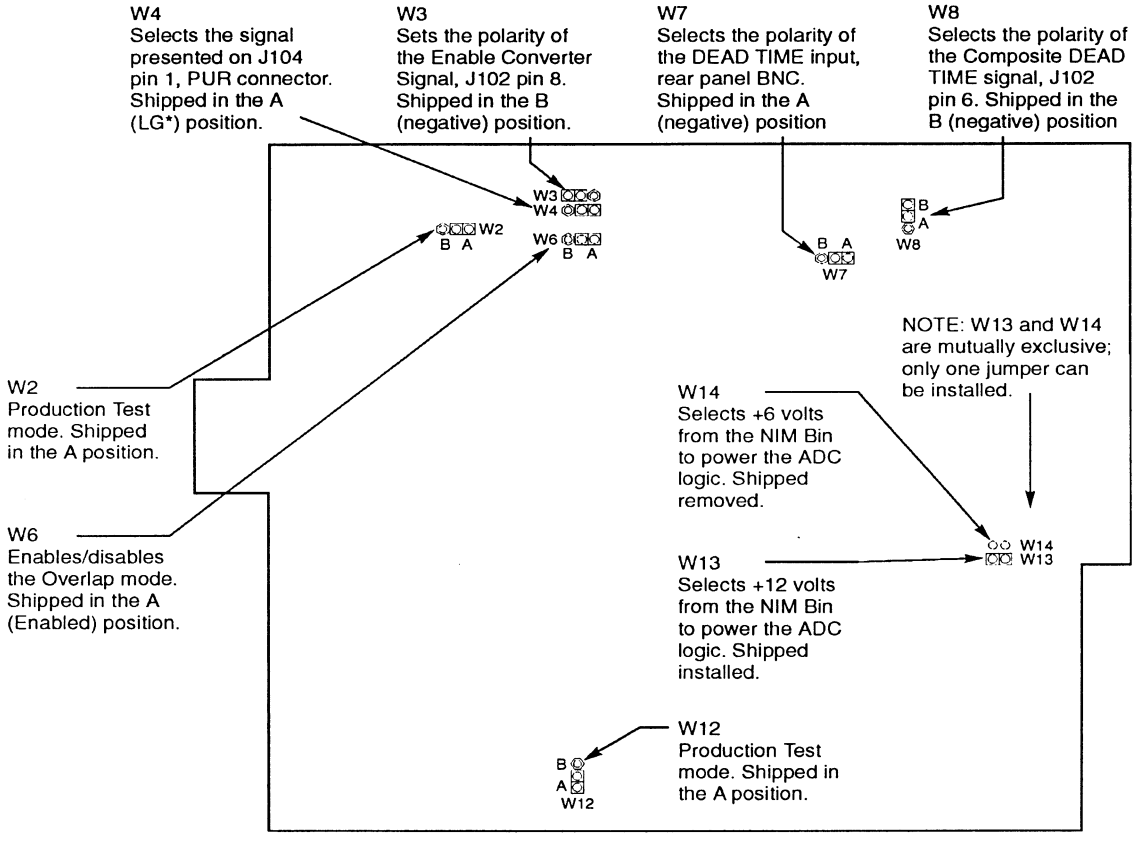

Figure 2.3 Internal Controls

3. Operation

This section discusses the use of the 8713's controls and functions.

3.1 Busy

The BUSY indicator is 20-segment LED display which shows the average dead time in increments of five percent. Dead time is the time that the ADC is busy converting an input and increases proportionately with increases in conversions per unit time.

3.2 Gain

The GAIN controls the ADC's resolution; that is, the number of parts into which the full-scale (10 V) inputs can be divided. The larger the selected gain, the finer the divisions and the greater the resolution.

3.3 Range

The RANGE switch is commonly set to equal the size of the MCA memory group assigned to the ADC. For instance a memory assignment of 4096 channels would require a RANGE of 4096.

Inputs which exceed the selected RANGE will not be stored in the MCA's memory. Since the range check is made after the input has been converted, these conversions will add to the ADC's dead time.

3.4 Offset

The OFFSET is used to precisely shift the memory assignment of the ADC's conversions. With no OFFSET (all switches down), the ADC's channel numbers are the same as the memory's channel numbers.

For example, if the GAIN is set to 8192 and the memory assignment is only 4096, an OFFSET of zero will allow only the lower half of the full-scale conversions to be stored. That is, pulses up to five volts will be stored, pulses greater than five volts will not be stored.

If, in this example, the OFFSET were set to 4096 (the 4096 switch up), channel 4096 of the ADC would be shifted down to correspond to channel zero of the memory. This offset would allow the upper half of the full-scale conversions, those above five volts, to be stored in the assigned MCA memory.

3.5 LLD and ULD

The Lower Level Discriminator (LLD) and the Upper Level Discriminator (ULD) controls set the limits for the input signals to be accepted by the ADC for conversion. If an input pulse falls within the selected window (higher than the LLD setting but lower than the ULD setting) the input will be converted. If the input does not fall within the window, the input will not be converted. The window check is made at the conclusion of the linear gate time. An input pulse outside of the window will add to the ADC's dead time, since no pulses may be accepted for processing by the ADC while the linear gate is open.

3.6 Zero

The ZERO control varies the zero intercept of the ADC conversion so that zero energy is stored in the memory's channel zero. The Model 8713 is shipped with the ZERO set for a GAIN of 8192. For other gains, a slight adjustment of the control may be necessary for precise energy calibration.

For accurate setting of the ZERO control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. Connect the Pulser's SIGNAL OUT to the ADC Input.
2. Set the Pulser to HI, 0°, +, and 0.5 µsec Rise Time.
3. Set the ADC's GAIN control as desired.
4. Set all binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY on, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.
5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be switched in on the ADC. For instance, if the memory is 4096 channels and the GAIN is set for 8192, an OFFSET of 4096 must be added so that conversion can take place in the highest channel of the memory.
6. Turn all binary switches on the Model 8210 OFF, except the 1/64 switch, which should be left ON.
7. Set all OFFSET switches on the ADC to the OFF (down) position.
8. Adjust the ZERO control so that counts are being collected in the proper channel, as follows:

Gain	Channel
16 384	256
8192	128
4096	64
2048	32
1024	16
512	8
256	4

9. Repeat steps 4 through 8 until no further adjustments are necessary.

3.7 Peak Detect

The linear gate, which allows a valid input to be acquired, is normally open. In the AUTO mode, the linear gate closes when the peak amplitude of the input pulse has been detected. Wide input pulses may make the AUTOmatic detection of the peak amplitude uncertain. To overcome this uncertainty, the DELAYED peak detect mode may be used. In the DELAYED mode, the linear gate closes at the end of a selectable time delay. This time delay can be set with the ADJ control while monitoring the INSP test point adjacent to the control. The adjustment range is from 2 to 100 µs.

The INSP test point provides a positive logic pulse which starts when the input crosses the threshold and ends when the linear gate closes. The threshold voltage follows the LLD setting up to 500 mV maximum. Note that the signal must return below the threshold to allow the ADC to accept a second input. Therefore, the input signal's baseline must be below 500 mV for proper ADC operation.

3.8 Gate

Input pulse conversions may be enabled or disabled by using the GATE function. This function is not the same as the linear gate, which is an internal circuit.

In the COINC mode, a positive logic pulse at least 250 ns wide or a positive dc level must be present at the GATE connector during the linear gate time. The linear gate time is defined as the time the input crosses the threshold to the closing of the linear gate and can be monitored at the INSP test point.

Since a common gating signal is the output of an independent SCA module, this late-arriving pulse can be accommodated by using the DELAYED peak detect mode and adjusting the linear gate time, as seen at the INSP test point, so that the linear gate closes after the SCA's output arrives. Thus the need for delaying the ADC INput signal can be eliminated.

If the GATE input is low during the entire linear gate time, conversion will not take place.

In the ANTIcoincidence mode, the logic sense of the GATE signal is inverted. That is, a logic low will enable the linear gate and a logic high will disable it.

In any gating mode, an open GATE (nothing connected to the GATE connector) acts as if an enabling level were present.

3.9 Sampled Voltage Analysis

The ADC is usually used in the Pulse Height Analysis (PHA) mode, but by changing the PHA/SVA switch to the SVA position, analog voltages can be sampled by the ADC. The result will be an amplitude distribution curve of the input signal. The input signal must be between 0 and 10 V in amplitude to be sampled. If desired, an amplitude window may be set with the LLD and ULD controls.

The GATE input supplies the sampling signal, which must be equal to or greater than 1 μs in width. However, for pulse inputs (rather than dc levels or slowly changing ac signals), the GATE input signal must be narrower than the input pulse width.

In SVA, the GATE input can also be used to trigger the Delay Timer by placing the AUTO/DELAYED switch to the DELAYED position. This mode allows the use of Gate Inputs which are narrower than 1 μs. In this configuration, the COINC/ANTI switch is used to select the triggering edge, rising or falling. COINC selects rising and ANTI selects falling. As in the PHA mode, the ADJ control is used to set the delay time.

The sampling rate should be at least twice the frequency of the input signal for accurate sampling.

3.10 Rear Panel Connectors

J106 DEAD TIME – A BNC connector which is used as an external dead time input from Canberra Amplifiers equipped with PUR/LTC. This input is ORed with the ADC Dead Time.

Accepts a negative or positive logic signal jumper, selectable via W7; shipped in the A (negative) position.

J102 DATA – Used to connect the ADC to an MCA, an AMX, a Digital Stabilizer, or an LFC module. The proper cable is supplied with the MCA.

J105 LTC/PUR – Accepts the REJect signal from, and provides the Linear Gate (LG) signal to, Canberra Amplifiers equipped with PUR/LTC.

Further information and signal specifications for these connectors can be found in Appendix A, Specifications.

3.11 ADC Interfacing

This ADC improves its throughput by using a data buffer, or overlap mode, which allows the ADC to accept another analog input and start converting it while the previous conversion is being transferred from the buffer to the memory unit. In the unlikely event that the conversion finishes before the previous data has been transferred from the buffer, the new data is held in the counter and no new conversion can start until the DATA ACCEPTED signal is received. No valid conversion data is discarded by the ADC.

The result of the ADC's conversion is a 14-bit binary-coded number. At the end of the conversion, this number is transferred into the data buffer and signal DATA READY is set true. The address data can now be used by the MCA and the ADC is free to begin another conversion.

The DATA lines are driven by tri-state drivers that are controlled by the ENABLE DATA input. The DATA ACCEPTED input signals the ADC that the current output data has been transferred and the result of the next conversion can be loaded into the buffer.

In a synchronous application, such as Multiparameter Acquisition, it is necessary to operate the ADC in a non-overlap mode, which disables the internal buffer. In this mode, the ADC cannot accept a second input for conversion until the first conversion has been accepted by the MCA. The non-overlap mode is selected by placing W6 in the B position. The ADC is also automatically placed in the non-overlap mode when used in SVA. This is required by the 8223 and 8224 AMX modules.

Invalid inputs are not normally stored by the MCA. In the overlap mode, invalid inputs are converted but are not stored in the buffer and the DATA READY signal is not generated. In the SVA and non-overlap modes, invalid events are converted and the ADC generates the DATA READY and INHIBIT output signals. This causes the MCA to service the ADC; that is, the DATA ACCEPT and ENABLE DATA signals will be generated, but the data will not be stored by the MCA because of the INHIBIT signal. Invalid inputs are defined in "Invalid Flag Conditions" on page 9.

It may sometimes be necessary to record all inputs whether valid or not. This is true for Multiparameter or other synchronous applications. For this case, the ADC must be configured in the non-overlap mode, W6 in the B position. In this configuration the INHIBIT signal is now considered an INVALID signal, flagging an invalid input but not inhibiting storage. The multiparameter MCA would use this INVALID indication as an input to record these type of events.

The ENABLE CONVERTER input (J102, pin 8) or the front panel GATE input can be used to inhibit a later conversion and thus synchronize multiple ADCs.

The COMPOSITE DEAD TIME output is the sum of the conversion time and the time that the input is above the threshold. The output signal begins when the input signal exceeds the input threshold and ends when the conversion is complete or the input signal goes back below the input threshold, whichever time is longer.

If an external Live Time Corrector (for example, the Model 2024 or 2025 Amp) is used, its BUSY signal is summed with the ADC DEAD TIME. The ENABLE CONVERTER signal and gate signal make no contribution to the dead time, although when false, they do inhibit conversion.

3.12 Invalid Flag Conditions

For a conversion to be accepted, it must meet all of the following criteria. When violated, the INVALID flag (J102, pin 12) will be set if the ADC is configured for this mode.

SCA Window

Pulses not in the SCA's analog window will be rejected, initiating a dump cycle. An LLD or a ULD violation will generate the INVALID flag. Both states are interrogated at the peak detection time.

Digital Underflow

Input pulses resulting in a numeric conversion less than the ADC ZERO baseline or less than the digital offset, or both, will be rejected by inhibiting ADC READY. The INVALID flag will be set at the end of LOAD (transfer of data from converter).

Digital Overflow

Input pulses resulting in a numeric conversion greater than the ADC RANGE will be rejected by inhibiting ADC READY. The INVALID flag will be set at the end of LOAD (transfer of data from converter).

Coincidence/Anticoincidence

The GATE pulse width must be at least 250 ns wide and be true (high for coincidence, low for anticoincidence) for at least 100 ns before the peak detection point or the end of Linear Gate. Otherwise the conversion is aborted by initiating a dump cycle. The INVALID flag will be set at the peak detection point.

3.13 Preventative Maintenance

Preventative maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap, side or rear panels.

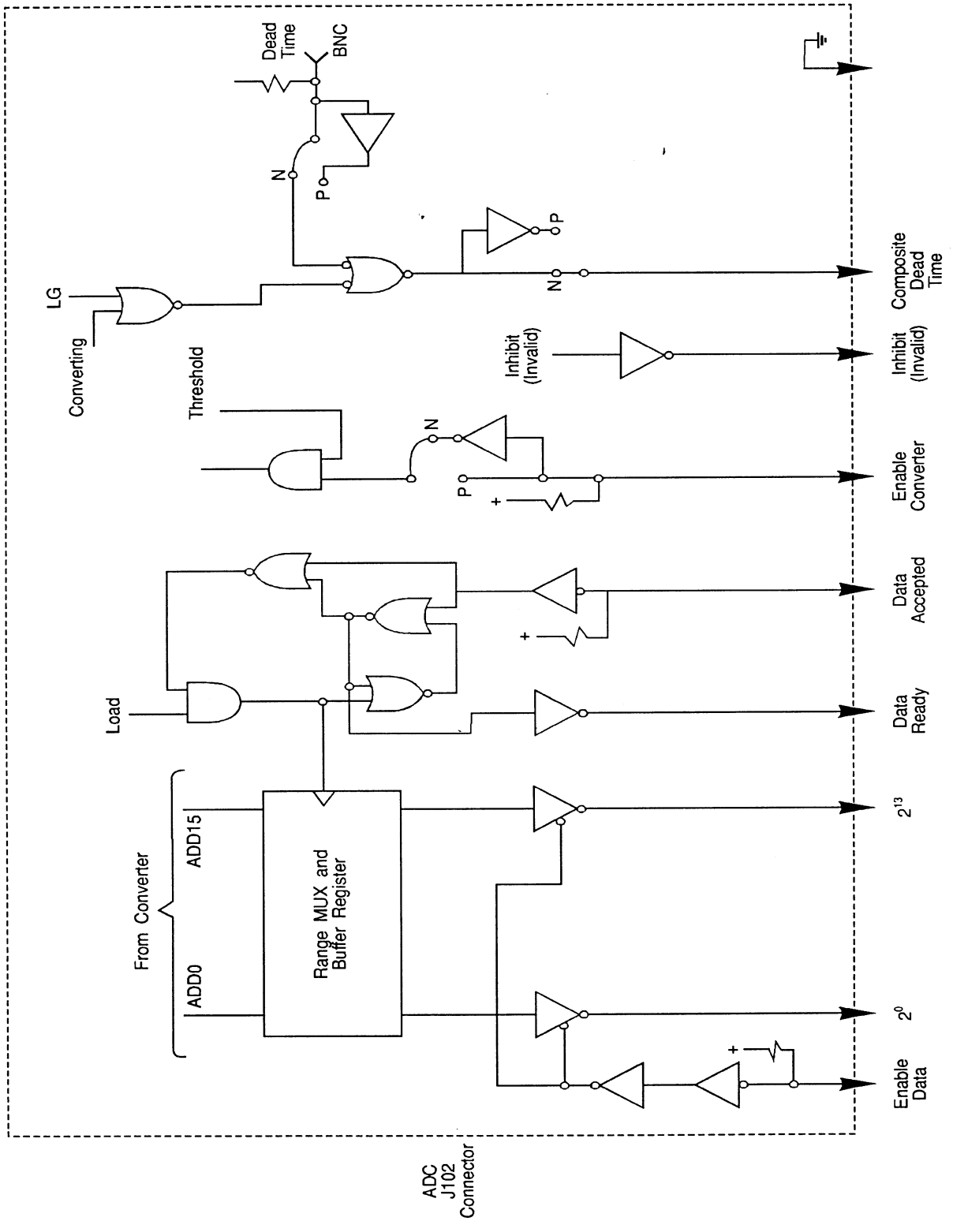

Figure 3.1 Interfacing Logic Block Diagram
(Refer to Schematic B-27133)

4. Theory of Operation

In this chapter, all negative true signals are shown with a trailing asterisk (DUMP*); all other signals are positive true. Each section of the Theory of Operation includes the relevant schematic sheet number after the section title. Two timing diagrams have been included, one for overlap mode and one for non-overlap mode.

4.1 Peak Detector [Sheet 1]

The peak detector circuit is designed to track the input signal to its peak amplitude, detect that the peak has been reached, store the peak amplitude and inform the control logic that an input event has been captured. The input is buffered by U53 and presented to the positive input of U54, if the linear gate is open, LGC* high. During the positive transition of the input, U54 supplies current through CR3 pin 3 to charge the storage capacitor, C16. When the peak of the input pulse has been reached, CR3 stops conducting current and charging C16; C16 now holds the peak value of the input pulse.

U41 is a unity gain buffer which provides current isolation between the storage capacitor and the circuit output connections. One of these connections is the peak detector comparator U32. U32 compares the voltage stored on the holding capacitor with the buffered input pulse. When the input pulse is lower in amplitude than the stored voltage the output of U32, PHD*, switches low.

PHD*, Peak Detect, informs the control logic that an input has been captured. The control logic now closes the linear gate by switching LGC* low.

After the converter has digitized the stored voltage, the storage capacitor is rapidly discharged when the control logic sets the DUMP* signal low. The linear gate is reopened immediately following the DUMP* pulse.

4.2 SCA [Sheet 1]

The input signal is compared to three separate reference voltages prior to the conversion cycle. These are the LLD, ULD and threshold settings. The threshold tracks the LLD setting up to 500 mV. The output of U53 is compared to the threshold voltage by U45. When an input crosses the threshold, THD* will switch low. The output of the peak detector circuit, VC, is compared to the LLD and ULD setting by U30 and U31 respectively. If the stored voltage is higher than the LLD and lower than the ULD then ULD* will be high and the input will be considered valid for conversion.

4.3 Sliding Scale [Sheet 2]

The sliding scale circuit is used to improve the differential non-linearity of the ADC. The sliding scale circuit averages variations in the channel width over 256 channels.

U33 and U48 make up a random number generator. The output of this generator is presented to a DAC, U20. The output of the DAC modifies the amplitude of the signal presented to the converter for processing by subtracting small analog values. In this way, the same input amplitude will produce different results from the converter. This variation is corrected for by adding the random number to the result of the converter. This is done by U22, U35, U42, and U50 on Sheet 3.

4.4 Analog to Digital Converter [Sheet 2]

U19 is the Analog to Digital Converter. It is controlled by inputs TRIG*, LOAD* and Gain Control. The TRIG* signal starts the conversion process. When the conversion is complete, EOC*, (End of Conversion) is set low by U19. The control logic recognizes the EOC*, and, if there are no previous conversion waiting for MCA service, sets the LOAD* signal low to enable the output of U19. The Gain Control input is controlled by the VGAIN input on J102 pin 30 which is generated by the 8233 Digital Stabilizer. The Gain Control input will change the gain of the ADC by ±3% for a ±5 volt input on VGAIN.

4.5 Conversion Gain Control [Sheet 3]

The Conversion Gain setting of the front panel rotary switch is encoded into a 3-bit code (CG0-2*) by the Input PAL, U18, on sheet 4. This 3-bit code is presented to the Conversion Gain Mux PALs U21, U34 and U49. The Conversion Gain Muxes latch the data from the ADC after the random number has been subtracted and perform a shift right of that data. The magnitude of the shift is determined by the Conversion Gain setting. Because the ADC has a fixed conversion time it is always allowed to convert to its full range regardless of the Conversion Gain setting. By shifting the data right the MSB from the ADC is aligned with the MSB associated with the Conversion Gain setting. As an example, for 16K Gain, a shift of one bit is performed therefore the input ADD15 would drive the output MX14. 8k Gain would result in a shift of 2 bits, 4K 3 bits and so on.

The Mux PALs also latch the data from the ADC. This is controlled by the LOAD* signal. The data is latched in order to allow the ADC to convert a second pulse when configured in the Overlap mode, W6 in the A position.

4.6 Digital Offset

The Digital Offset is subtracted from the Gain corrected data by adders U23 and U36. When one of the digital offset switches on the front panel is on, the corresponding signal (DOXXX*) will be low. A twos complement addition is performed which subtracts the digital offset value from the output of the Conversion Gain Muxes.

4.7 Range Control

The Range PAL, U9, tests the corrected data from the Conversion Gain Muxes (Q0-Q7) and the Digital Offset adders (Q8-Q15) for an over- or under-range condition. Over-range is defined as the condition where the data exceeds the Range setting of the front panel rotary switch. Under-range occurs when the data is less than zero. This can happen when the input fails to exceed the digital offset value, the sliding scale causes a negative value, or the input fails to exceed the Zero Baseline setting. Q15 is used as a sign bit for the data, if this bit is high then the data is negative and considered under-range. Both under- and over-range conditions are indicated by the OFLO* signal being set low.

4.8 Control Logic [Sheet 4]

The Control Logic is made up of three PALs: the Input PAL, U18; the Output PAL, U5; and the State Machine PAL, U10.

The Input PAL collects inputs from the front panel switches, the GATE BNC and the peak detector. It generates two signals for the State Machine: Peak Detected (PHDX*) and

GATEX*. Three additional outputs, CCG0-2*, are used by the Gain Control Logic (see "Conversion Gain Control" on page 13).

The Output PAL provides the signals required to interface the ADC to an MCA and amplifiers equipped with LTC/PUR.

The State Machine PAL is the heart of the control logic. There are six possible states plus an initialization state which sets all the outputs off. The remaining states are Linear Gate (STL), Peak Detection (STP), Wait (STW), Converter Busy (STC), Dump (STD), and Data Gating (STG). Please refer to the timing diagrams for the sequence of these states. The State Machine PAL generates the signals that control the Peak Detector and Linear Gate (THEN*, DUMP*, LGC*), the ADC Module (TRIG*, LOAD*) and the transfer of data from the ADC module to the output buffers, U15 and U16 on Sheet 3 (LOAD*).

The State Machine is driven by the 10 MHz oscillator, Y1, and controlled by an internally generated signal, Input Condition Met (ICM*). ICM informs the State Machine when the status of the ADC is correct to allow continuation to the next state. For example, when the State Machine is in the Linear Gate State, ICM* will remain false until an input has crossed the threshold (THD* low) for a PHA mode of operation. ICM also triggers the one-shot U2B which generates a delay (DLY*) time period of 0.5 µs.

4.9 Dead Time Display [Sheet 3 and Schematic B-27427]

U3 and U4 (Board 2) are integrated circuits that sense analog voltage levels and drive the two 10-segment bar graphs U1 and U2 (Board 2), providing a linear analog display of the ADC dead time. The analog voltage is integrated from the ADC dead time signal DISP by R76 and C31. R1 (Board 2) sets the reference voltage for U3 and U4 so that 100% dead time causes all 20 segments to be lit.

4.10 Power Supplies [Sheet 5]

VR2 and VR3 are 3-terminal regulators that supply the –15 V and +15 V supplies from the –24 V and +24 V NIM supplies. VR1 is a simple switcher step-down Regulator which supplies +5 V from the +12 V NIM supply.

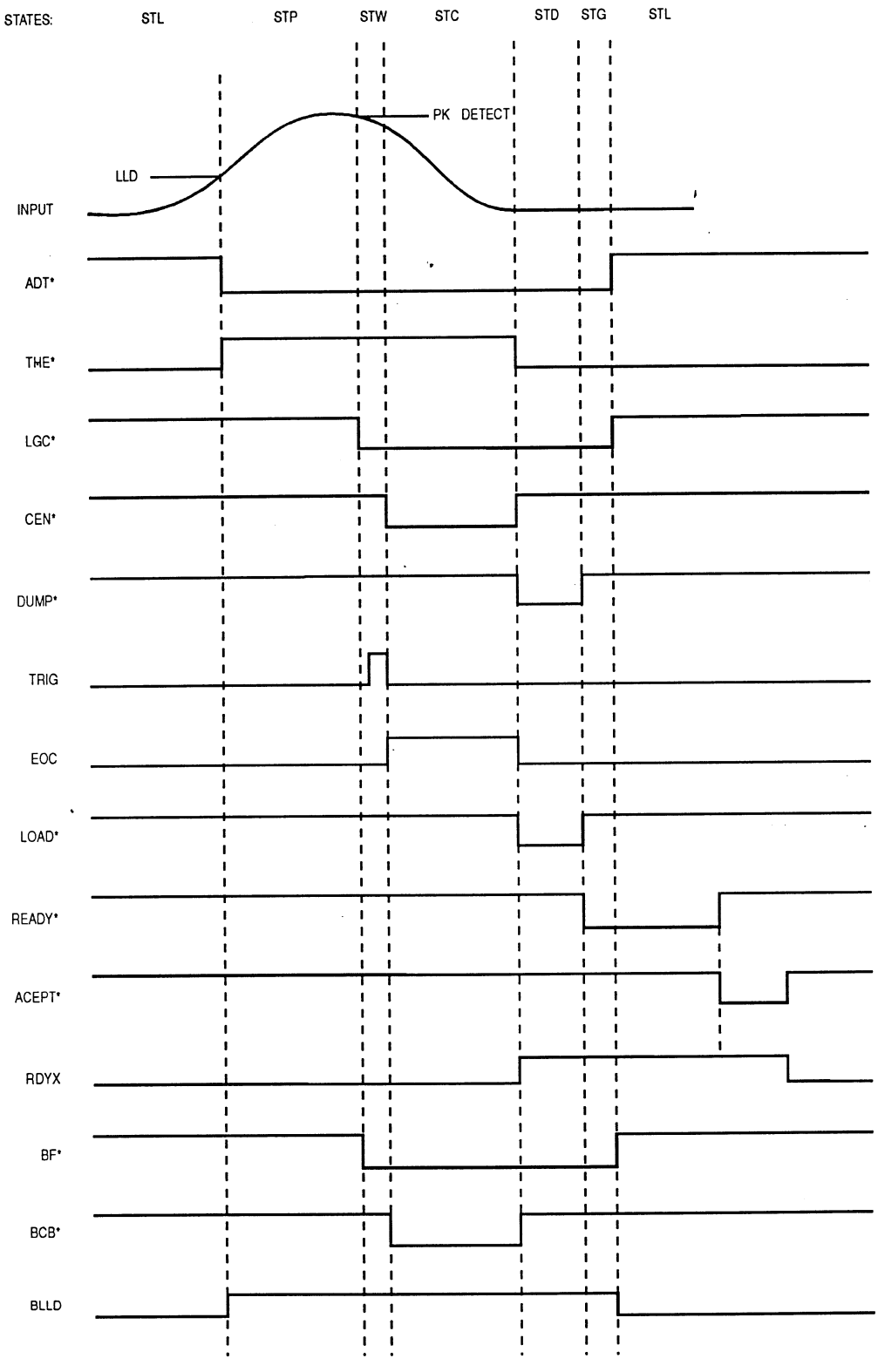

Figure 4.1 8713 Overlap Mode Timing

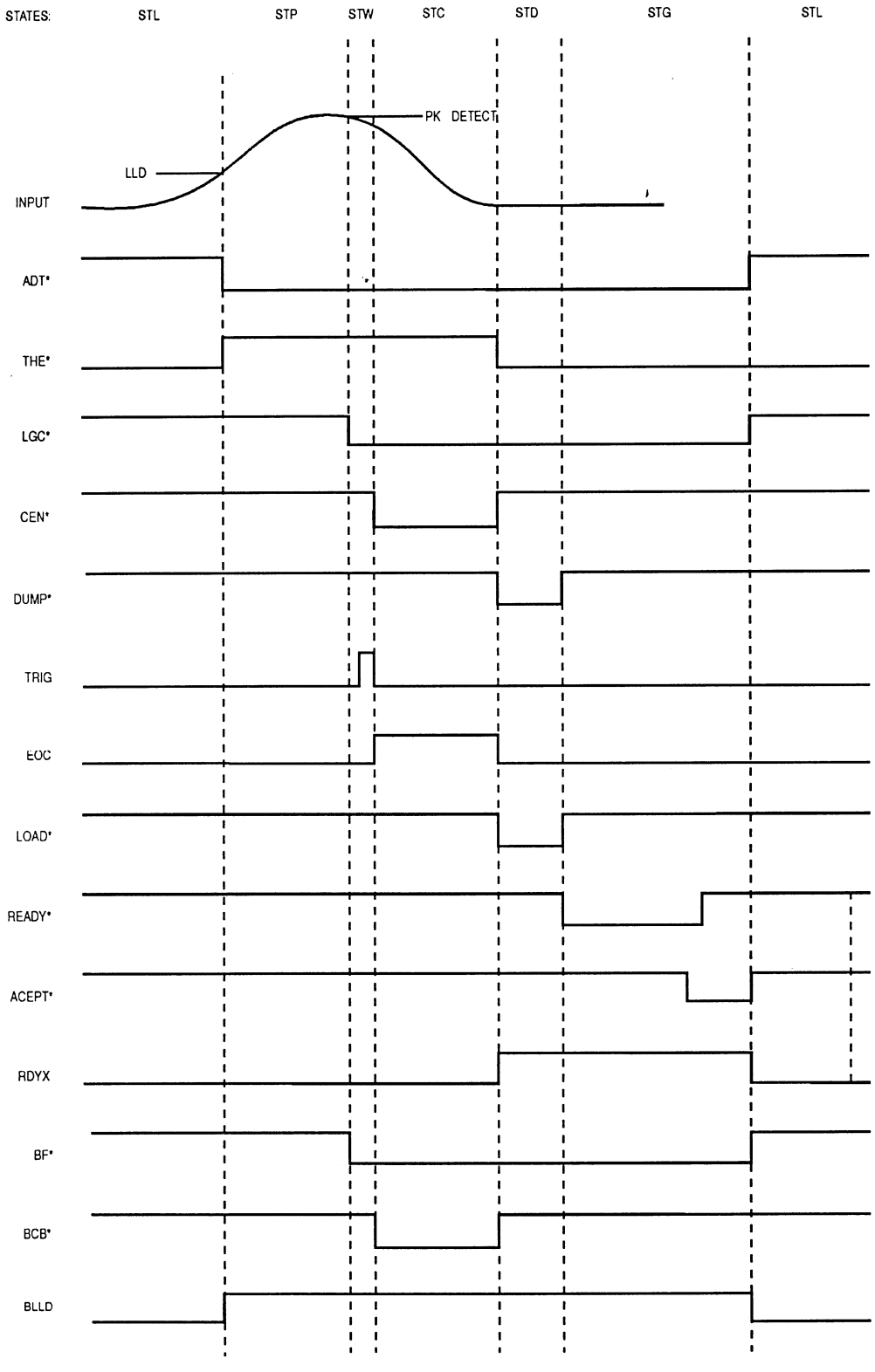

Figure 4.2 8713 Non-Overlap Mode Timing

A. Specifications

A.1 Inputs

ADC IN - Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for the SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 µs maximum; width 0.5 µs minimum; Z_{in} = 1 kΩ, direct coupled; front panel BNC and test point.

GATE IN - Accepts a positive logic pulse or dc level; high amplitude ≥+2.5, Low amplitude ≤400 mV, 0 to +7 V maximum; dc coupled; Loading with COINCidence selected is 1 kΩ to +5 V and 1 kΩ to 0 V for ANTIcoincidence; width ≥250 ns; PHA analysis does not require a gate input; minimum gate pulse width for SVA is 1 µs.

DEAD TIME - Rear panel BNC connector which receives an external dead time INPUT. Accepts a negative or positive logic signal, jumper selectable, which is ORed with the ADC dead time; negative true amplitude ≤400 mV, positive true amplitude ≥+2.5 V, 0 to +7 V maximum; loading 2.2 kΩ to +5 V. The composite dead time signal may be accessed through pin 6 of the rear panel DATA connector. Internal jumper plug selects the output composite dead time signal polarity, positive true or negative true; shipped in the NEG position; TTL compatible.

A.2 Outputs

DATA - Provides 14 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 34-pin ribbon cable connector. Data lines are negative true. Two input lines are also provided for the Model 8233 Digital Stabilizer correction voltages. Stabilizer Control range; zero: ±3%, gain: ±3%.

PILEUP REJECTOR/LIVE TIME CORRECTOR - Accepts Reject and Live Time signals from Canberra amplifiers equipped with PUR/LTC. It also provides Linear Gate to those units for full interactive operation; rear panel 3-pin Molex connector for use with Model C1514 PUR/LTC interface cable.

REJect - Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur during the ADC Linear Gate (LG) signal time; amplitude ≥ 2.5, 0 to 7 V maximum; width ≥100 ns; loading 1 kΩ to 0 V. Accessible through pin 2 of the rear panel PUR connector.

LG - Provides a negative true logic signal; logic low while the ADC acquires an input pulse, returns to a logic high at the pulse acquisition conclusion. TTL compatible output, 47 Ω series resistor. Accessible through pin 1 of the rear panel PUR connector. The LG signal may be viewed on the front panel INSPect test point, positive true, series 33 Ω resistor.

A.3 Front Panel Controls

GAIN - Seven-position rotary switch to select full scale resolution of the input signal; selection of 256, 512, 1024, 2048, 4096, 8192, or 16 384 channels for a 10 V input pulse or level.

RANGE - Seven-position rotary switch to select 256, 512, 1024, 2048, 4096, 8192, or 16 384 channels as the upper output address limit.

OFFSET - Six toggle switches to digitally offset the spectrum to the left; subtracts 0 to 16 128 channels in binary multiples of 256 channels.

LLD - Screwdriver-adjusted multi-turn potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range 0 to +10 V dc.

ULD - Screwdriver-adjusted multi-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range 0 to +10.5 V dc.

ZERO - Screwdriver-adjusted multi-turn potentiometer sets the input analog zero level; adjustment range ±3% of the ADC full scale range.

PEAK DETECT - Toggle switch to select either AUTOmatic or DELAYED initiation of conversion cycle. In AUTOmatic mode, an internal peak detector operates on the input pulse. In DELAYED mode, the conversion begins after a user selectable delay, initiated by the input signal rising through the LLD setting. An ADJustment potentiometer permits selection of a delay from 2 to 100 µs. An INSPect test point is provided to monitor the Linear Gate time delay adjustment, positive true, series 33 Ω resistor.

COINC/ANTI - Toggle switch to select either the COINCidence or the ANTIcoincidence gating mode. In the COINCidence mode (ANTIcoincidence) a positive GATE pulse enables (disables) the conversion of the present input. If gating is used, the pulse must be present during the Linear Gate time as monitored on the INSPect test point.

PHA/SVA - Toggle switch to select the Pulse Height or Sample Voltage Analysis mode. In PHA, the conversion cycle is initiated by the INPUT pulse. In SVA, the conversion cycle is initiated by a GATE pulse. In either mode, the LLD and ULD acceptance criteria apply. The GATE pulse must be positive in COINC mode or inverted in ANTI mode.

A.4 Indicators

DEAD TIME - 20 segment LED indicator displays the average dead time of the converter.

A.5 Performance

INTEGRAL NONLINEARITY - <±0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY - <±0.9% over the top 99.5% of range including effects from integral nonlinearity.

GAIN DRIFT - <±0.005% of full scale/°C

ZERO DRIFT - <±0.005% of full scale/°C

LONG TERM DRIFT - <±0.005% of full scale/24 hours at a constant temperature.

PEAK SHIFT - <±0.025 of full scale at rates up to 100 kHz.

ADC DEAD TIME - Linear Gate Time + 5.9 µs

CHANNEL PROFILE - Typically flat over 90% of channel width when strapped for 6 volt power supply operation and using a 2100 or equivalent NIM Bin. Typically flat over 60% of channel width when strapped for 12 volt power supply operation. For internal power supply strapping, please refer to the description of jumper plug W14 in Figure 2.3, "Internal Controls".

A.6 Power Requirements

+24 V - 110 mA	+12 V - 280 mA or
–24 V - 140 mA	+ 6 V - 510 mA

A.7 Physical

SIZE - Standard single width NIM module 3.42 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-00457T

NET WEIGHT - 1.04 kg (2.3 lb)

SHIPPING WEIGHT - 2.1 kg (4.6 lb)

A.8 Cables

Cable not supplied; MCA must support 34-pin ADC Standard. Consult factory if required.

B. Rear Panel Connectors

This chapter lists the details of the ADC's rear panel interface and power connectors.

B.1 Data Interface Connnector

This 34-pin ribbon conector (J102) provides all the necessay signals for connection to the MCA. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	CDT* or CDT
7	GND	8	ENC* or ENC
9	GND	10	READY*
11	GND	12	INB* (INV*)
13	ADC13*	14	ADC00*
15	ADC07*	16	ADC01*
17	ADC08*	18	ADC02*
19	ADC09*	20	ADC03*
21	ADC10*	22	ADC04*
23	ADC11*	24	ADC05*
25	ADC12*	26	ADC06*
27	Reserved	28	Reserved
29	BF*	30	VGAIN
31	BLLD	32	VZERO
33	BCB*	34	ADC 13X*

Interface Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

SIGNAL	PIN	DESCRIPTION
ADC00*	14	OUTPUT: Binary data 2^0 (LSB)
ADC01*	16	OUTPUT: Binary data 2^1
ADC02*	18	OUTPUT: Binary data 2^2
ADC03*	20	OUTPUT: Binary data 2^3
ADC04*	22	OUTPUT: Binary data 2^4
ADC05*	24	OUTPUT: Binary data 2^5
ADC06*	26	OUTPUT: Binary data 2^6
ADC07*	15	OUTPUT: Binary data 2^7
ADC08*	17	OUTPUT: Binary data 2^8
ADC09*	19	OUTPUT: Binary data 2^9
ADC10*	21	OUTPUT: Binary data 2^{10}
ADC11*	23	OUTPUT: Binary data 2^{11}
ADC12*	25	OUTPUT: Binary data 2^{12}
ADC13*	13	OUTPUT: Binary data 2^{13} (MSB)
ADC13X*	34	OUTPUT: Binar data 2^{13} (Alternate MSB)
ENDATA*	4	INPUT (Enable Data): Used to enable the tri-state buffers driving the 14-bits of data onto the output lines ADC00* through ADC13*.
READY*	10	OUTPUT (Data Ready): Indicates that data is available for transfer to the MCA. READY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	INPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may reset when READY* resets (handshake).
INB*	12	OUTPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer must be completed, the data itself should be discarded by the MCA.
ENC* or ENC	8	INPUT (Enable Convertor): This signal enables or disables the ADC module. A jumper option (W3) allows selection of polarity. ENC = logic 1 enables ADC operation. ENC = logic 0 prevents the ADC from reopening the linear gate thereby inhibiting further operation.
CDT* or CDT	6	OUTPUT (Composite Dead Time): This signal indicates the time when the ADC or connected amplifier is busy and cannot accept another input event. It is used to gate the live time clock circuit in the MCA. A jumper option (W8) allows selection of polarity.
BF*	29	OUTPUT: This signal is set true at peak detect time and remains true until the leading edge of ACEPT*. This signal is meaningful in the NON-OVERLAP mode only.

BCB*	33	OUTPUT: This signal is set true at peak detect time and remains true until READY* is set true. It represents the conversion time of the internal ADC.
BLLD	31	OUTPUT: This signal is set true when the input pulse rises above the ADC Threshold level and remains true until the trailing edge of ACEPT*.
VZERO (Analog)	32	INPUT: This analog signal cohtrols the ADC zero and it is normally provided by the spectrum stabilizer. The ZERO shift of the ADC is ±3% for a ±5 volt input signal. A more positive level on this signal causes spectral peaks throughout the spectrum to move downward.
VGAIN (Analog)	30	INPUT: This analog signal controls the ADC gain and is normally provided by the spectrum stabilizer. The GAIN shift of the ADC is ±3% for a ±5 volt input signal. A more positive level on this signal causes spectral peaks at the upper end of the spectrum to move downward (lowers the gain).
GND	1,3,5,7,9,11	DC common for all interface signals.

B.2 LTC/PUR Connector

The PUR/LTC 3-pin Molex connector provides the connection to the spectroscopy amplifier for pulse pileup rejection and accurate live time correction.

SIGNAL	PIN	DESCRIPTION
LG*	1	OUTPUT: This signal is set true when the input pulse rises above the ADC threshold level and remains true until peak detection. An alternate signal (CB*) which is true during the ADC conversion time is optionally available via internal jumper W4. Used for PUR livetime correction in combination with the amplifier. Logic true = 0 to 0.5 volts; logic false = 3 to 5 volts.
REJ	2	INPUT: A positive level on this signal any time during LG* causes the ADC to reject the event in process. Used for PUR in combination with the amplifier. Logic true = 3 to 5 volts Logic false = 0 to 0.5 volts
GND	3	Signal common.

B.3 Dead Time Connector

The Dead Time BNC connector accepts a negative or positive true amplifier busy signal, with polarity selectable via jumper W7. This signal is logically ORed with the ADC busy signal to provide proper livetime correction in the MCA via signal CDT* on the MCA interface connector.

C. Setup Diagrams

These block diagrams are included to help you set up your system.

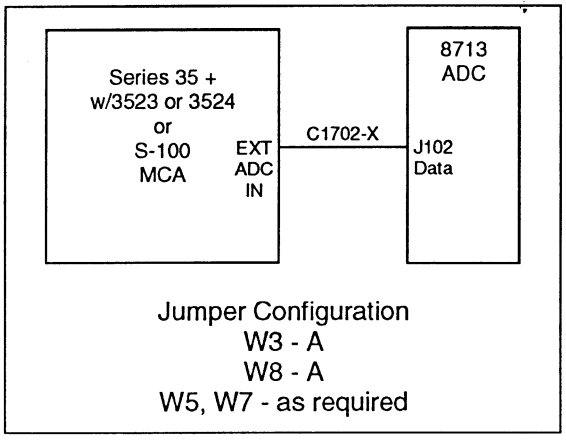

Figure 1

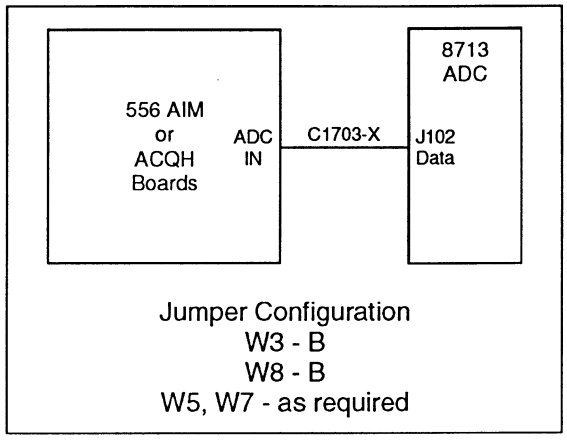

Figure 2

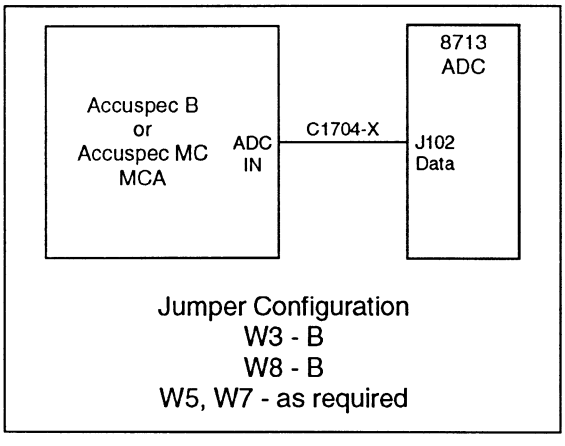

Figure 3

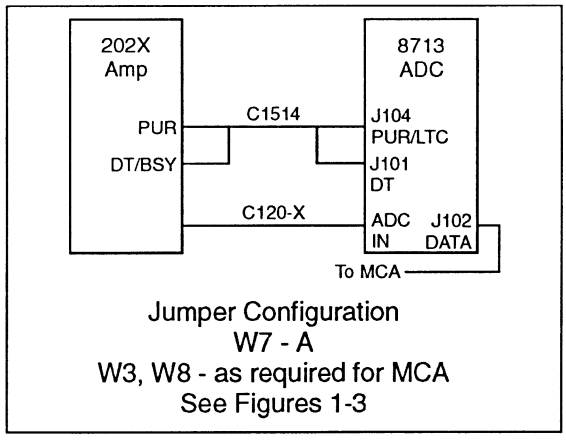

Figure 4

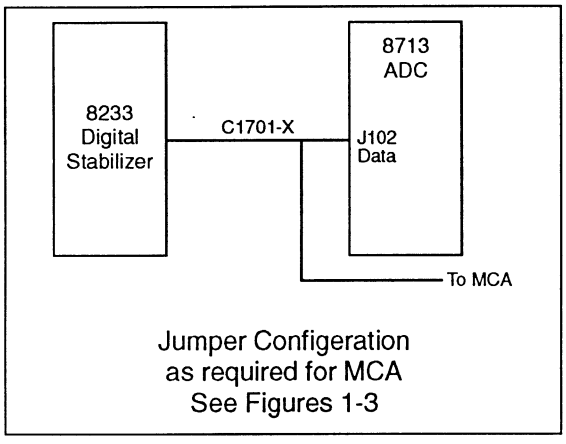

Figure 5

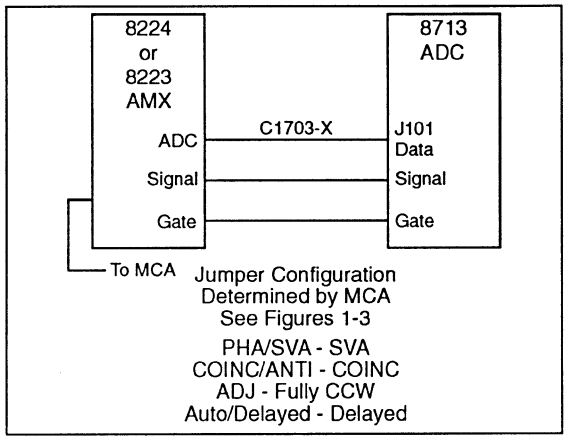

Figure 6

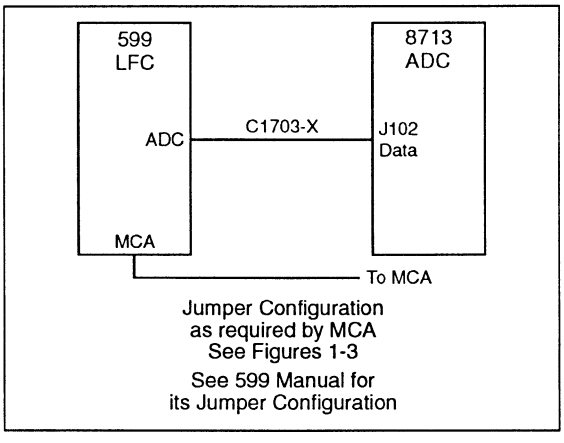

Figure 7

D. Environmental Specifications

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- a rack or tabletop enclosure fully closed on all sides with rear door access
- single point external cable access
- blank panels to cover open front panel Bin area
- compliant grounding and safety precautions for any internal power distribution
- the use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance to the specified EU requirements.

Operating Temperature: 0-50 degrees Centigrade
Operating Humidity: 0-80% Relative, Non-condensing
Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution degree 2

Request for Schematics

Schematics for this unit are available directly from Canberra. Write, call or FAX:

Training and Technical Services Department
Canberra Industries
800 Research Parkway, Meriden, CT 06450
Telephone: (800) 255-6370 or (203) 639-2467
FAX: (203) 235-1347

If you would like a set of schematics for this unit, please provide us with the following information.

Your Name _____

Your Address _____

_____

_____

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_____

Unit's model number _____

Unit's serial number _____

Note: Schematics are provided for information only; if you service or repair or try to service or repair this unit without Canberra's written permission you may void your warranty.