MODEL 2144A

FAST/SLOW COINCIDENCE

INSTRUCTION MANUAL

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Section 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Model 2144A provides in a single width NIM module a high speed multiple input coincidence/anticoincidence analyzer which provides both overlap period and adjustable width coincidence logic outputs for the needs of sophisticated experiments.

Each of the 5 inputs accepts independently a fast negative NIM current pulse or a slow positive NIM voltage pulse as the logic input without the need for selector switches. Input impedance is 50 ohms for negative inputs, and 1K ohm (selectable internally to 50 ohms) for positive inputs.

Each input is enabled by a toggle switch on the front panel adjacent to the relevant connector for use in coincidence (logical AND), anticoincidence (logical OR), or OFF as desired. It is possible to use up to 4 inputs as veto (anticoincidence) for 1 in vote (coincidence).

The fast coincidence result in the Model 2144A is provided on the front panel as a negative NIM pulse, the period being equal to the duration of the selected coincidence. Both normal OVERLAP and complementary $\overline{\text{OVERLAP}}$ are available simultaneously. The user may recognize that by deMorgan's Theorem, if all inputs are selected for the anticoincidence function (logical OR = $\overline{\text{AND}}$) the logic output is provided properly on the $\overline{\text{OVERLAP}}$ output and its complement on the OVERLAP output.

The shaped outputs may be triggered by either the leading edge or the trailing edge of the overlap period by selecting the ⌐▼⌐ or the ⌐▲⌐ of the fast OVERLAP, respectively. The width of the shaped outputs may be adjusted between 50 nanoseconds and 10 microseconds using a screwdriver-adjust trimming potentiometer. Outputs are provided on the front panel as dual fast negative NIM pulses and dual slow positive NIM pulses. An internal jumper plug may be set to provide a complementary logic output for either or both positive and negative shaped outputs on the lowest BNC connectors.

The circuitry of the Model 2144A is entirely DC coupled, and the front end through the OVERLAP outputs is capable of resolving pulses separated by < 10 nanoseconds. The shaped outputs will be limited by the selected pulse width.

1.2 APPLICATIONS

This unit can be used as a fast five-input overlap coincidence by switching all inputs to COINC. It can also be used as a N-input coincidence/M-input anticoincidence by switching N-inputs to COINC and M-inputs to ANTI (N + M not more than 5). The coincidence signal (AND) is at the OVERLAP output, and its complement ($\overline{\text{AND}}$) is at the $\overline{\text{OVERLAP}}$ output. The one-shot signals can be derived from either the leading or the trailing edge of the OVERLAP output via the +/- edge switch on the front panel.

The unit can also be used as a five input fan-in (OR) gate, by switching all input to $\overline{\text{ANTI}}$. The OR signal is then at the OVERLAP output, its complement at the $\overline{\text{OVERLAP}}$ output. (This is an illustration of deMorgans Theorem in Boolean Algebra.) Again the one-shot output can be derived from the leading or the trailing edge of the NOR or OVERLAP output. There are more applications, the experimenter is free to use his ingenuity.

Section 2

SPECIFICATIONS

2.1 INPUTS

IN A, IN B, IN C, IN D, IN E

5 independent front panel inputs accept either positive NIM logic levels ($\geq$ +2.0V peak, width $\geq$ 5nsec), or negative NIM logic levels ($\geq$ -0.6V peak, width $\geq$ 2nsec); input rise time 1 nsec to 100 nsec; Z_{in} = 1K ohms, DC coupled, for positive signals (selectable by internal jumper to 50 ohms); Z_{in} = 50 ohms, DC coupled for negative signals.

2.2 OUTPUTS

OVERLAP

Front panel output provides a negative NIM logic pulse of -16mA to external 50 ohm load; rise time $\leq$ 2nsec; width determined by overlap of the selected coincidence events.

$\overline{\text{OVERLAP}}$

Same characteristics as OVERLAP except complementary logic function.

SHAPED OUTPUTS

NEGATIVE

Two independent front panel outputs provide a negative NIM logic pulse of -16mA to an external 50 ohm lead for each coincidence event, rise time <2nsec; width determined by setting of front panel WIDTH control. Lower output selectable by internal jumper for complementary logic function.

POSITIVE

Two independent front panel outputs provide a pulse of +5V nominal for each coincidence event; rise time <10 nsec; Zout = 50 ohms; width determined by setting of front panel WIDTH control. Lower output selectable by internal jumper plug for complementary logic function.

2.3 CONTROLS

COINC/O/ANTI	Front panel toggle switch adjacent to each input connector to select the logic function of that input: COINC for coincidence, O for off, ANTI for anticoincidence.
TRIG	Front panel toggle switch to select the edge of the overlap period from which the shaped outputs are to be triggered.
WIDTH: OVERLAP/VAR1/VAR2	Front panel toggle switch to select the pulse width of the SHAPED OUTPUTS to be the same as OVERLAP, VARiable 50nsec to 1μsec (1), or VARiable 500nsec to 10μsec (2) by means of adjacent 22-turn trimming potentiometer.

2.4 PERFORMANCE

RESOLVING TIME	An input overlap of ≥3 nanoseconds will generate any or all outputs.
PULSE PAIR RESOLUTION	< 10nsec for front panel fast OVERLAP and $\overline{\text{OVERLAP}}$ outputs in any mode; <20nsec for SHAPED OUTPUTS with minimum WIDTH.
COUNT RATE	> 50MHz for fast OVERLAP and $\overline{\text{OVERLAP}}$ outputs; limited by selected width for SHAPED OUTPUTS.
OPERATING TEMPERATURE RANGE	0° to 50°C

2.5 CONNECTORS

All signal connectors are front panel mounted BNC

2.6 POWER REQUIREMENTS

+12 VDC - 85mA	+24 VDC - 0mA
-12 VDC - 485mA*	-24 VDC - 0mA

2.7 PHYSICAL

SIZE	Standard single width NIM module (1.35 x 8.71 inches) (3.43 x 22.13cm) per TID-20893(rev.)
WEIGHT	1.9 lbs. (0.9 kg)

*This power exceeds the normal BIN power allotment of 167mA for a single width module.

Section 3

CONTROLS

3.1 GENERAL

This section describes the functions of the controls in the Model 2144A FAST/SLOW COINCIDENCE. It is recommended that this section be read before proceeding with the operation of the instrument.

3.2 FRONT PANEL CONTROLS

The five COINC/O/ANTI switches allow each input to be used to detect the coincidence or anticoincidence time between events or to disable an input if it is not being used.

The TRIGger switch selects which edge, negative going or positive going, the SHAPED OUTPUTS will be triggered from.

The WIDTH switch determines if the width of the SHAPED OUTPUTS will be that of the OVERLAP output (OVERLAP) or variable in 2 ranges, 50nsec to 1μsec (1) or 500nsec to 10μsec (2) adjusted by the 22-turn VAR control.

3.3 INTERNAL JUMPERS

Jumpers J1 through J5 select the input impedance for each input to 1K ohm or 50 ohms for positive NIM signals. Input impedance is always 50 ohms for negative NIM signals regardless of jumper position.

Jumpers J6 and J7 select normal or complementary logic functions on the lower NEGATIVE and POSITIVE SHAPED OUTPUTS, respectively.

See Figure 3.1 for jumper locations.

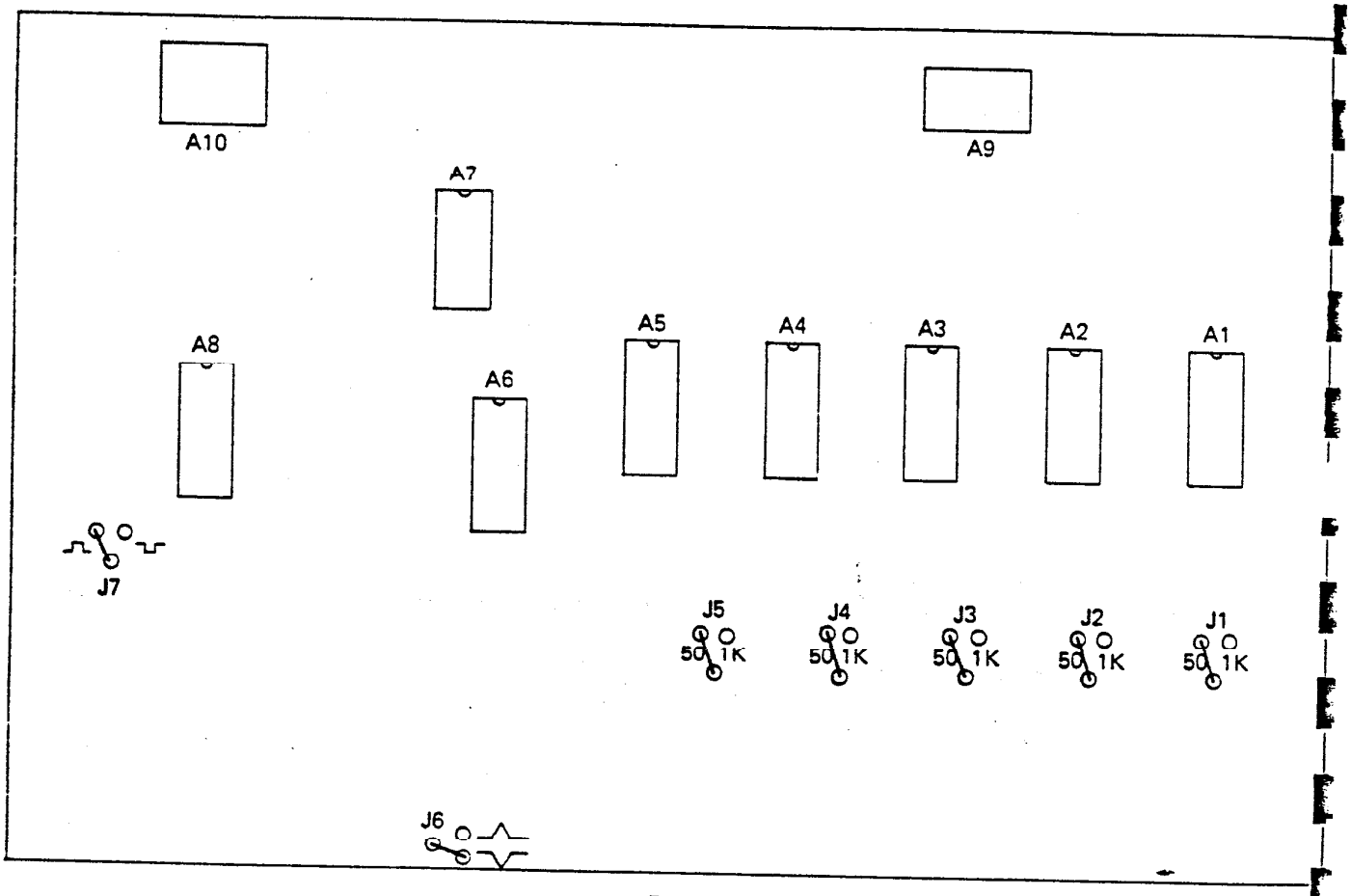


Figure 3-1

Section 4

OPERATING INSTRUCTIONS

4.1 GENERAL

The purpose of this section is to familiarize the user with the MODEL 2144A FAST/SLOW COINCIDENCE, and to check that the unit is operating properly. Since it is difficult to determine the exact system configuration in which the unit will be used, explicit operation instructions cannot be given. However, if the following procedure is carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand.

4.2 TEST EQUIPMENT REQUIRED

A. Pulse Generator (Data Dynamics 5109 or equivalent) known as the "Pulser" in the procedure.

B. Calibrated dual trace oscilloscope with sensitivity of 5nsec/div. or better (Tektronix Model 454 or equivalent), to be identified as the "Scope" in the procedure.

C. Shielded coax cables RG58/U, BNC to BNC, as required in the procedure. Lengths as short as practicable.

D. 50Ω terminators as required in the procedure.

E. BNC TEE's as required in the procedure.

F. NIM Bin to be identified as the "Bin" in the procedure.

4.3 PROCEDURE

A. INITIAL SETUP

1. Scope and Pulser should be on and warmed up.

2. Prepare the unit under test as follows:

   a. Set all front panel COINC/ANTI switches to the "0" position

   b. Set TRIG switch to the ⌐‾¬ position.

   c. Set the WIDTH switch to the OVERLAP position.

3. Set the Pulser controls as follows:

RATE	1 KHz
RATE VERNIER	CW
PULSE WIDTH	1μsec
FUNCTION	NORM
MODE	SINGLE
+ OUTPUT Z	50Ω
- OUTPUT Z	50Ω

4. Set the Scope controls as follows:

CH 1	1V/div., DC coupled
MODE	CH 1
TIME/DIV	0.5μsec/div.
SOURCE	EXTernal trigger
COUPLING	DC
SLOPE	+

B. INPUT CIRCUIT CHECK

1. Connect an RG-58/U cable to the left hand + OUTPUT on the Pulser. Connect the other end of the cable through a TEE with a 50Ω terminator to the Scope CH 1 INPUT.

2. Adjust the Pulser controls for a +2.5V signal with a pulse width of 1μsec.

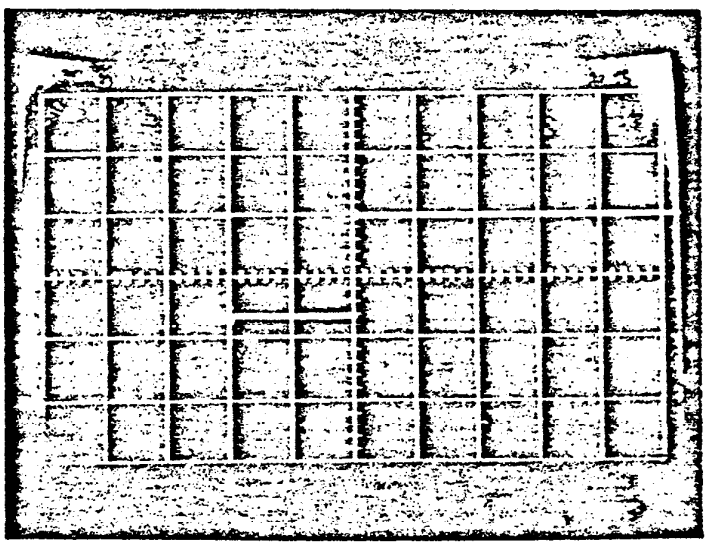
3. Leaving the TEE and terminator at the Scope CH 1 INPUT, move the cable from the TEE to the IN A BNC on the front panel of the 2144A.

B. CIRCUIT CHECK (cont.)

4. Connect an RG-58/U cable from the front panel OVERLAP BNC of the 2144A to the TEE at the Scope CH 1 INPUT. Set the Scope CH 1 vertical range to .5V/div.

5. Connect an RG-58/U cable from the front panel $\overline{\text{OVERLAP}}$ BNC to the Scope CH 2 INPUT through a TEE and 50 Ω terminator at the Scope end. Set the Scope CH 2 vertical range to .5V/div.

6. Put the IN A COINC/O/ANTI switch to the COINC position and verify the Scope CH 1 trace presents a negative NIM current pulse whose amplitude is -800mV ± 100mV. (The signal should switch from 0V.) The pulse width should be 1μsec ± .1μsec. A typical OVERLAP output is shown below.



7. Put the IN A COINC/O/ANTI switch back to the O position and move the cable connected to the Pulser OUTPUT from the IN A BNC to the IN B BNC on the 2144A.

8. Put the IN B COINC/O/ANTI switch to the COINC position and verify the same signals appears on the Scope CH 1 trace with the same specifications.

B. INPUT CIRCUIT CHECK (cont.)

9. Repeat Steps 7 and 8 for all IN BNC's.

NOTE: An output will not be observed unless all the unused IN switches are in the O position.

10. Put the IN E COINC/O/ANTI switch to the ANTI position and the Scope MODE switch to the CH 2 position and verify the same negative NIM current signal appears on the CH 2 trace.

11. Disconnect the cable connected to the OVERLAP BNC on the 2144A from the TEE at the Scope CH 1 INPUT.

12. Move the cable connected to the Pulser left hand + OUTPUT from the IN E BNC on the 2144A to the TEE at the Scope CH 1 INPUT. Set the IN E COINC/O/ANTI switch back to the O position and the Scope MODE switch to the CH 1 position.

13. Move the same cable from the Pulser left hand + OUTPUT to the right hand - OUTPUT.

14. Use the Scope POSITION controls and the PULSER controls to adjust for a CH 1 signal of -1V with a pulse width of 1μsec at the -500mV level. (See previous photo for reference.)

15. Disconnect the cable from the TEE at the Scope CH 1 INPUT and reconnect it to the IN A BNC on the 2144A.

16. Reconnect the cable at the OVERLAP BNC of the 2144A to the TEE at the Scope CH 1 INPUT.

17. Put the IN A COINC/O/ANTI switch to the COINC position and verify the same negative current signals appears on the Scope CH 1 trace with the same specifications.

C. SHAPED OUTPUTS

1. Move the cable from the OVERLAP BNC on the 2144A to the upper ⎍ BNC on the 2144A.

2. Put the Scope CH 1 vertical range to 1V/div.

C. SHAPED OUTPUTS (cont.)

3. Put the WIDTH switch on the 2144A to position 2 and verify a positive signal of 2.5V ± 0.25V appears on the CH 1 trace. Remove the 50Ω terminator at the Scope CH 1 input and verify the signal goes to 5V ±0.4V. Reinstall the 50Ω terminator. Put the TRIG switch on the 2144A to the ⌐‾ position and verify the leading edge of the displayed signals shifts 1μsec to the right (the same distance as the input pulse width). Put the TRIG switch back to the ‾⌐ position.

D. OUTPUT PULSE WIDTH CHECK

1. With the Pulser connected to the IN A BNC and the COINC/O/ANTI switch in the COINC position, put the scope time base to .1μsec/div. Adjust the front panel WIDTH control on the 2144A (screwdriver adjust) full CCW and verify the pulse width of the signal on the Scope CH 1 trace to be ≤ 500nsec.

2. Put the Scope Time Base to 2μsec/div. Adjust Pulser RATE VERNIER control for at least 15μsec between the first two displayed pulses. Adjust the WIDTH control pot full CW and verify the signal pulse width to be ≥ 10μsec.

3. Move the cable connected to the TEE at the Scope CH 1 INPUT from the upper ⌐‾⌐ BNC to the upper ⌐‾ BNC on the 2144A. Put the WIDTH switch to position 1.

4. Put the Scope CH 1 vertical range to .5V/div. and set the Scope time base to .5μsec/div. Verify the signal on the CH 1 trace to be -800mV ± 100mV with a pulse width ≥ 1μsec.

5. Adjust the WIDTH control pot to full CCW on the 2144A and set the Scope time base to .05μsec/div. Verify the signal on the Scope CH 1 trace to have a pulse width of ≤ 50nsec.

E. AUXILIARY OUTPUT CHECK

1. Move the cable from the upper ⌐‾ BNC on the 2144A to the lower ⌐‾ BNC and verify the same signal appears on the Scope CH 1 trace as in Step F5.

2. Move the cable from the lower ⌐‾ BNC on the 2144A to the lower ⌐‾⌐ BNC. Put the Scope CH 1 vertical range to 1V/div. and verify the ⌐‾⌐ signal is on the Scope CH 1 trace.

E. AUXILIARY OUTPUT CHECK (cont.)

4. Internal jumpers are provided to change the lower  and lower  outputs to the complement. See Figure 3.1 for jumper locations.

Section 5

THEORY OF OPERATION

5.1 GENERAL

The Model 2144A FAST/SLOW COINCIDENCE accepts the NIM standard logic pulses in either the positive voltage or negative current forms, and executes the logical AND function to generate output signal pulses which may represent the duration of the selected coincidence function, and/or the simple presence of such a selected coincidence. The circuitry consists of 3 sections: input circuits for each of the 5 inputs, the fast coincidence circuitry, and the shaped output circuitry.

5.2 INPUT CIRCUITS

Each of the 5 inputs consists of a discrete transistor pulse sorter and a coincidence/anticoincidence steering gate.

Negative NIM current pulse input signals are received through a 47 ohm series resistor into the emitter of a common base switching transistor. This device is threshold biased by a diode-connected transistor for a temperature stabilized operating point conducive to the fastest current pulse response. The Schottky diode is used as an antisaturation clamp to enhance recovery of the transistor from an input overdrive and assure minimum time skew of a narrow input pulse.

Positive NIM voltage pulses are received by a conventional inverting transistor switch. To avoid pulse reflections on the positive input caused by a conventional 1K ohm input impedance as driven by some sources of the positive voltage pulse signal which are not source end terminated, the Model 2144A allows the user to set the input impedance for such pulses to either 1K ohm nominal or 50 ohms nominal. Jumpers J1 through J5 implement this simple selection directly.

The transistors used for the negative and positive pulse sorting are biased and driven in a manner that assures virtually no time skew between positive and negative signals. Thus, positive voltage signals may be used in coincidence/anticoincidence with negative current signals accurately.

The sorted signal at the collectors of the transistors is level translated to ECL logic levels and steered through an I.C. gate for proper polarity to serve as a coincidence (logic low) or anticoincidence (logic high) vote pulse to the fast coincidence circuitry. The front panel switch controls only a DC level to enable one gate (by coupling one input to -5V), while disabling the complement (by allowing its input to go to logic high, and thereby cutting off the gate output). In the O position, the switch allows both gates to be driven to output logic low.

5.2 INPUT CIRCUITS (cont.)

For reference, ECL logic high is nominally -0.8V, and logic low is nominally -1.8V.

5.3 FAST COINCIDENCE

Voting inputs are summed for coincidence as logic low pulses at the input to the 5-input $\overline{\text{AND}}$ gate A6b. The ECL complementary logic outputs of this gate represents the duration of coincidence of the selected inputs, and are thus provided to the front panel as OVERLAP and $\overline{\text{OVERLAP}}$ complementing negative NIM current outputs. The output driver is a conventional high speed differential amplifier.

5.4 SHAPED OUTPUTS

The complementary pulse outputs of A6b are also used through the front panel TRIGger selection switch to generate a firing pulse to an adjustable period one-shot and thereby the dual positive voltage and negative current shaped output pulses. A7 selects the appropriate polarity output from A6b to generate a firing pulse on either the leading or trailing edge of the OVERLAP period to initiate the one-shot in A6a. Two VARiable ranges are provided, as well as an override which forces the shaped outputs to be of the same duration as the fast coincidence OVERLAP output.

The positive NIM voltage outputs are derived by level translating the logic low ECL pulse at A6a pin 3 to conventional totem pole TTL-style outputs. The outputs are each source terminated in 50 ohms nominal to prevent ringing and multiple outputs due to transmission line effects within uncontrolled load impedances. A jumper J6 allows the user to select either a normal or complementing output voltage on the lower front panel BNC connector. The negative NIM current outputs are again conventional high speed current steering differential amplifiers. One fixed normal output and one selectable normal/complementing output are provided, the latter governed by the position of jumper J7. In both instances the defined 50 ohm load impedance permits the current output to be optimized for fast edges without source end termination.