Model 2126
Constant Fraction Discriminator

User's Manual

8/93

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FIGURE LISTING

Section 1. Introduction

The Model 2126 is a 200 MHz Constant Fraction Discriminator in a single width NIM. It has independent controls for threshold, walk, output pulse width, and operating mode, and provides maximum flexibility for use in any timing application.

The 2126 is fully dc coupled and provides two count rate operating ranges for use over a wide range of input count rates. In the standard count rate range, the 2126 operates to 150 MHz with the front panel potentiometer controlling both the output width and the internal dead time. Alternatively, a special high count rate range can be selected which provides operation to 200 MHz (typically 250 MHz) with fixed output width and deadtime.

The 50 ohm input of the 2126 accepts negative pulses with amplitudes up to -5 V. Input protection is provided for inputs outside the expected range. An internal jumper can connect a X2 attenuator to the input to extend the input range to -10 V. Three operating modes are provided. In addition to its normal Constant Fraction (CF) timing mode, the 2126 provides a Constant Fraction with Slow Risetime Reject (SR) timing mode and a Leading Edge (LE) mode. A fraction module is provided and set for 0.4; it can easily be changed to another fraction, if desired. An alternate plug-in module allows Leading Edge operation.

Two independent fast negative-timing outputs and two independent positive-timing outputs are provided. This provides maximum flexibility for most timing applications. In addition, an LED is provided to indicate the presence of input signals.

The 2126 can operate from NIM bins with the standard ± 12 V and ± 24 V power supplies. If a ± 6 V power supply is available, the 2126 can be configured to use that supply for much of its power requirements.

Section 2.
Controls, Connectors and Indicators

2.1 FRONT PANEL

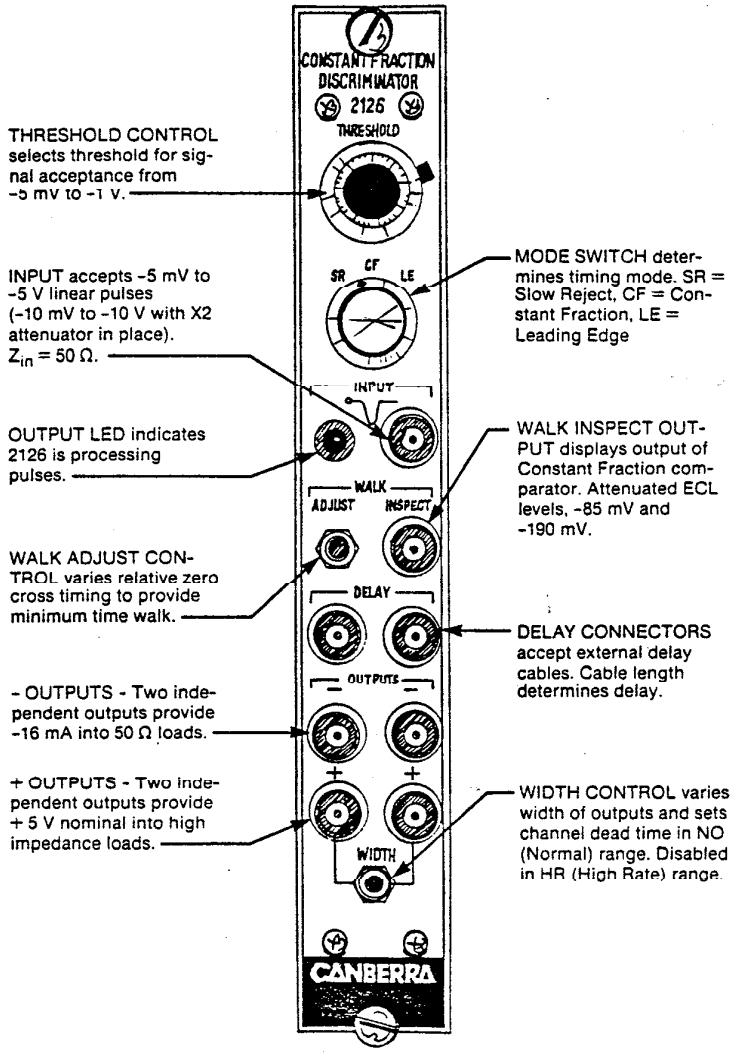

Figure 2.1
Front Panel

Section 3.
Setup Information

This section describes the function of the various jumpers and modules mounted on the printed circuit board of the 2126. Any adjustments should be made prior to installing the 2126 in a NIM bin or connecting the 2126 to a power source. Remove the left cover of the 2126 to expose the circuit board.

3.1 ATTENUATOR MODULE

The 2126 is provided with an input attenuator module. This module provides the choice of no attenuation or X2 attenuation of the input signal. The input range of the 2126 is -5 mV to -5 V. If the peak input signal is expected to be -5 V or less, no attenuation should be selected. For applications where the peak input signal is between -5 V and -10 V, the X2 attentuation should be selected. The attenuator module is a small assembly containing two resistors and a short jumper wire mounted near the front of the 2126 (Figure 3.1). The attenuation factor can be changed by removing the module from the socket, rotating it 180 degrees, and replacing it in the socket. See Figure 3.2 which illustrates the two choices of attenuation provided by the attenuator module. The attenuator module is shipped from the factory in the no attenuation position.

3.2 FRACTION MODULE

In timing experiments, one of the important variables to consider is the fraction of the input signal used to derive the constant fraction function. Most applications provide optimum timing with a fraction of 0.4. This fraction is provided by the 2126. However, the 2126 offers the user an easy means to change the fraction. The fraction module is located immediately below the attenuator module near the front of the 2126. The user can change the desired fraction in two ways. Figure 3.3 illustrates the fraction module and lists values for two resistors that can be changed by the user to implement different values for the fraction. Alternately, contact the factory regarding other values of fraction modules available on special order.

3.3 COUNT RATE RANGE (NOrmal/High Rate)

Two count rate ranges are provided on the 2126. The user can select the desired count rate range by moving a jumper mounted on the circuit board. NOrmal range (NO) is intended for most uses of the 2126. It provides for count rates up to 150 MHz. In the NOrmal range, the front panel WIDTH potentiometer controls the width of the negative and positive timing outputs and the internal deadtime of the 2126.

In certain extremely high rate applications, the user should select the High Rate range (HR). This range provides for usable count rates of greater than 200 MHz. However, certain precautions should be observed in using the HR range of the 2126. In this range, the front panel WIDTH potentiometer is inactive. The width of the negative timing outputs and the internal deadtime of the 2126 channel are internally set at approximately 2 ns. The input signal should be approximately 2 ns in width and show a clean return to the baseline in order to fully utilize the speed of the HR mode of the 2126.

In addition, the user should verify that companion NIM modules used with the 2126 in its HR range are capable of accepting negative NIM inputs of 2 ns width. The NO/HR jumper is located just to the right of A2 on the 2126. See Figure 3.1. NO is the upper position of the jumper. HR is the lower position of the jumper. The 2126 is shipped in the NO position.

3.4 OPERATING MODE (Constant Fraction/Slow Reject/ Leading Edge)

The 2126 provides three operating modes: Constant Fraction (CF), Constant Fraction with Slow Reject (SR), and Leading Edge (LE). See Section 4.3 for a description of these operating modes.

3.4.1 The Constant Fraction Mode

The Constant Fraction (CF) mode is intended for use with detectors such as fast plastic detectors which exhibit fast rise time outputs with little risetime variation. The Constant Fraction with Slow Risetime (SR) mode is often used with Germanium detectors which exhibit a wide range of rise time variation. The Leading Edge mode is used with detectors which provide fast outputs with little amplitude or risetime variation.

3.4.2 Constant Fraction and Constant Fraction with Slow Reject Modes

Both Constant Fraction (CF) and Constant Fraction with Slow Reject (SR) modes use the internal fraction module supplied with the 2126. To use either mode, verify that the fraction module is properly installed in its socket near the front of the 2126 circuit board. Figure 3.3 shows the proper installation of the fraction module. With the fraction module installed, the front panel Mode Switch allows selection of Constant Fraction (CF) mode or Constant Fraction with Slow Reject (SR).

3.4.3 Leading Edge Mode

To select the Leading Edge Mode, the user should remove the fraction module from its socket near the front of the board and replace it with the Leading Edge module. A socket is provided near the bottom of the circuit board to hold the unused module. The front panel Mode Switch should be set to Leading Edge (LE) to use the Leading Edge mode. Figure 3.4 shows the proper installation of the Leading Edge module. Table 3.1 summarizes the module and switch settings for the three operating modes.

Figure 3.1 shows the internal layout of the 2126. The function of the internal controls and their normal configuration is illustrated.

Table 3.1
Operating Mode Summary

Operating Mode	Module	Front Panel Switch
Constant Fraction	Fraction	CF
Constant Fraction with Slow Reject	Fraction	SR
Leading Edge	Leading Edge	LE

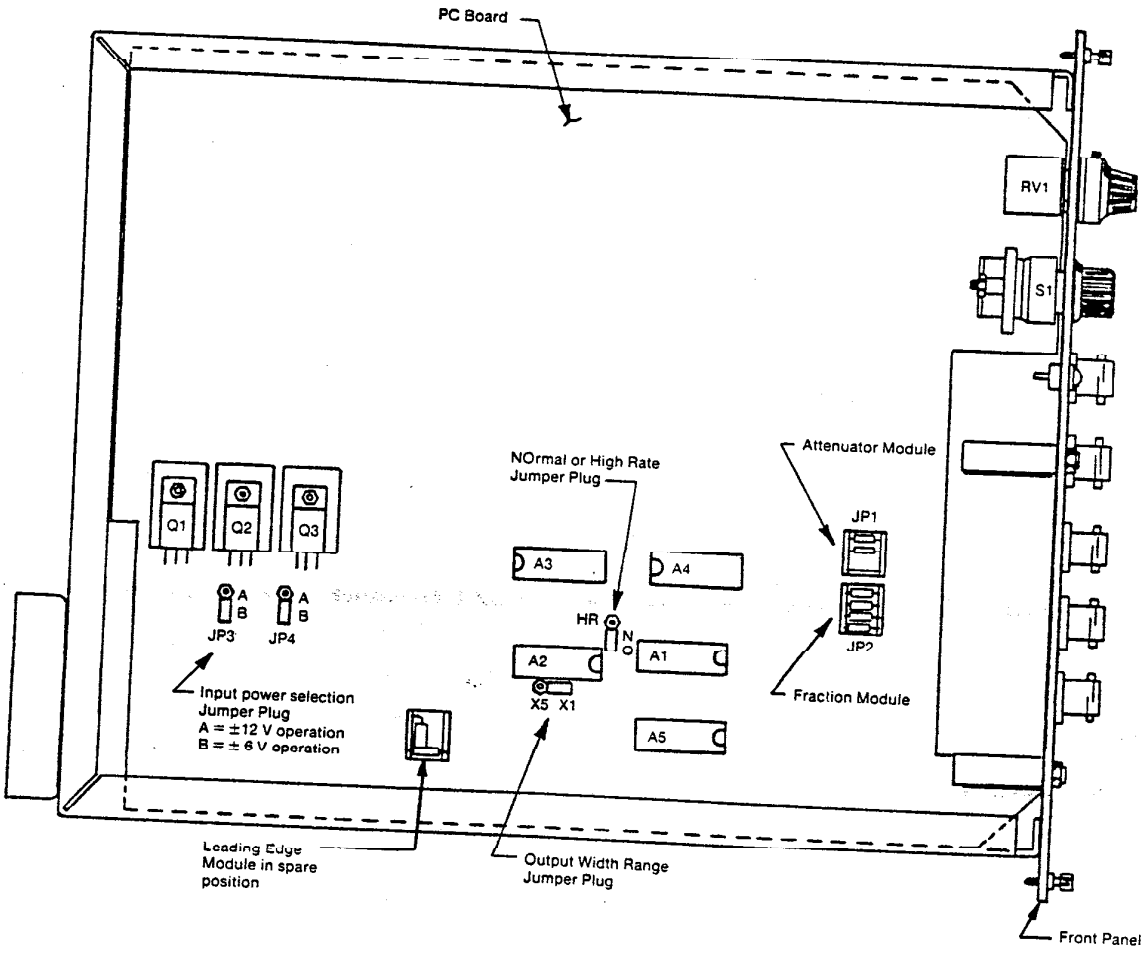

Figure 3.1
Internal Controls

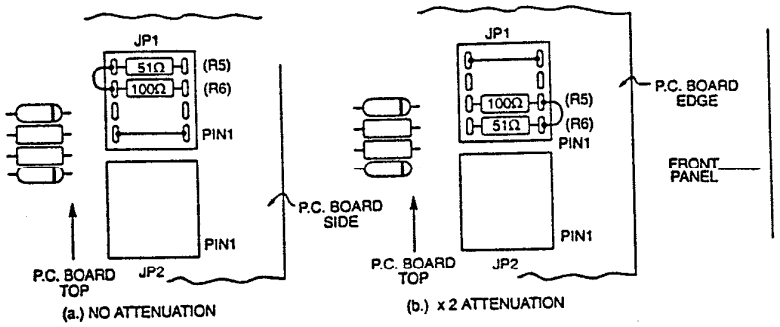

Figure 3.2
Options for Attenuator Module

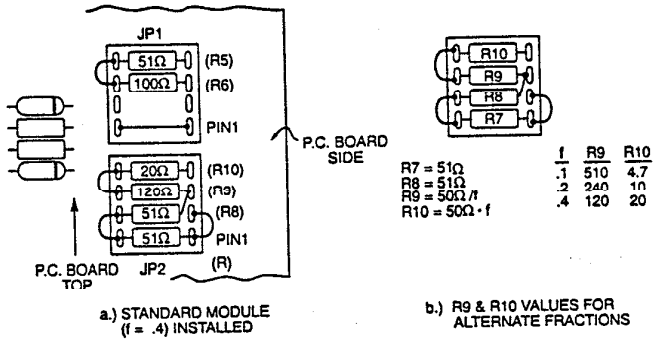

Figure 3.3
Constant Fraction Module, Including Resistor Values for Field Changes

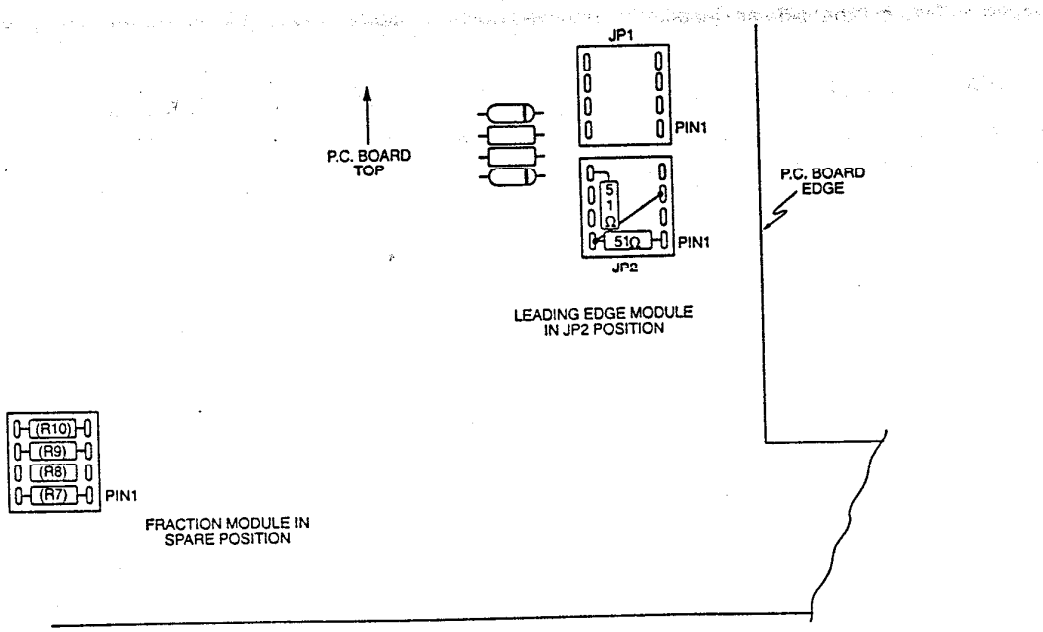

Figure 3.4
Leading Edge Module

3.5 OUTPUT WIDTH RANGE (X1/X5)

Two ranges of adjustment are provided for the front panel WIDTH potentiometer. Since the WIDTH potentiometer controls the output widths as well as the internal deadtime of the 2126, the proper range for the WIDTH adjustment should be selected. Use X1 for fast plastic detectors and most sodium iodide detectors. Detectors that provide input signals of 100 ns width or greater, or that cause baseline perterbations extending longer than 100 ns, should use the X5 range. The X1/X5 jumper is located below A2. See Figure 2.2. X1 is to the right and X5 is to the left. The X1/X5 jumper is shipped in the X1 position.

3.6 STANDARD/ALTERNATE POWER SUPPLIES

The 2126 can operate from NIM bins equipped with the standard ± 12V and + 24 V power supplies as well as those with the optional ± 6 V power supply. Since the 2126 draws current is excess of the single-width NIM module limit when connected to a ± 12 V supply, operation of the 2126 from ± 6 V will reduce the current drawn to within the single-width module limits. If a ± 6 V power supply is available, set the input power jumpers to the 6 V position, otherwise use the 12 V position. See Figure 3.1. The 6 V position for both jumpers is towards the bottom of the module and is labeled "B". The 12 V position is towards the top of the module and is labeled "A".

3.7 STANDARD SETUP

The following can be considered a standard setup and is shipped from the factory in this configuration:

Attenuator module	: X1 (no attenuation)
Fraction module	: Constant Fraction, f = 0.4
Timing range	: NO (NOrmal)
Operating mode	: CF (Constant Fraction)
Output width range	: X1 (2-100 ns)
Power supply	: ±12 V

Section 4. Operation

4.1 POWER SUPPLY

The 2126 is intended to be operated in a NIM bin equipped with a power supply providing ± 12 V and ± 24 V. Alternately, a NIM bin providing ± 12 V, ± 24 V and ± 6 V can be used. See Section 3.6. For lab bench testing, a NIM power supply extension cable may be used. However, excessive voltage drops in the extension cable may be encountered due to the relatively high current requirements of the 2126. For use in experiments, secure installation in a NIM bin is recommended. The NIM bin power supply should be off when the 2126 or other NIM are installed or removed from the NIM bin.

4.2 INPUT SIGNALS

Typical input signals to the 2126 are generated by scintillation detectors utilizing photomultiplier tubes or solid state detectors with a charge sensitive preamp and timing filter amplifier. Such signals are negative, going from a baseline of ground. Rise times can vary from 1 ns to greater than 100 ns, and widths from 1 ns to greater than 500 ns. For laboratory test bench, a logic pulser can be used as an input to the 2126. See Figure 4.1 for a typical input signal produced by a logic pulser.

4.3 OPERATING MODE

Selection of operating mode depends on the requirements of the given experiment. Some general compromises worth considering are discussed in the following paragraphs.

4.3.1 Constant Fraction (CF) Mode

In the Constant Fraction (CF) mode, timing is derived from a comparison between a fixed ratio (40% in the 2126) and the peak amplitude of each successive pulse. This instantaneous self-reference yields a time mark that is theoretically independent of the pulse height, as contrasted to the behavior of the leading edge mode. In the 2126, the ratio reference signal is taken internally, and the full amplitude pulse is delayed for the comparison by an external cable connected between the two front panel DELAY connectors.

When the length of this external cable is chosen to generate a time delay less than the rise time of the input pulse, the resulting time mark is stabilized for both amplitude and rise time variations of that pulse. This is the basis for ARC (Amplitude and Rise time Compensated) timing. The compromise in Constant Fraction (and also ARC) timing is the ability to provide proper delays for the rise time of the input pulse considering either rate and pile-up effects or the distortions introduced by varying wavefront shapes due to charge collection deficit, ballistic effects, or trapping effects in the detector. It is these accommodations that lead to empirical determinations of the optimum delay cable length for a given detector and setup.

4.3.2 Constant Fraction With Slow Reject (SR) Mode

In the Constant Fraction with Slow Rise time reject (SR) mode, a further accommodation is offered for the longer rise times of solid state detectors. The timing mark for the Constant Fraction is derived from the slightly delayed pulse, with the presumption that the THRESHOLD level has been set quite low and this level is exceeded prior to the derivation of the timing mark. In the case of solid state detectors, where long varying wavefronts of the input pulse are common, a relatively short delay cable is frequently used and the above timing premise may not be satisfied. In that case, the amplitude discriminator keyed to the THRESHOLD setting may switch late, and the resulting timing will represent some mix of the intended Constant Fraction timing with Leading Edge timing. This effect causes either tailing or a satellite peak in a time spectrum. In the SR mode, a logic alternation causes rejection of pulses which do not exceed the THRESHOLD prior to the derived Constant Fraction timing mark. The result is enhanced timing resolution due to elimination of the Leading Edge errors, but with some loss of counting efficiency.

4.3.3 Leading Edge (LE) Mode

The Leading Edge mode is used less often than the two Constant Fraction modes. It is typically used for detectors with fast risetimes and little amplitude variation. Since the Constant Fraction function is disabled when the 2126 is used in Leading Edge mode, amplitude and risetime variation can introduce timing walk. If the input signals are all essentially of the same amplitude and risetime, the Leading Edge mode can offer good timing performance.

4.4 DELAY CABLE

The delay cable used to set the Constant Fraction timing mark should provide a delay less than the known rise time of the applied input pulse for full compensation of both amplitude and rise time variations (for a fixed shape). For fast and moderately fast detector pulses (up to 10 ns rise time) a delay of nominally 75% of the rise time is most effective. For solid state detectors, a delay of 40% of the pulse rise time is commonly used for the reasons given above.

The internal delay of the 2126 is 0.3 ns, and this must be corrected by picking a suitable cable. For example, if the detector rise time is 4 ns, a 3 ns delay would be recommended. The external cable length, estimated on the basis of 4.8 ns per meter for RG-58 cable, would be:

$$L = \frac{\text{External Delay}}{4.8} = \frac{\text{Total delay - Internal Delay}}{4.8}$$

$$L = \frac{3.0 - 0.3 \text{ ns}}{4.8 \text{ ns/m}} = 56.3 \text{ cm or about 22 inches}$$

4.5 WALK TRIM

The adjustment of the amplitude sensitive variation of the timing mark (time walk) in the Constant Fraction and CFRR modes remains a less exact procedure. Proper adjustment is possible only when the dc offset present on the input to the 2126 is less than ± 6 mV dc. Thus detector leakage or dark current errors must be minimized before attempting adjustment.

Laboratory trimming of the unit can be demonstrated by using a suitable pulse generator with a known fast, clean wavefront and a delay chosen as discussed above. A very broadband 50 ohm attenuator such as the Hewlett Packard HP-3496, or one whose time walk is very precisely known, should be used. An externally triggered oscilloscope capable of displaying at least 1 ns/division is also necessary. Step attenuations should be then yield a stable time position of the 2126's output signal when starting from a reference -5 V peak pulse input. Care must be taken that the pulse generator offset is small and does not change for different attenuator settings. The WALK ADJUST trimming potentiometer can be used to find the best adjustment of the finite time walk over a narrower amplitude range as desired.

When the 2126 is used with the intended detector, timing resolution may be trimmed experimentally by successive measurements in the setup at hand. A qualitative monitoring is available by monitoring the front panel INSPECT output with an oscilloscope. For fast detectors, the output should indicate an attenuated logic low ECL level (approx. -0.19 V dc, into 50 Ω) where noise just disappears into this level and pulses are seen as transitions to logic high ECL (approx. -0.085 V dc into 50 Ω). Reference Figure 4.2. For slower detectors, a noise band between the ECL levels may be seen, with transitions to ECL logic high and low of about equal intensity. Reference Figure 4.3.

4.6 THRESHOLD ADJUSTMENT

The 2126 threshold adjustment can be used as a lower level control to select the threshold above which input pulses will generate an output signal. A front panel test point is provided to allow easy measurement of the selected threshold voltage. As a general rule of thumb, select a threshold voltage as high as possible while not excluding input signals of interest. Unless experimental conditions dictate otherwise, do not use minimum settings of the threshold, since input signals often show ringing or baseline perterbations which may generate unwanted outputs.

4.7 OUTPUTS AND WIDTH CONTROL

The 2126's negative logic outputs are intended to drive 50 ohm loads through any reasonable length of suitable 50 ohm coaxial cable (such as RG-58). Figure 4.4 shows the typical negative output pulse shapes into 50 ohm loads, with the WIDTH control set to minimum. For optimum performance, terminate unused negative outputs in 50 ohms.

Since the WIDTH control also sets the DEAD TIME following a given pulse in the NOrmal count rate range, the user should set this control consistent with the pulse rate requirements of the given experiment. In the minimum (fully counterclockwise) position of the WIDTH control, a count rate in excess of 150 MHz can be expected for the NOrmal mode of the 2126. The WIDTH control of the 2126 is inoperative in the High Rate mode.

The 2126's positive logic outputs are designed to drive relatively high impedance loads with logic levels of nominally 0 and + 5 V. Since this type of output is inherently slower than current mode outputs (the negative outputs), the positive outputs may not provide proper logic transitions at the high count rates the 2126 is capable of.

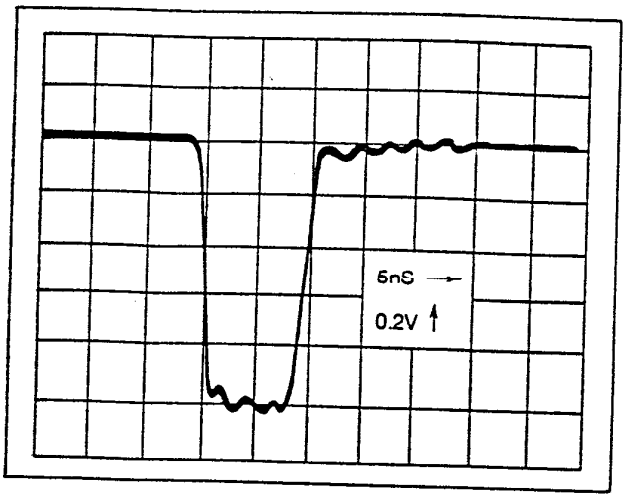

Figure 4.1
Typical Input Signal
Produced by a Logic Pulser

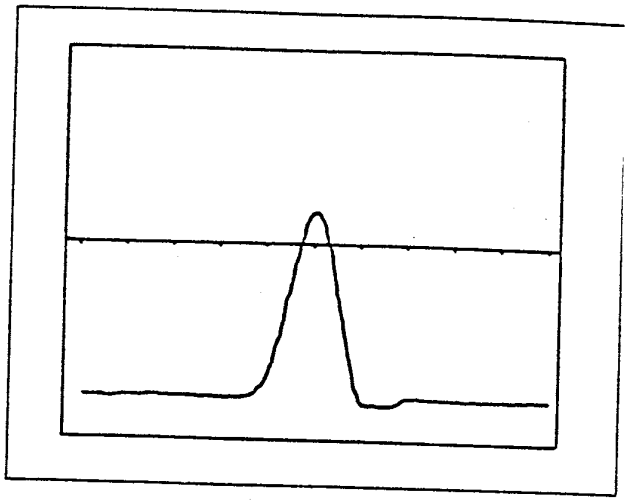

Figure 4.2
Walk Inspect Wave Form
Using Plastic Detectors

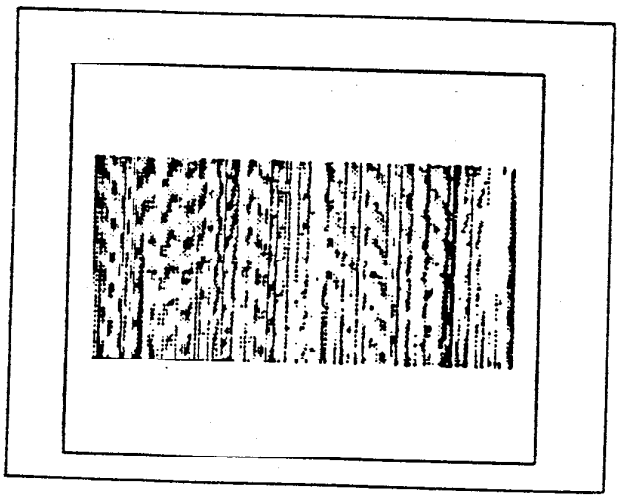

Figure 4.3
Walk Inspect Wave Form
for Slow Detectors

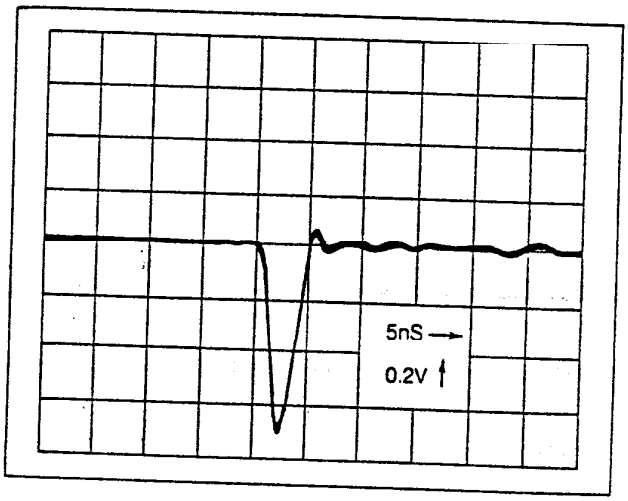

Figure 4.4
Typical Negative Output Pulses into
50 ohms Load

Section 5.
Circuit Description

The 2126 is a high performance Constant Fraction Discriminator in a single width NIM. It also includes a power supply circuit to provide logic power to the unit. This section describes the operation of both the power supply and the Constant Fraction Discriminator.

5.1 POWER SUPPLY

The 2126 consists primarily of ECL logic which uses a supply voltage of -5.2 V. In addition, a TTL supply voltage of + 5.0 V is required. Two methods of obtaining these voltages are provided, selectable by a jumper plug. When the 2126 is used in a NIM bin with the standard supply voltages of ± 12 V and ± 24 V, the logic supply voltages of -5.2 and + 5.0 V are provided by adjustable three-terminal regulators. Q1 and Q2, together with their associated circuitry, provide stable well-regulated logic voltages. If a ± 6 V NIM power supply is available, the 2126 board-mounted jumpers can be set to provide the required logic voltages directly from the ± 6 V supplies. In each case, a diode (D1 for + 6 V, D2 for -6 V) drops the power supply voltages to the logic voltages required by the 2126. In either case, the -2 V ECL pull-down voltage is provided by an additional three-terminal regulator (Q3), operating from the -5.2 V logic supply.

5.2 CONSTANT FRACTION AND THRESHOLD CIRCUITS

The input signal is applied directly to pin 10 of the threshold comparator. D1 provides a temperature compensated voltage which is divided to produce -1 V across the threshold potentiometer (RV1). The wiper voltage of RV1, which varies from -5 mV to -1 V, is applied to pin 10 of the threshold comparator.

The constant fraction function is implemented at the inputs of the ultrafast comparator A4b. The input attenuator module is a X2 attenuator that maintains the proper 50 ohm input impedance. It can be rotated to provide no attenuation (short between the input and pin 5 of the fraction module) or X2 attenuation (100 ohms between the input and pin 5 of the fraction module). The fraction module serves to attenuate both the prompt and delayed inputs to the constant fraction comparator (A4b) while providing the proper 50 ohm input impedance. The prompt input to A4b (pin 8) is attenuated more than the delayed input (pin 7) resulting in the fraction f = 0.4. This combination of attenuation and delay provides the following signals at the inputs of the constant fraction comparator:

pin 8: 0.3 input amplitude, prompt
pin 7: 0.67 input amplitude, delayed by cable selected

See Figure 5.1 which illustrates the signals associated with the constant fraction and threshold comparators.

Prior to the application of an input signal, the inverting output of A4b (pin 2) can be in either logic state depending on the offset voltage applied to A4b pin 8 by the WALK ADJUST potentiometer. Upon application of an input signal, A4b pin 8 initially is lower than A4b pin 7, driving the inverting output A4b pin 2 to a logic high. When the delayed signal arrives at A4b pin 7, it causes this pin to become more negative than A4b pin 8 which causes the inverting output (A4b pin 2) to fall to a logic low. The timing of this low-going signal is input amplitude independent. The inverting output of the threshold comparator (A4a pin 15) is normally a logic high. When an input signal is applied, the inverting output of A4a goes to a logic low when the input signal crosses the selected threshold voltage. This logic transition occurs ahead of the output from the constant fraction comparator since the input to the constant fraction output is delayed by the front panel delay cable. Thus, the 10H209 OR/NOR (A3b) gate has a high input from the threshold comparator and an indeterminant input from the constant fraction comparator prior to the application of an input signal. When an input is applied, A3b pin 7 goes low if the threshold is crossed. Shortly later, A3b pin 5 goes low due to the constant fraction comparator. The inverting output of A3b (pin 3) goes high when the constant fraction comparator fires if the threshold was crossed. This logic signal is the clock to the ultra fast 11C70 D flip-flop A2.

When the 2126 is used in the Constant Fraction mode, the D input of A2 (pin 11) is held at a logic low by A3a pin 14. After the preceding signal was processed, A2 was left in the SET state with the Q output high and the Qbar output low. When the clock signal arrives at A2 pin 7 from A3 pin 3, the D flip-flop is RESET by clocking in the low at A2 pin 11, the outputs are active and the channel is unable to process further inputs. A2 is SET via the HR or NO jumper, thus terminating the outputs and the internal deadtime. In the NOrmal mode of operation, the Q output of A2 is pulled down by the current source consisting of Q9 and associated bias resistors. The line driver/receiver A1a senses the falling edge of A2 pin 2 and drives the SET input of A2 high, thereby SETting A2 and terminating the output. The front panel WIDTH potentiometer varies the current source Q9 and thus varies the rate of fall of A2 pin 2. Thus, the width of the one-shot formed from A2 is varied. In the High Rate mode, the current source Q9 and A1a are bypassed. The rising edge of A2 Qbar is coupled directly to the SET input of A2. Thus, the propigation delays associated with A2 determine the output widths and the internal deadtime.

In the Slow Reject mode, the circuit functions virtually the same. The D input of A2 is driven by A3a pin 14, which now has a low going logic signal driven by the threshold comparator through A3a. A slight delay is provided by R14 and C7. For fast risetime signals, the D input of A2 is low before the clock drives pin 7 high. However, slow risetime signals cause the threshold comparator to fire slightly later. For these slow risetime signals, the falling edge of the signal at A2 pin 11 arrives after the clock at pin 7 and a high is clocked into to flip-flop. Since the flip-flop is already SET, no change occurs at its output and the input signal is ignored.

In the Leading Edge mode, the Constant Fraction comparator (A4b) is disabled in a state that permits the Leading Edge comparator (A4a) to generate the clock for flip-flop A2.

The line driver/receiver A1b is driven by the Qbar output of A2 and serves to drive the two independent negative outputs differentially. It also toggles A1c, the one-shot driving the front panel LED. The negative output transistors are conventional differential switches with the collectors driving the 50 ohm outputs directly.

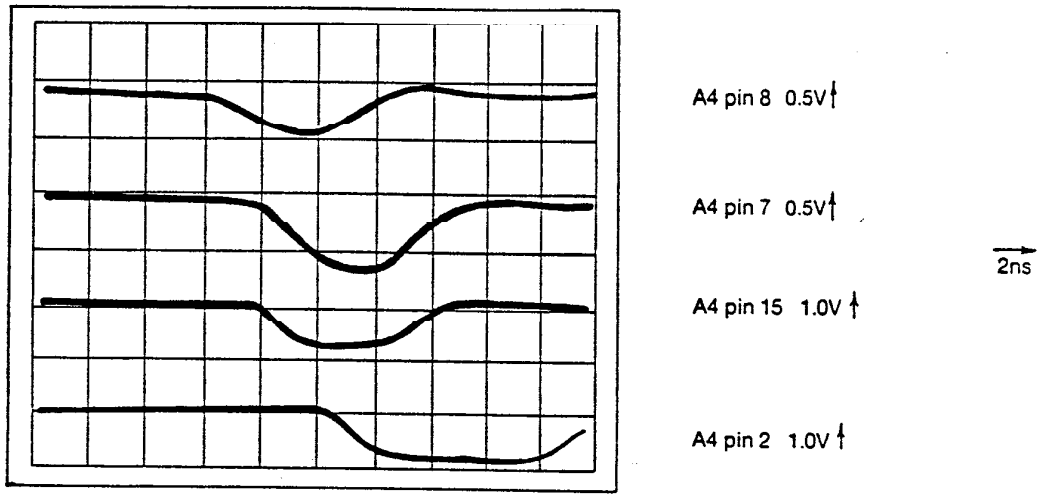

Figure 5.1
Timing Signals

Appendix A. Specifications

A.1 INPUTS

INPUT - Accepts -5 mV to -5 V (-10 mV to -10 V with internal X2 attenuator) linear pulses; rise time $\geq$ 1 ns; Z_{in} = 50 ohms, dc coupled; front panel BNC connector protected to $\pm$ 100 V (duration limited).
DELAY - Two BNC connectors between which a delay cable is connected to form the internal constant fraction signal. Recommended lengths are based upon RG-58 cable propagation delay of $\approx$ 4.8 ns/m to provide a delay of $\approx 0.2\ t_{rise}$ for germanium detectors and $\approx 0.8\ t_{rise}$ for most other detector types.

A.2 OUTPUTS

WALK INSPECT - Displays output signal of zero crossing discriminator for use in trimming time walk; Z_{out} = 50 ohms.
NEGATIVE OUTPUTS - 2 independent negative current outputs, each providing -16 mA into 50 ohms, rise time $\approx$ 1 ns; dc coupled front panel BNC connectors; pulse width controlled by WIDTH potentiometer in Normal mode; 2 ns nominal in High Rate mode.
POSITIVE OUTPUTS - 2 independent positive voltage outputs, each providing 2 V minimum into 50 Ω, 4 V minimum into high impedance, rise time 10 ns or less, dc coupled front panel BNC connectors; pulse width controlled by WIDTH potentiometer in Normal mode, undefined in High Rate mode.

A.3 CONTROLS - FRONT PANEL

THRESHOLD - Front panel 10-turn potentiomenter to set acceptance threshold for input pulses; range -5 mV to -1 V.
WALK ADJUST - Front panel potentiometer to compensate walk of the internal zero crossing discriminator.
WIDTH - Front panel 10-turn potentiometer to vary internal deadtime and width of negative outputs in Normal mode. Range $\approx$ 2-100 ns or $\approx$ 10-500 ns as determined by internal jumper. Inoperative in High Rate mode.

A.4 CONTROLS - INTERNAL

ATTENUATION - Board mounted DIP jumper selects no attenuation or X2 attenuation of input signal.
FRACTION - Board mounted DIP jumper selects value of constant fraction; 0.4 standard, other values available by special order.
TIMING MODE - Board mounted jumper selects Constant Fraction (CF) or Constant Fraction with Slow Risetime Reject (SR) timing mode.
OPERATING MODE - Board mounted jumper selects Normal (NO), or High Rate (HR) operating mode.
OUTPUT WIDTH RANGE - Board mounted jumper selects $\approx$ 2-100 ns (X1) or 10-500 ns (X5) output WIDTH range.
POWER SUPPLY - Board mounted jumpers select $\pm$ 12 V or $\pm$ 6 V as input power for 2126 logic.

A.5 PERFORMANCE

DYNAMIC RANGE - 1000:1
WALK - < 100 ps for a 1 ns rise-time pulse over a 100:1 dynamic range (referenced to -5 V) in the CF mode.
COUNTING RATE - Normal mode to 150 MHz, as limited by deadtime; High Rate mode to 200 MHz.
PULSE PAIR RESOLUTION - Normal mode < 7 ns as limited by deadtime; High Rate mode $\leq$ 5 ns.
THRESHOLD STABILITY - Better than $\pm$ 0.02%/°C ($\pm$ 200 ppm/°C)
TEMPERATURE RANGE - 0°C to +50°C
THRESHOLD LINEARITY - $\pm$ 0.25% integral

A.6 TYPICAL CABLE LENGTHS (RG-58)

For plastic, NaI, and silicon detectors - 0.3 to 1.0 m (1.0 to 3.3 ft.)
For Planar Ge Detectors - 1.0 to 2.0 m (3.3 to 6.6 ft.)
For Coaxial Ge Detectors - 2.0 to 4.0 m (6.6 to 13 ft.)

A.7 POWER REQUIREMENTS

Power jumpers set to $\pm$12 V:
+12 V dc — 130 mA
- 12 V dc — 350 mA*

Power jumpers set to $\pm$ 6 V:

+12 V dc — 20 mA	+6 V dc — 130 mA
- 12 V dc — 120 mA	- 6 V dc — 250 mA

*Exceeds the NIM power allotment for a single-width module.

A.8 PHYSICAL

SIZE - Single width NIM module 3.43 × 22.12 cm (1.35 × 8.71 in.) per TID-20893 (rev.)
NET WEIGHT - 0.9 kg (2.0 lbs.)
SHIPPING WEIGHT - 1.8 kg (4.0 lbs.)