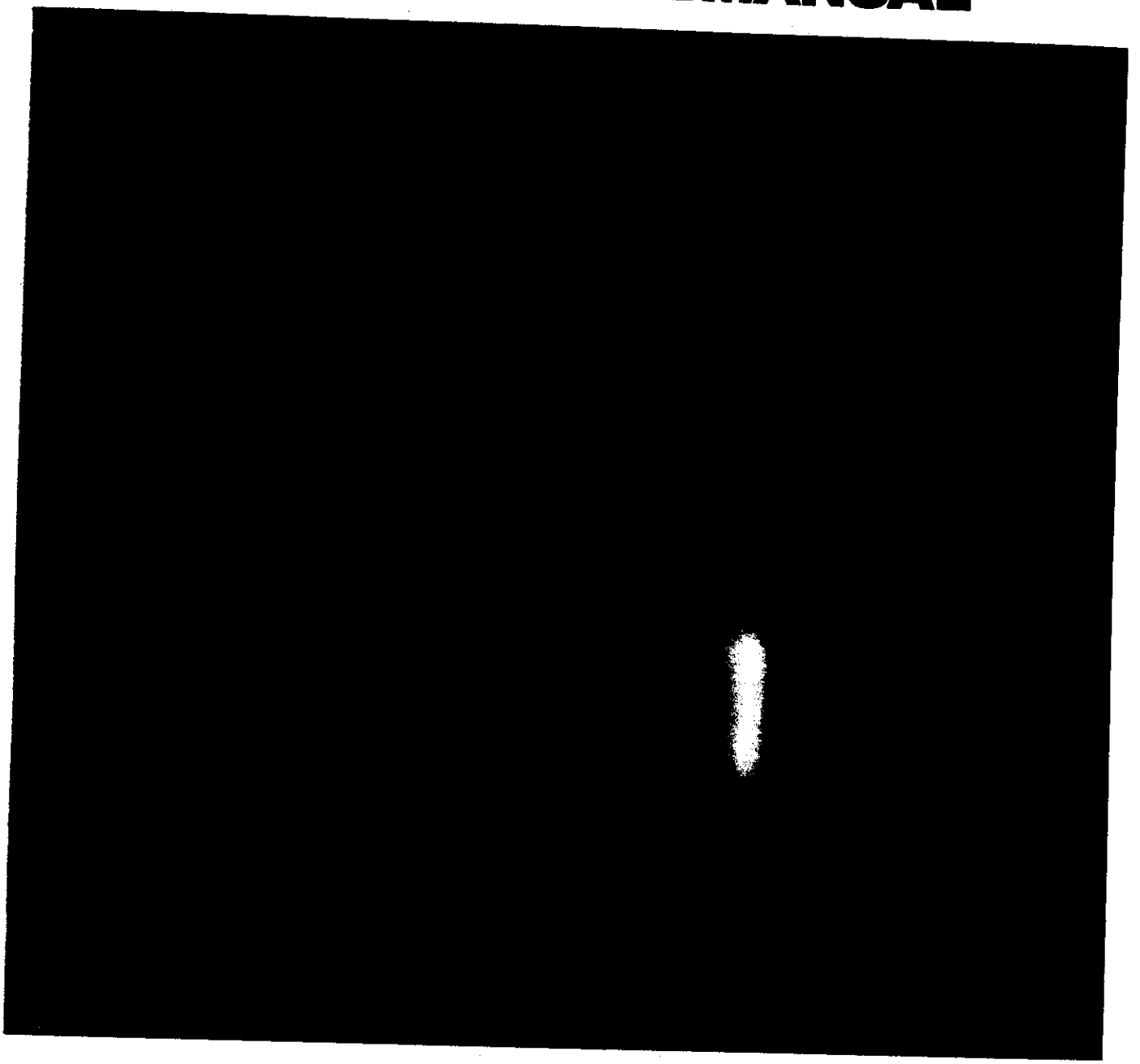
CANBERRA INSTRUCTION MANUAL



MODEL 2110
Timing Filter Amplifier

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TIMING FILTER AMPLIFIER

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MODEL 2110

TIMING FILTER AMPLIFIER

Section 1

INTRODUCTION

1.0 GENERAL

The Canberra Model 2110 Timing Filter Amplifier is a wideband DC coupled amplifier designed for maximum flexibility in the nuclear physics laboratory. The unit accepts positive or negative impulses from a wide range of detector preamplifiers and provides continuously adjustable gain, selectable differentiation and/or integration, and DC level adjustment to suit the needs of advanced experimental work. The unit delivers an output of up to ± 5V into a 50 ohm load.

Primarily designed to enhance timing analysis with moderate (NaI) to slow [Ge(Li)] speed radiation detectors when used in conjunction with a constant fraction discriminator such as the Model 1428A, this instrument will still fulfill the needs of more general laboratory applications requiring a stable DC coupled fast pulse amplifier.

The gain range of the Model 2110 has been keyed to the most common laboratory requirements, and spans a range of x1.5 to x100. To provide maximum resolution and user convenience, the switch selectable gain range increments in binary steps from x3 to x100, and the fine gain control range is ≈ x0.45 to x1.0.

A pair of front panel connectors is available to employ delay cable clipping of the input. This feature is useful in extracting the desired signal from varying DC levels on the source signal such as the ramp of pulsed optical feedback preamplifiers when single differentiation may be undesirable because of tailing or uncompensated secondary time constants. Delay cable clipping also provides the fastest shaping possible, and is most effective in processing very high count rate inputs. The Canberra Model 2058 Delay module provides the required 50 ohm impedance cable and permits delays up to 63.5 nanoseconds in 0.5 nanosecond increments.

The front panel shaping switches permit defeat of differentiation (full DC coupling) and/or integration, or independent selection of RC clipping and/or smoothing time constants of 10, 20, 50, 100 or 200 nanoseconds as required. The user may also employ fast differentiation and integration in conjunction with a delay cable at the input as provided to generate a fast bipolar shaped timing signal for zero crossing analysis.

The unique combination of fast risetime (5 nanoseconds), bipolar signal handling capability, full flexibility in pulse shaping, and high count rate capability collectively offers the experimentalist significant improvements in timing measurement capability.

Section 2

SPECIFICATIONS

2.1 INPUTS

SIGNAL INPUT

Accepts positive or negative detector or preamplifier impulses; when used with clipping cable, accepts DC levels of up to ± 3V; input clamp protected to ± 6V; input impedance 50 ohms, DC coupled.

Linear input signal range is dependent on the selected shaping mode:

a) in full DC mode, with INT-TIME CONST. and DIFF-TIME CONST. switches set to OUT, linear input range = output voltage swing range (up to ± 5V) + selected gain.

b) in shaped mode, with INT-TIME CONST. and DIFF-TIME CONST. switches each set to any position other than OUT, linear input signal range is limited by the COARSE GAIN as follows:

COARSE GAIN	INPUT RANGE
100	± 0.25V
50	± 0.5V
25	± 1V
12	± 2V
6	± 4V
3	± 8V

CLIP CABLE

A pair of front panel connectors accommodates any length of 50 ohm cable to provide delay clipping of the input pulse shape and rejection of the common mode DC level.

A 50 ohm terminator provided with the instrument is normally left secured to the left hand clip cable BNC connector when a clipping cable is not used. This terminator provides the 50 ohm input impedance in the normal mode.

2.2 OUTPUT

SIGNAL OUTPUT

Provides ± 5.0V minimum to a 50 ohm load, with shaping or polarity as selected by front panel controls; short circuit proof current source output, direct coupled.

2.3 PERFORMANCE

RISE TIME

With the INT-TIME CONST control set to OUT, risetime is $\leq$ 5 nanoseconds for up to $\pm$ 5V output to an external 50 ohm resistive load. In other settings, risetime $\simeq$ 2.2 x selected integration time constant.

OVERSHOOT

Less than 10% for INTEG-TIME CONST set to OUT.

Less than 2% for any other selected integration time constant.

NONLINEARITY

Less than $\pm$ 1% (integral) for up to $\pm$5V output to an external 50 ohm resistive load, with any selected shaping, and with input signal within linear range specified above.

GAIN STABILITY

Better than $\pm$ 0.1%/°C averaged over a range of 0 to 50° C ambient.

DC DRIFT

Output DC level shift is better than $\pm$ 1mV/°C averaged over a range of 0 to 50° C ambient.

NOISE

Less than 50μV RMS referred to the input for maximum gain in a wideband mode (DIFF and INT-TIME CONST switches set to OUT) over a 100MHz bandwidth. With 200 nanosecond DIFF and INT-TIME CONST selections, RMS noise referred to the input is less than 15μV.

2.4 CONNECTORS

All input and output connectors are type BNC.

2.5 POWER REQUIREMENTS

+24 VDC:	45mA
-24 VDC:	0mA
+12 VDC:	400mA *
-12 VDC:	375mA *

* This current drain exceeds the normal Bin allotment of 167mA for a single width NIM module.

2.6 PHYSICAL

SIZE

Standard single width NIM module (1.35 x 8.71 inches) (3.5 x 22.1 cm) per TID-20893 (rev.)

NET WEIGHT

1.9 lbs. (0.9 kgs)

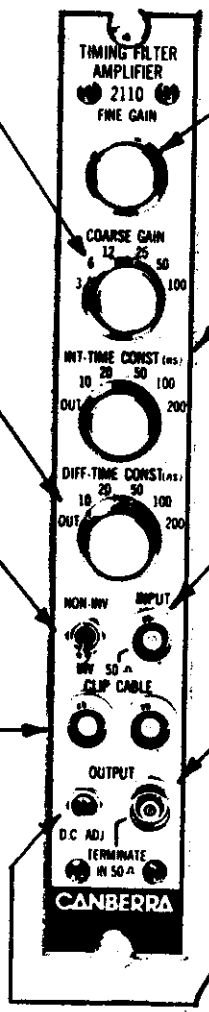
Section 3

CONTROLS AND ADJUSTMENTS

3.1 GENERAL

Complete understanding of the purpose of the various controls and connectors is essential for the proper operation of the 2110 and it is strongly recommended that this section be read before proceeding with the operation of the module.

3.2 FRONT PANEL



COARSE GAIN
Six position rotary switch to select gain factors of 3, 6, 12, 25, 50 or 100

DIFF-TIME CONST
Six position rotary switch to select RC differentiation time constant (DC coupled, 10, 20, 50, 100 or 200 nanoseconds)

INV-NON INV
Toggle switch to select inverting or non-inverting output polarity.

CLIP CABLE
Provision to use external cable for fastest clipping of pulse width. A 50 ohm terminator is used on left connector when cable clipping is not employed.

FINE GAIN
Single turn potentiometer to adjust gain factor from x0.45 to x1.0.

INT-TIME CONST
Six position rotary switch to select RC integration time constant (none, 10, 20, 50, 100 or 200 nanoseconds).

INPUT
Accepts positive or negative detector signal pulses; Zin = 50 ohms, direct coupled.

OUTPUT
Provides current output to external 50 ohm load; swing range ±5V, short circuit protected.

DC ADJ
22 turn screwdriver adjustment potentiometer to trim output base line to 0 VDC.

Section 4

OPERATING INSTRUCTIONS

4.1 GENERAL

The primary application of the Model 2110 Timing Filter Amplifier is amplification and pulse shaping in the timing path of a detection system. This section will outline a generally applicable adjustment procedure. Details relevant to specific applications will be discussed in Section 5, Application Notes.

> **IMPORTANT NOTE**
>
> Prior to final adjustment, allow at least one hour warm-up stabilization time to avoid DC level shifts.

When setting up the amplifier, keep in mind that this is a truly DC coupled instrument; i.e., DC offset voltages generated within the unit (which are unavoidable in practice) are transmitted to the output. Changing the gain or switching from inverting to non-inverting mode or vice versa will affect the DC output level. This is especially true when switching the DIFF-TIME CONST selector from OUT (DC coupling from input to output) to some other position. These level shifts can be compensated by adjusting the DC ADJ control. In practice it is sufficient to adjust the DC level to 0V at the beginning of the set up procedure, and to do a final touch-up at the end.

4.2 GENERAL ADJUSTMENT PROCEDURE

1. Observe the pulses coming from the test signal source on a sufficiently fast oscilloscope, using a 50 ohm terminator, and determine the pulse rise time, decay time and amplitude. This will provide orientation for setting up the gain and shaping time constants of the Timing Filter Amplifier. Check if the linear input range (including DC offset) may be exceeded (see Section 2.1).

2. Connect the signal source of the input connector. If no CLIP CABLE is used be sure that the chained 50Ω terminator is placed on the left hand CLIP CABLE connector.

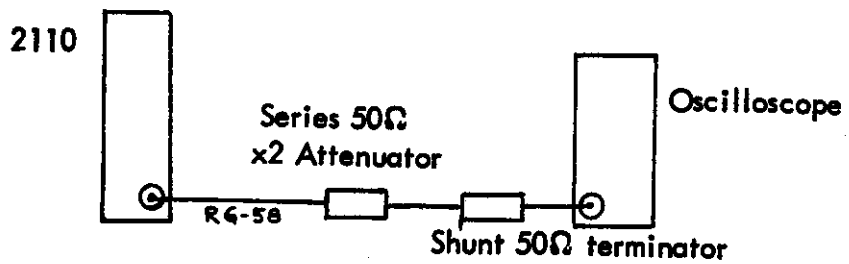
3. Set the NON-INV/INV toggle switch to the appropriate position.

4. Set the DIFF-TIME CONST switch to the anticipated value (at this point it is only important to decide if the correct setting is either OUT or any other setting). If in doubt, select the 200ns setting.

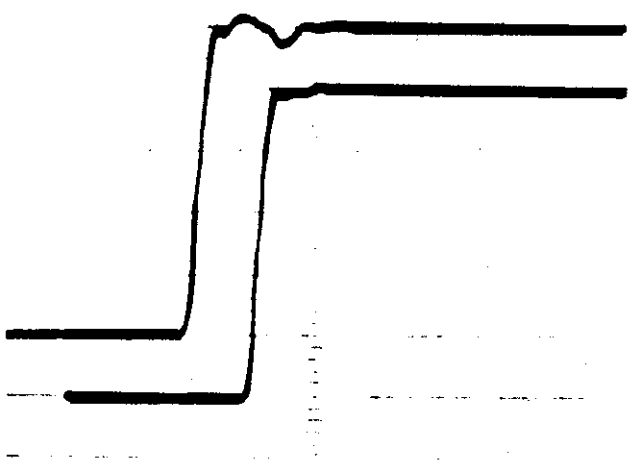
4.2 GENERAL ADJUSTMENT PROCEDURE (cont.)

5. Monitor the OUTPUT of the amplifier on an oscilloscope, using the DC coupled input mode for all observations.

IMPORTANT NOTE: If the vertical amplifier of the oscilloscope has a 50 ohm resistive input the resulting display will be correct. If the oscilloscope vertical amplifier has an input of 1MΩ shunted by some capacitance (typically 20-30pf), then an attenuator and terminator must be used as illustrated below to prevent the reactive impedance from causing a reflection thru the cable, and distorting the signal shape.



The photo below illustrates the kind of signal distortion caused by the reflection described above in the upper trace. The lower trace illustrates a normal clean output using the recommended termination.



4.2 GENERAL ADJUSTMENT PROCEDURE (cont.)

6. Monitor the OUTPUT of the amplifier and reduce the COARSE GAIN if overloading occurs.

7. Set the DC output level to 0V with the DC ADJ control.

8. Increase the INT-TIME CONST (beginning in the OUT position) until the rise time at the amplifier output begins to increase, thereby matching the bandwidth of the amplifier to the frequency spectrum of the input pulse. In certain cases it might be advantageous to deviate from this rule, e.g., with coaxial Ge(Li) detectors, where larger integration time constants are often used to equalize pulse risetimes.

9. Now set the DIFF-TIME CONST. In general, signal to noise ratio is optimum for DIFF = INT. However, if minimum pulse width is desired to reduce pile up, smaller values of DIFF should be tried. In this case delay line clipping is often the optimum choice.

   For cable clip operation remove the 50Ω terminator from the left hand CLIP CABLE connector and connect a 50Ω coaxial cable whose length corresponds to the desired clipping time (propagation time for RG-58 cable ≈ 1.5 nanoseconds/ft. or 5.0 ns/m). For details see Section 5.1, Application Notes. In principle, any combination of RC differentiation and cable clipping is possible.

   NOTE: The introduction of RC shaping reduces the effective gain of the amplifier, depending on the input pulse width and the selected combination of INT-TIME CONST and DIFF-TIME CONST. The nominal gain figures only apply to wideband operation (DIFF-TIME CONST and INT-TIME CONST in OUT position). Figures 4-1 to 4-4 illustrate the effect of various combinations of shaping time constants.

10. Set the desired output amplitude by a suitable combination of COARSE GAIN and FINE GAIN settings. The overload margin is greatest in the extreme clockwise setting of the FINE GAIN control. Due to the excellent overload characteristics of the 2110, a certain amount of overload can be tolerated as long as the trigger level of the subsequent discriminator is still in the linear range.

11. As a final step touch up the DC ADJ for an output base line of 0V.

BASIC SHAPINGS

All illustrations are at 1V/DIV. vertically, 50nsec/DIV horizontally. Input is step pulse. Output illustrated for positive only.

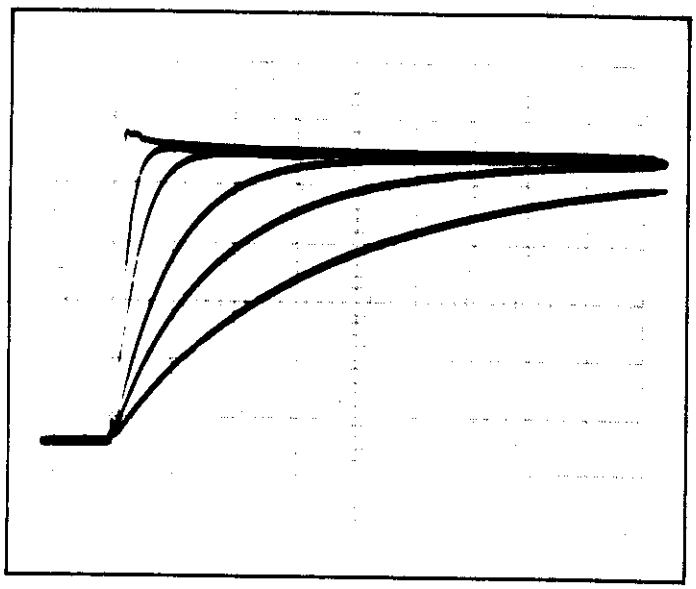


Figure 4-1: INTegration (with DIFFerentiation OUT) for positions OUT, 10, 20, 50, 100 and 200 nanoseconds.

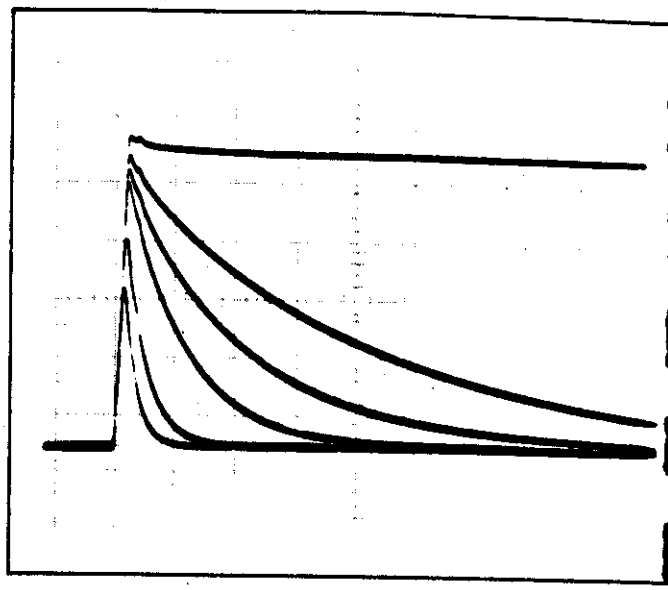


Figure 4-2: DIFFerentiation (with INTegration OUT) for positions OUT, 10, 20, 50, 100, and 200 nanoseconds.

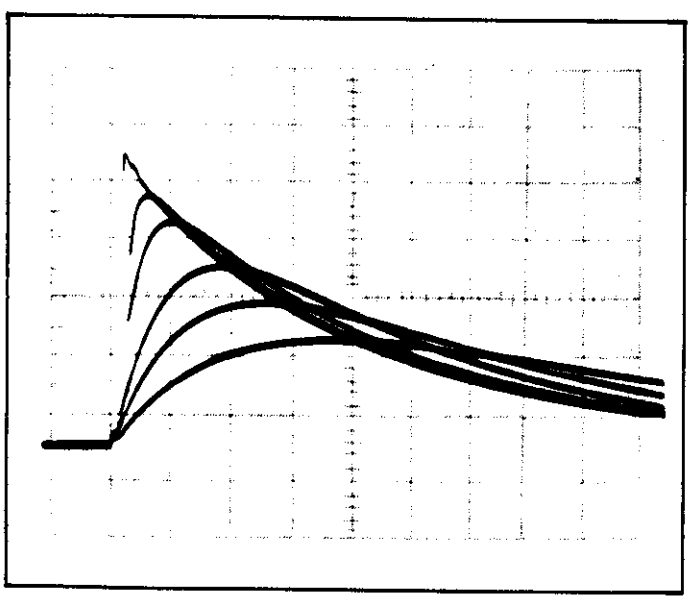


Figure 4-3: Effects of selected INTegrations of OUT, 10, 20, 50, 100, and 200 nanoseconds for set 200 nanoseconds DIFFerentiation.

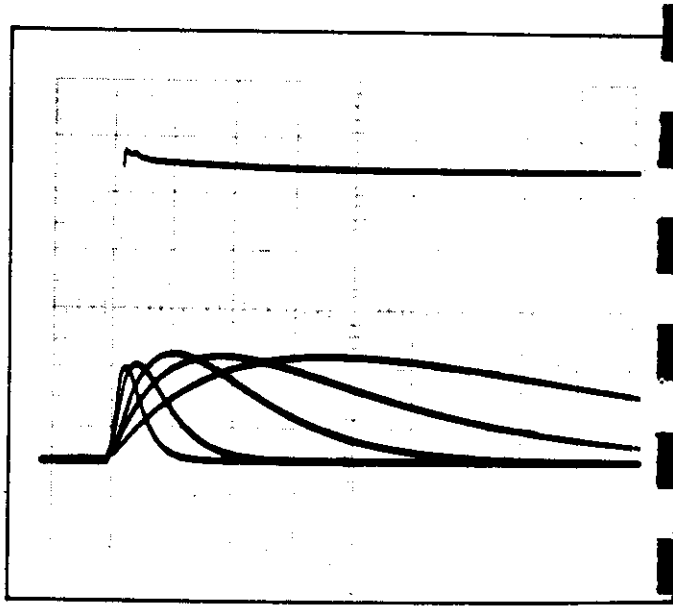
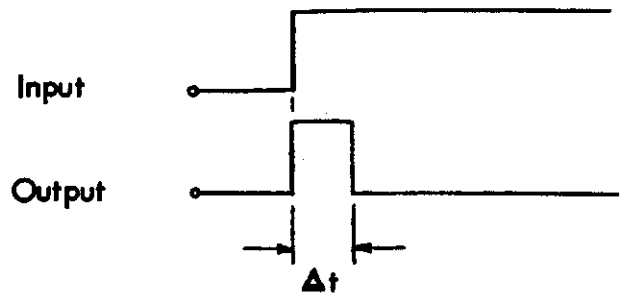


Figure 4-4: Waveshapes for equal INTegrations and DIFFerentiations of OUT, 10, 20, 50, 100, and 200 nanoseconds successively.

APPLICATION NOTES

5.1 DELAY LINE CLIPPING

Delay line clipping is optimum for applications requiring fast pulse pair recognition, i.e., fast baseline recovery. The principle of delay line clipping is to subtract a time delayed replica of the input pulse from the non-delayed input pulse as depicted below.



Δt is the time delay introduced by the delay cable connected to the CLIP CABLE connectors. The cable must have a 50Ω impedance and may be of any length.

The step input pulse shown above is an idealized case, where there is no decay time constant. This premise would only be valid for the output signals of pulsed feedback preamplifiers, but it is adequately met for many resistive feedback charge-sensitive preamplifiers if the clip cable length (delay time) is quite short compared to the decay time. The advantage of cable clipping is superior base line recovery compared to the exponential decay produced by RC clipping ("differentiation"). This improvement is a definite asset in processing pulses at very high rates (> 1MHz).

If the applied input pulse already has a fairly short exponential decay relative to clipping delay, baseline recovery is less rapid than for the step input, but still superior to simple RC differentiation.

5.1 DELAY LINE CLIPPING (cont.)

The photograph below illustrates the baseline overshoot produced on the output for one selected clipping cable length (lower trace) operating on an already fairly short input decay.

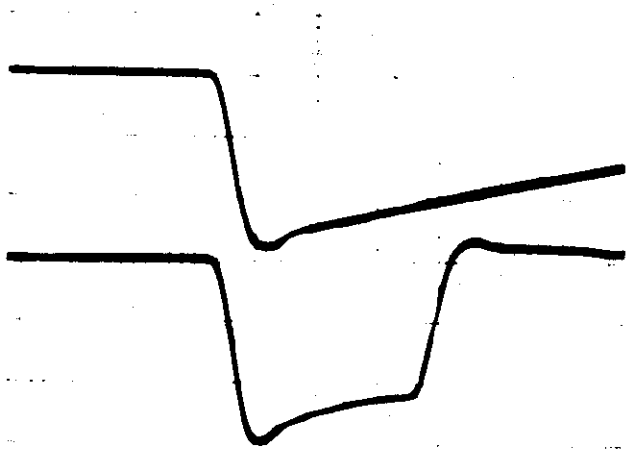


Figure 5-1

5.1 DELAY LINE CLIPPING (cont.)

Baseline recovery may be improved by using additional RC clipping (the DIFF-TIME CONST control set to some position other than OUT), thereby forming a fast bipolar pulse as illustrated below, in Figures 5-2 and 5-3.

Illustrations with output at 1V/div. vertically; horizontal at 50nsec/div.

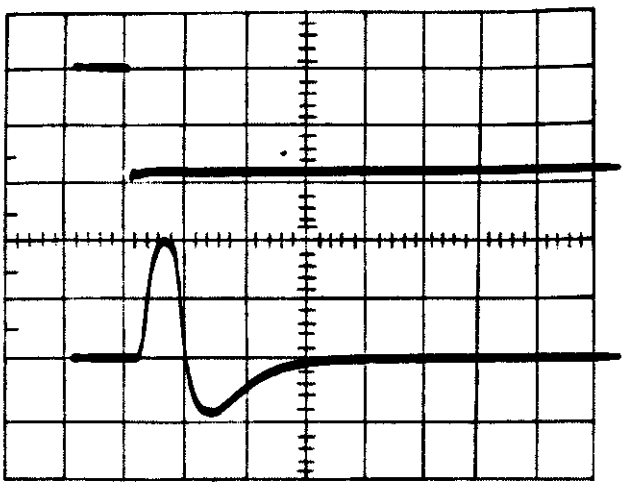


Figure 5-2: Bipolar output pulse for step input simulating pulse from pulsed-optical feedback preamp. Clip cable, INT and DIFF each 20 nanoseconds.

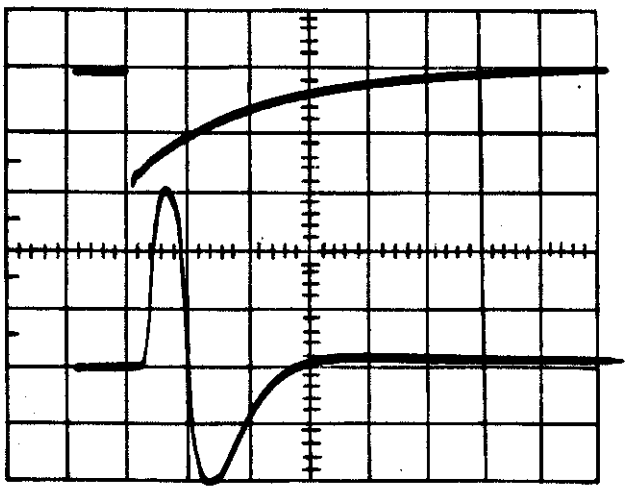


Figure 5-3: Bipolar output pulse for fast tail pulse input. Clip cable, INT and DIFF each 20 nanoseconds.

A better method to obtain fast baseline recovery is to attenuate the delayed subtraction signal by $e^{-\Delta t/\tau}$ where Δt is the delay time and τ the decay time constant of the input pulse.

for $t > \Delta t$:

$$V_o' = V_o e^{\frac{-t}{\tau}} - V_o e^{\frac{-\Delta t}{\tau}} \cdot e^{\frac{-(t-\Delta t)}{\tau}}$$

$$V_o' = V_o \left(e^{\frac{-t}{\tau}} - e^{\frac{-\Delta t}{\tau}} \cdot e^{\frac{-t}{\tau}} \cdot e^{\frac{+\Delta t}{\tau}} \right) = 0$$

5.1 DELAY LINE CLIPPING (cont.)

This situation is shown below schematically in Figure 5-4.

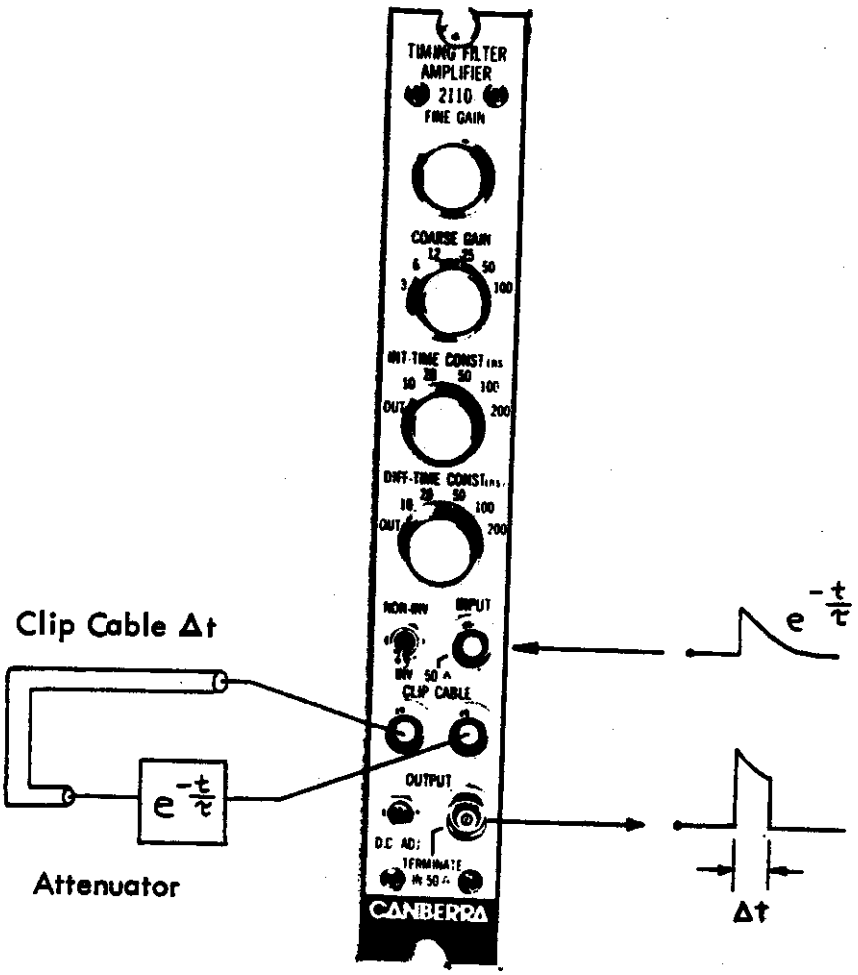


Figure 5-4

This scheme requires close matching of the delay time and the attenuation factor, and requires the use of a variable 50Ω attenuator, an item not commonly found in nuclear physics laboratories. An alternative scheme is to use a fixed attenuator and a variable delay. The 0.5 ns increments provided by the Canberra Model 2058 Nanosecond Delay are usually adequate for good compensation. Fixed 50Ω attenuators for 3 dB (attenuation factor = 0.7) and 6 dB (attenuation factor = 0.5) are readily available or can easily be constructed with common carbon composition or metal film resistors.

5.1 DELAY LINE CLIPPING (cont.)

The photograph below illustrates a fast decay input pulse in the upper trace, and 2 examples of clip cable shaping in the lower 2 traces. Series resistive attenuation was used with the clipping cable as indicated above to enhance the baseline recovery.

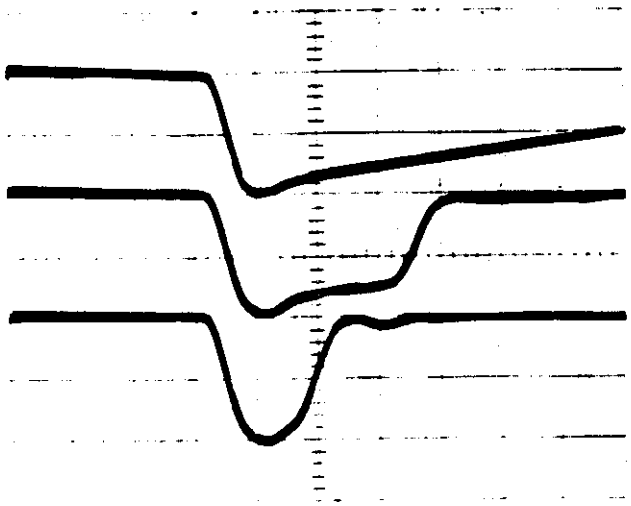


Figure 5-5

This fast "pole zero compensation" scheme is strictly applicable to exponentially decaying pulses, but it is also quite effective on the anode pulses of NaI (Tl) scintillation detectors where the decay is characterized by several time constants but dominated by one.

In cases where some integration may also be used without degrading the time data, a further smoothing to suppress small finite reflections is possible, as illustrated in Figure 5-6.

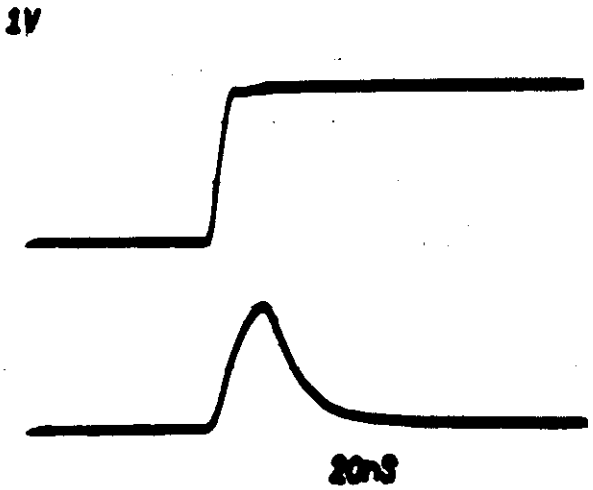


Figure 5-6

5.2 DERIVATION OF TIMING SIGNALS FROM PULSED OPTICAL FEEDBACK DETECTOR SYSTEMS

In a pulsed optical feedback preamplifier, the detector pulses are superimposed on a slowly varying voltage ramp over a range of several volts. In a DC coupled system the ramp voltage - which in an X-ray system may be several orders of magnitude larger than the detector pulses - would severely limit the dynamic range of the system due to overload in the input circuit of a high gain amplifier. The Model 2110 Timing Filter Amplifier offers a unique solution to this problem by means of the clip cable mode. In this mode, the ramp voltage is turned into a common-mode component which is suppressed by the differential input stage of the 2110 (see Section 6.1). At maximum gain, the permissable common mode voltage range of the 2110 is ± 3V, which is adequate for all pulsed optical feedback preamplifiers currently on the market. In order to avoid unnecessary degradation of signal to noise ratio - of prime importance for low energy work - the clipping time should be larger than the risetime of the output pulses of the preamp. Note that these risetimes may range up to 200 ns, depending on the detector and preamplifier in use.

5.3 NaI (Tl) - Ge(Li) FAST-SLOW COINCIDENCE ELECTRONICS

Figure 5-4 illustrates a typical fast-slow coincidence set up using a NaI (Tl) scintillation detector and a Ge(Li) detector. Typical INTegration TIME CONSTant for the NaI (Tl) detector are OUT, 10, or 20 ns depending on the quality of the phototube. The DIFFerentiation TIME CONSTant is typically 100 or 200 ns (or 200 to 300 ns cable clipping). On the Ge(Li) side the proper shaping time constants depend on the size and geometry of the detector. With coaxial geometry it may be advantageous to partially equalize the varying risetimes of the output pulses by judicious selection of the integration time constant, depending on the rise time compensation properties of the timing discriminator. In all of these applications, it is necessary to determine optimum combinations of shaping constants experimentally.

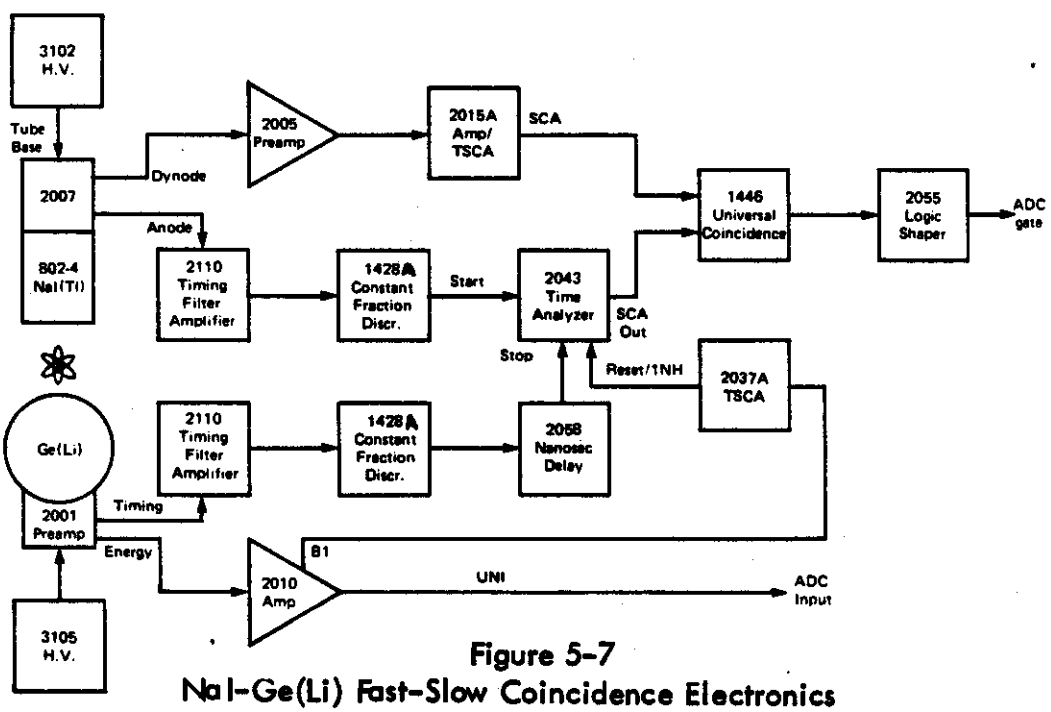


Figure 5-7
NaI-Ge(Li) Fast-Slow Coincidence Electronics

5.4 DRIVING MULTIPLE LOADS

The OUTPUT of the Model 2110 is designed to normally drive one 50 ohm resistive load. The photograph below illustrates a normal output in the upper trace, and the effect of connecting 2 such 50 ohm loads via "tee" connectors to the front panel OUTPUT in the lower trace. Note both the attenuation and slight increase in ringing evident (both shapings OUT).

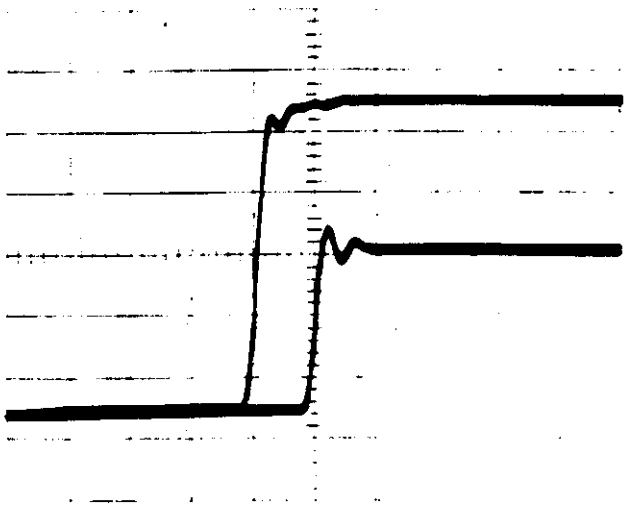


Figure 5-8

An alternate scheme to accommodate dual loads is the use of RG-62 (93Ω) ohm coax cable from a "tee" on the front panel OUTPUT of the Model 2110 to individual 100 ohm load terminations. Where the loads can be altered to provide this impedance, a full range output swing and clean wavefront can be delivered to each, as illustrated below.

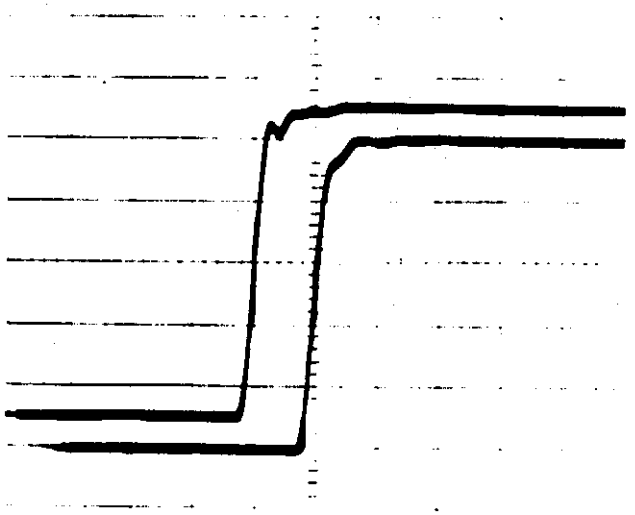


Figure 5-9

THEORY OF OPERATION

6.1 ARCHITECTURE

In the Model 2110 Timing Filter Amplifier, input signals are applied through a switched constant impedance attenuator (COARSE GAIN) to one input of a differential amplifier. In the delay line clipping mode the input signal is routed to the second input of the differential amplifier via the CLIP CABLE to perform the subtraction operation.

NOTE: It is possible to operate the 2110 Timing Amplifier in a differential input mode by applying the differential input signals to the CLIP CABLE connectors and placing the chained-on 50Ω terminator on the INPUT connector with a "tee". However, the COARSE GAIN control is only effective in the X100 and X50 positions in this mode of operation.

Following the first gain stage are a switched passive RC integrator (INT-TIME CONST), a switched passive RC differentiator (DIFF-TIME CONST), a composite differential gain block, and a class A tranconductance output amplifier. Differential emitter followers between these stages minimize mutual interactions.

This sequence of shaping and gain stages was chosen to obtain maximum dynamic range, especially with unfavorable combinations of τ_{diff} and τ_{int}. This scheme has two disadvantages: 1. Noise voltage referred to the input increases with decreasing values of COARSE GAIN (since this is actually an input attenuator). 2. Noise generated in the second gain block and in the output driver is not reduced by bandwidth reduction due to pulse shaping or by gain reductions. However, these trade-offs are justified by the following considerations: 1. Low gain settings imply a large input signal where signal-to-noise ratio at the amplifier input is of lesser importance. 2. The purpose of a timing filter amplifier is to provide gain, pulse shaping facilities and output drive capability. In applications where signal-to-noise ratio is crucial, it should be defined at the input of a preamplifier which is mounted close to the detector and which provides sufficient gain to override the noise of subsequent units.

6.2 CIRCUIT DESCRIPTION

Throughout the following circuit descriptions refer to the circuit schematic.

INPUT STAGE

IC1 - a monolithic transistor pair - forms the basic differential input stage. The emitter current source Q1 provides common mode rejection. COARSE GAIN is decreased by introducing additional emitter degeneration (relay switched) in the X50 position.

INPUT STAGE (cont.)

In the other positions a passive input attenuator is introduced. The input attenuation scheme maintains a balanced, essentially constant source impedance to the inputs of the differential amplifier to maintain DC stability in different COARSE GAIN positions. RV1 is pre-adjusted internally for best DC balance between the direct coupled and differentiated modes.

Input overvoltage clamping protection at approximately ± 5V is provided to each side of the differential amplifier.

SHAPING

Shaping is performed in both legs of the differential output of the first gain stage by a dual integrator and a succeeding dual RC differentiator. Emitter follower stages IC2, IC3a, and IC3b provide isolation. IC3c provides a stable common mode DC bias for the input of IC3b when RC differentiation is selected. R40 and R41 steer this bias to the inputs and provide the load resistance for the selected clipping time constant.

FINE GAIN

FINE GAIN is controlled by a continuously adjustable resistor-FET attenuator R46-Q2, R47-Q3. Maximum attenuation is set by RV2.

DIFFERENTIAL GAIN BLOCK

A differential cascode amplifier formed by IC4 in the pattern of the Gilbert gain cell, and Q4 and Q5 as buffered by IC6, provides a broadband voltage gain of about 13. Polarity inversion (INV/NON-INV) is provided by retarding gain in one side of the cross coupled differential pair. IC5 provides a stabilized current source for biasing the gain block. IC7 regulates the common mode component at the output of IC6. This loop does not introduce any low frequency limitation but acts to stabilize the DC balance and preserve DC coupling.

OUTPUT DRIVER

Q9 through Q14 comprise a complementary symmetry class A transconductance (voltage to current) driver. The output current drive affords a voltage thruput gain of X2 to a 50 ohm load, with an output swing range linear to ±5V minimum. This scheme as a current drive output permits the fastest and cleanest high level transitions to be fed through a coaxial cable to a remote load, but of course depends upon a resistive load impedance to properly match the transmission line. The current limited design is inherently output short-circuit proof.

OUTPUT DRIVER (cont.)

Symmetry of the output swing is essential to optimize overload recovery. IC9 biases the output push-pull stages as a voltage mirror, and the current swing limit is trimmed by RV7.

The driver section is biased by a second voltage mirror in IC8, Q6, Q7, and Q8. The front panel "DC ADJ" is derived from this regulator to balance the output current by introducing an offset voltage summed into IC8.