CONSTANT FRACTION TIMING SCA
Model 2035A

Instruction Manual
March, 1979

CANBERRA INDUSTRIES, INC.
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BASIC WARRANTY

CANBERRA - MANUFACTURED EQUIPMENT

Equipment manufactured by Canberra Industries, Inc. is warranteed against defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in the instruction manuals. During the warranty period, repairs or replacement will be made at Canberra's option on a return to factory basis. The transportation cost, including insurance, to and from Canberra, is the responsibility of the Customer. Except for defects discovered upon initial operation, shipping expense to Canberra is to be paid by the customer; shipping expense to return the repaired equipment will be paid by Canberra.

The customer must obtain shipping instructions, including an Authorized Return Number (ARN), before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty*. In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment. If, upon receipt of the equipment, Canberra determines that such equipment is not defective within the terms of this warranty, the customer shall pay to Canberra, upon invoice, the cost of diagnosis at the then prevailing Canberra repair rate and the cost of return transportation.

The Canberra Basic Warranty applies only to equipment manufactured by Canberra which is returned to the factory. If equipment must be repaired at the customer's site, the actual repair labor and parts will be provided at no charge during the warranty period. However, travel expenses to and from the customer's site, and living expenses while on site, shall be paid by the customer unless an On-Site Warranty Option has been purchased. This option may only be purchased prior to shipment of the equipment to the customer.

This warranty shall not apply to Canberra equipment that has been modified or serviced by other than Canberra Service Personnel, or to failures of Canberra equipment caused by defective equipment not manufactured by Canberra.

The Express warranties set forth herein are the only warranties with respect to the products, or any materials or components purchased from others and furnished by Canberra, and there are no other warranties, expressed or implied. The warranty of merchantibility is expressly limited as herein provided and all warranties of fitness are expressly disclaimed and excluded. Canberra shall have no liability for any special, indirect or consequential damages, whether from loss of production or otherwise, arising from any breach of warranty hereunder or defect or failure of any product or products sold hereunder.

EXCLUSIONS

Warranty service is contingent upon the proper use of all equipment and does not cover equipment which has been modified without Canberra's written approval or which has been subjected to unusual physical or electrical stress as determined by Canberra Service personnel. Canberra Industries shall be under no obligation to furnish warranty service (preventive or remedial): (1) if adjustment, repair or parts replacement is required because of accident, neglect, misuse, failure of electrical power, air conditioning, humidity control, transportation, or causes other than ordinary use: (2) if the equipment is maintained or repaired or if attempts to repair or service equipment are made by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by warm-up or by neutrons or heavy charged particles. Damage from these causes is readily identifiable as described in the manual accompanying each detector.

EQUIPMENT NOT MANUFACTURED BY CANBERRA

Canberra's basic one-year warranty applies only to equipment manufactured by Canberra. Although Canberra may frequently supply, as part of systems, equipment manufactured by other companies, the only warranty that shall apply to such non-Canberra equipment is that warranty offered by the original manufacturer if any.

Canberra will, upon request, offer, as an option, warranty coverage for non-Canberra equipment such as computers and peripherals sold as part of a system supplied by Canberra. Quotations on this coverage may be obtained by contacting Canberra Nuclear Systems Division.

SOFTWARE

Canberra warrants proper system operation *only* with programs developed by Canberra using the operating system supplied to the customer. Canberra assumes no responsibility for user-written programs or programs published as part of information exchange in Canberra periodicals.

Engineering assistance for software development is available and can be contracted through the Canberra Nuclear Systems Division Sales Department.

INSTALLATION

Installation of equipment purchased from Canberra shall be the sole responsibility of the customer unless the installation is specifically contracted for at the prevailing Canberra field service rates. To insure timely installation after receipt of equipment, it is recommended that installation be contracted for at the time the equipment is ordered.

ON-SITE WARRANTY OPTION

The On-Site Warranty Option provides for free on-site warranty work (Canberra pays all travel and living expenses) within the first 90 days after delivery of equipment to the customer. If installation is ordered from Canberra, the 90 day period commences upon completion of the initial installation. After the 90 day period, labor and materials used on site will still be covered by the basic warranty, but the customer shall pay for all travel and living expenses incurred for any on-site service.

A maintenance contract may be purchased covering the period after the 90 days on-site warranty period, or after initial installation of the equipment. This is to be contracted through Canberra's Nuclear Systems Division.

REPAIRS

Any Canberra-manufactured instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. When returning instruments for repair, contact the Customer Service Department for shipping instructions and an Authorized Return Number (ARN).

All correspondence concerning repairs should include Model Number and a description of the problem observed.

Once repaired, all equipment passes through our normal pre-shipment checkout procedure. Return shipping expense on out-of-warranty repairs will be charged to the customer.

For instruments out of warranty, the customer must supply a purchase order number for the repair before the item will be returned to him.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping, If damage is found, immediately notify Canberra and the carrier making delivery, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in processing damage claims.

Due to the delicate nature of cooled detectors [Ge(Li) and Si(Li)] Canberra requires that delivery to and from air freight terminals be handled with special care. Do not ship such Detectors without first obtaining advice from our Traffic Department.

REVISION B
July 1, 1978

CONSTANT FRACTION TIMING SCA
MODEL 2035A

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Section 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The Canberra Model 2035A Constant Fraction Timing Single Channel Analyzer performs both energy and timing analysis on analog pulses from nuclear pulse shaping amplifiers. Energy analysis is derived by discrimination of the peak amplitude of the input energy pulses, and timing is derived by discrimination of a ratiometric constant fraction of the input pulse height.

The constant fraction technique of timing signal derivation provides a timing mark that is theoretically independent of precise pulse amplitude over a very wide range, assuming a uniform input pulse shape. This timing stability, as contrasted with the performance of an approach using a fixed amplitude reference at any level, provides the research laboratory user with an excellent tool for use in high resolution spectroscopy systems.

1.2 ENERGY ANALYSIS

The primary logic output (SCA) is provided as both positive and negative NIM-level pulses for each input analog pulse whose peak amplitude is between the levels determined by the front panel ten-turn dial controls. The pulse peak must exceed the LOWER LEVEL (E) reference, but not exceed the sum of the LOWER LEVEL (E) + WINDOW (Δ E) reference to generate the SCA output. Auxiliary positive-only outputs are generated as a Lower Level Discriminator (LLD) output for each input pulse which exceeds the LOWER LEVEL (E) reference regardless of its upper limit, and an Upper Level Discriminator (ULD) output only for each input pulse which exceeds the sum of the (E) + (Δ E) reference levels. Timing of each of these logic outputs is synchronous as derived by the constant fraction discriminator.

These multiple SCA, LLD and ULD outputs may be used separately or together as desired to assist in a wide variety of conventional applications from simple noise stripping to extraction of a narrow energy range from a wide spectrum for detailed spectroscopy, or timing spectroscopy on two energy levels simultaneously.

Energy discrimination in the Model 2035A is sharp, precise and stable. Temperature drift of the discrimination thresholds, for example, is less than $\pm$ 0.005%/^{o}C ($\pm$ 50 ppm/^{o}C) of full scale. The energy discriminators are DC coupled at the input to allow excellent baseline stability limited only by the shaping amplifier's restorer. These significant features permit excellent amplitude discrimination, even in high count rate spectra.

The LOWER LEVEL (E) threshold is calibrated by reference to the regulated NIM supply voltages, and is usable in a range from + .025 VDC to + 10.00 VDC. Linearity of control is limited only by the specified $\pm$ 0.25% maximum integral nonlinearity of the front panel dial potentiometer. A front panel mounted light emitting diode (LED) is useful in visually monitoring the setting of the LOWER LEVEL (E) reference above the shaping amplifier's noise level. The LED fires for the duration of the time the input exceeds the selected (E) threshold. Thus with a properly set threshold the LED will be on dimly, triggered only by valid input energy pulses.

The WINDOW (Δ E) threshold is also calibrated by reference to the regulated NIM supply voltages, and is usable in a range from the LOWER LEVEL (E) setting to + 10.0 VDC. A front panel Δ E RANGE switch allows use of a 1.0 volt full scale for very fine adjustments of a small energy window.

An external lower level discriminator input on the rear panel may be used in lieu of the front panel control for applications requiring a ratioed or sweeping baseline reference over the energy range. This input requires a positive voltage, and is linear over the full scale of 0 to + 10.0 VDC. A locking toggle switch on the rear panel is used to select this input.

1.3 TIMING ANALYSIS

The constant fraction timing discriminator in the Model 2035A operates on the difference signal between the normal input signal and a delayed facsimile. The zero crossing point of the algebraic composite signal occurs at a constant fractional ratio of the input pulse height and thus exhibits time stability. Three separate internal delay lines are used to insure optimum stability (minimum walk) over the specified range of input pulse shaping time constants used in the driving amplifier. A front panel INPUT SHAPING switch permits the user to select these delays according to the shaping time constant selected on the amplifier.

One important design feature of the Model 2035A is the pulse lockout (pile-up rejection) logic. First, internal gating prevents the timing cycle (including the front panel selected DELAY) from being initiated on events below the selected LLD threshold and thus minimizes dead time. Events recognized above the ULD are accepted and processed through the full timing cycle so that the ULD can provide timing data. Secondly, the lock-out logic rejects energy pulses which arrive after the first valid signal (i.e., above the LLD) but prior to reset at the end of a normal timing cycle. This prevents a second, possibly higher energy signal from changing the data latches and causing an erroneous output (timed to one event and energy gauged to a second). Thirdly, the lock-out logic prevents timing aberrations due to pileup by responding only to the next full event following a timing cycle instead of the potentially long tail of a pulse arriving at or near the end of one timing cycle. Lockout logic thus eliminates the most common ambiguities and assures the user of valid data outputs.

The pulse outputs may be delayed by up to 11μsec relative to a prompt output by use of the front panel linear DELAY control. Two ranges are provided: 0.1-1.1μsec and 1-11μsec. The selected delay and the output pulse width plus reset time determine the pulse pair resolution under any given circumstances. Optimum performance is about 800nsec unless a shorter positive output pulse is acceptable.

A GATE/STROBE input allows the user to gate the functioning of the Model 2035A or strobe the energy latches at a selected time. An internal jumper plug permits selection of function (gate, strobe, or normal). In gating, a positive logic level voltage is required to enable the unit. Outputs are then generated per normal constant-fraction timing. In strobing, output pulses are generated coincident with the leading edge of an applied positive logic voltage pulse. The output pulses will contain energy data only (no-timing) based upon the first input pulse processed after the preceding strobed output because of the lock-out logic discussed above.

1.4 OUTPUT OPTIONS

Positive output logic signals are adjustable in peak amplitude for compatability with interfacing instruments. The outputs are source-matched with 50 ohm series resistive terminations to prevent ringing due to reflections on unterminated cables, and the resulting multiple counting frequently experienced. The instrument is shipped with socketed resistors for each output which limit the output to + 5V nominal (open circuit) for direct interface with common TTL circuitry. The user may remove the resistors as desired to obtain a + 8V nominal open circuit voltage for instruments requiring the NIM pulse level, or + 4V nominal into the 50 ohm load termination which some other instruments provide. This flexibility allows the user to adapt the output signal to his needs without risking the problems encountered with improperly driven cables and critical timing pulses.

The negative SCA output is a NIM standard 16mA current pulse designed to yield a nominal - 800mV pulse across a 50 ohm load termination. Source matching here again guarantees a clean, stable pulse output even with a load mismatch, if that becomes desirable.

Careful attention has been paid to minimize reflections of the fast logic pulses onto the analog input. Thus all logic outputs are isolated from chassis to prevent circulating pulse currents in the instrument Bin.

Section 2
SPECIFICATIONS

2.1 INPUTS

SIGNAL INPUT	Accepts + 0.025 to + 10.0VDC, unipilor or bipolar (positive lobe leading) pulses from shaping amplifier. DC coupled. Input impedance 1K ohms. Shaping time constant range 0.1 to 10 microseconds. Front and rear panel BNC connectors. Front panel test point.
EXTERNAL LLD REFERENCE	Accepts 0 to + 10VDC as substitute for front panel LOWER LEVEL (E) control when selected by rear panel switch. Input impedance 1K ohms. Rear panel BNC.
GATE/STROBE	Accepts + 5VDC logic level. Function selected by internal jumper plug. Input impedance one TTL load, clamped to + 5V for overvoltages. Rear panel BNC.

2.2 OUTPUTS

SCA (+)	Positive logic + 5V nominal pulse amplitude. Output impedance 50 ohms. Pulse width 0.5 microseconds nominal; rise time and fall time less than 25 nanoseconds. Front and rear panel BNC's. Front panel test point.
SCA (-)	Negative logic - 16mA current pulse (current sinking). Output impedance 50 ohms. Pulse width 20 nanoseconds nominal; rise time less than 5 nanoseconds. Front panel BNC. Front panel test point.
ULD	Same characteristics as the SCA (+) output. Rear panel BNC.
LLD	Same characteristics as the SCA (+) output. Rear panel BNC.

2.3 PERFORMANCE

DISCRIMINATOR NONLINEARITY	Less than ± 0.25% of full scale for either LOWER LEVEL (E) or WINDOW (Δ E).
DISCRIMINATOR STABILITY	Better than ± 0.005%/°C (± 50 ppm/°C of full scale, referenced to NIM class A supply + 24.0VDC line.
DISCRIMINATOR RANGE	400:1 (0.025 to 10.0VDC).
DELAY NONLINEARITY	Less than ± 1% of full scale.

DELAY STABILITY

Better than ± 0.01%/°C (± 100ppm/°C) of delay range.

PULSE PAIR RESOLUTION

Limited by output pulse width (positive) plus delay selected, plus 200 nanoseconds cycle time. Minimum resolving time 800 nanoseconds (with 0.1 microsecond shaped input).

WALK

Referenced to a + 10.0V full scale unipolar input using 0.5 microsecond shaping:

DYNAMIC RANGE	WALK (MAXIMUM)
10:1	± 1 nanoseconds
50:1	± 2 nanoseconds
100:1	± 4 nanoseconds
200:1	± 6 nanoseconds

Walk beyond a 200:1 range is limited by jitter due to amplifier noise effects. In an operating system, detector and other electronic noise and other baseline anomalies may restrict the usable dynamic range in a given experimental setup to less than that given above.

2.4 CONNECTORS

All inputs and outputs are by BNC, type UG-1094/U connectors. Output connectors are isolated from chassis.

2.5 POWER REQUIREMENTS

+24VDC : 30mA
- 24VDC : 10mA
+12VDC : 145mA
- 12VDC : 55mA

2.6 PHYSICAL

SIZE

Standard single width Nuclear Instrument Module (NIM), (1.35 x 8.714 inches), (3.43 x 22.13 cm) per TID-20893 (rev).

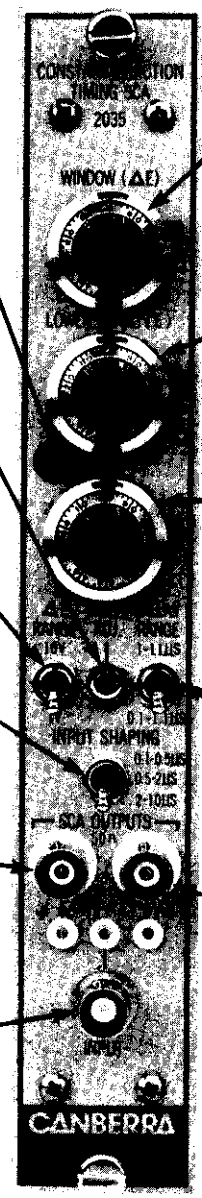
NET WEIGHT

Approximately 2.5 lbs. (1.15 kg).

Section 3
CONTROLS AND ADJUSTMENTS

This section describes the function of the controls, and the adjustments which the user can make, in the Model 2035 Constant Fraction Timing SCA. It is recommended that this section be read before proceeding with operation of the instrument.

3.1 FRONT PANEL



LIGHT EMITTING DIODE (LED)
Triggered while LLD threshold exceeded

WALK ADJ
Screwdriver trim potentiometer to adjust time walk

ΔE RANGE
Toggle switch to set full scale range of WINDOW (ΔE) control as 1.0 or 10.0VDC

INPUT SHAPING
Three position toggle switch to select internal delay line according to shaping time constant selected on amplifier

SCA OUTPUT (+)
Provides + 5V output pulse for each analog input pulse meeting SCA energy level requirements

INPUT
Accepts 0-10VDC peak pulses from nuclear pulse shaping amplifier for energy and timing analysis. Input impedance 1K ohms.

WINDOW (ΔE)
Ten turn locking dial potentiometer to set window width (upper discriminator threshold level, added to lower level). Scaled 0.0-10.0VDC

LOWER LEVEL (E)
Ten turn locking dial potentiometer to set lower discriminator threshold level. Scaled 0.0-10.0VDC

DELAY
Ten turn locking dial potentiometer to set delay between prompt timing point and desired output

DELAY RANGE
Toggle switch to set full range of DELAY control as 1.1 microseconds or 11 microseconds

SCA OUTPUT (-)
Provides - 16mA current pulse output for each analog input pulse meeting SCA energy level requirements.

3.2 REAR PANEL

ULD OUTPUT
Provides + 5V output pulse for each analog input pulse which exceeds sum of LOWER LEVEL (E) + WINDOW (Δ E) settings

SCA OUTPUT
Provides + 5V output pulse for each analog input pulse meeting SCA energy level requirements

GATE/STROBE
Accepts TTL level input to gate output (positive enable), or strobe (output on command) when selected by internal jumper plug

LLD REF MODE
Locking toggle switch to select front panel LOWER LEVEL (E) control (INT), or externally sourced voltage via adjacent BNC connector (EXT) for lower level reference

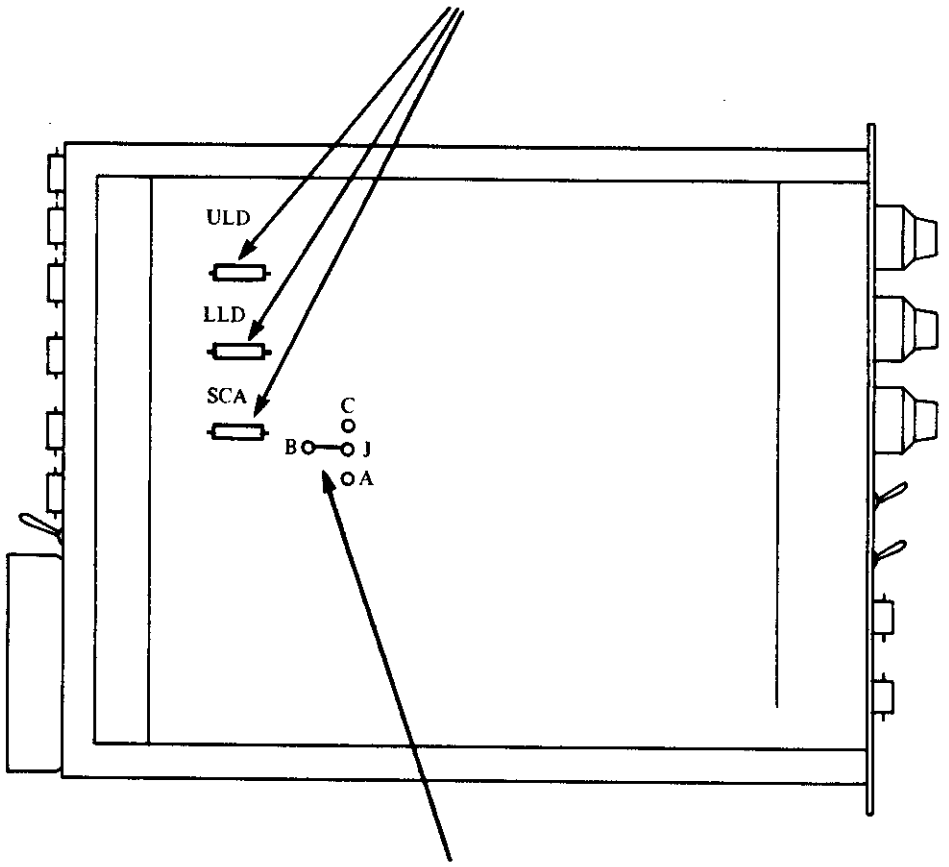
LLD OUTPUT
Provides + 5V output pulse for each input analog pulse which exceeds LOWER LEVEL (E) setting

INPUT
Accepts 0-10VDC positive analog pulses from shaping amplifier for energy and timing analysis

EXT. LLD REF.
Accepts 0-10VDC positive voltage reference to b e used in lieu of front panel LOWER LEVEL (E) control when selected by adjacent switch

3.3 INTERNAL

1.5K ohm resistors in sockets. Remove to raise output pulse amplitude.



GATE/STROBE/NORMAL JUMPER

J-A for GATE mode
J-B for NORMAL mode
J-C for STROBE mode

The trimming potentiometers internal to the instrument are carefully calibrated during factory test to provide the precise lower end and full scale limits for the front panel controls. The user should normally have no need to re-adjust these, but if adjustments are necessary the setup and general procedure given in Section 4 should be followed. The trimming functions are:

RV1:	Low end limit trim for WINDOW (Δ E)
RV2:	Transfer gain trim, LOWER LEVEL (E) to WINDOW (Δ E)
RV3:	High end limit trim for WINDOW (Δ E), 0-10V
RV4:	High end limit trim for WINDOW (Δ E), 0-1V
RV5:	Low end limit trim for LOWER LEVEL (E)
RV6:	High end limit trim for LOWER LEVEL (E)

The adjustment for output pulse voltage levels are made with the socketed 1.5K ohm resistors as illustrated. The upper resistor sets the ULD output pulse level, the middle resistor sets the LLD output pulse level, and the lower resistor sets the SCA output pulse level. With the resistors installed, the output pulse is clamped at + 5VDC nominal, open circuit. The user may remove any or all socketed resistors as needed. With the resistor removed, the output pulse voltage will be + 8VDC open circuit, and + 4VDC nominal into a 50 ohm load.

Section 4
OPERATING INSTRUCTIONS

The purpose of this section is to familiarize the user with the Model 2035A Constant Fraction Timing SCA, and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the unit will be used, explicit operating instructions cannot be given. However, if the following procedure is carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand. Additionally, if operating difficulties cause the user to suspect the proper functioning of the instrument at any time, this procedure will exercise the controls and operating modes such as to confirm proper functioning or to help isolate a malfunction.

4.1 DISCUSSION OF MEASUREMENT TECHNIQUES

There are two key measurements involved in checking the normal operation of a precision nuclear instrument such as the Model 2035A that can be distorted or even masked by improper measurement techniques: that setting the precise thresholds of energy discrimination, and that observing and/or trimming the time walk.

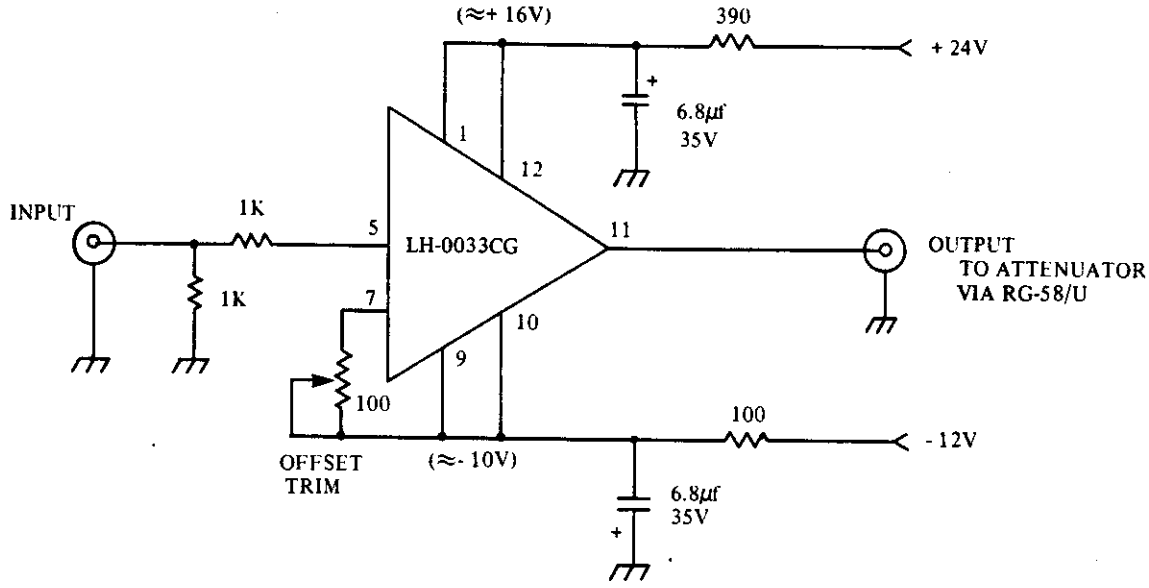
The upper and lower limits of the LOWER LEVEL (E) and WINDOW (Δ E) dial potentiometer ranges have been carefully calibrated in factory test. The precision of the examination to be described will be limited by the calibration of the user's oscilloscope. Hence, adjustments of the internal trimpots should not be attempted without a more exacting test technique. This examination will nonetheless familiarize the user with the operating range and the sharpness of discrimination and reveal malfunctions if they develop.

Regarding the walk measurements, the user must understand some subtle effects that will influence the apparent behavior of the instrument. First, when making a characterization of the instrument, the test signal amplitude must be constant at the output of the shaping amplifier and attenuation must be performed between the shaping amplifier output and the Timing SCA input. Without this simple precaution, the observed walk will include that of both amplifier and Timing SCA and the results will vary from amplifier to amplifier. The reason for this phenomenon is that the amplifier does exhibit some walk and a slight change in precise pulse shaping as the input signal amplitude changes because of slewing effects in the gain and pulse shaping stages. While the setup and trim of a complete system must absorb and compensate this effect by adjustment of the Timing SCA walk control, characterization or measurement of the walk of the Timing SCA itself is obviously distorted without such a procedural correction.

Secondly, the best attenuators for these precise timing measurements are 50 ohm attenuators, of either "T" or "π" configuration. Higher impedance attenuators (e.g., 93 ohm) do not demonstrate adequate band width and are observed to add up to a few nanoseconds of walk by themselves with various attenuation ratios. Acceptable 50 ohm attenuators include the Kay 430 series or equivalents with band widths of 1GHz or better. Precise terminations are highly recommended.

Thirdly, common nuclear shaping amplifiers are not rated to drive the required 10.0V or better output linearly to a 50 ohm load, and in fact demonstrate clipping and anomalies in pulse shaping due to loading effects on the loop gain of the output amplifier (which is commonly a final integrator).

This subtlety is induced by the attenuator impedance requirements and is not immediately apparent. Resolving this difficulty involves using a broad band buffer amplifier which will drive the 50 ohm attenuator. Such a circuit is fortunately available in the National Semiconductor LH-0033 CG. The circuit below illustrates one configuration that can be powered from the available NIM regulated power supply voltages, and has been found to yield excellent results.



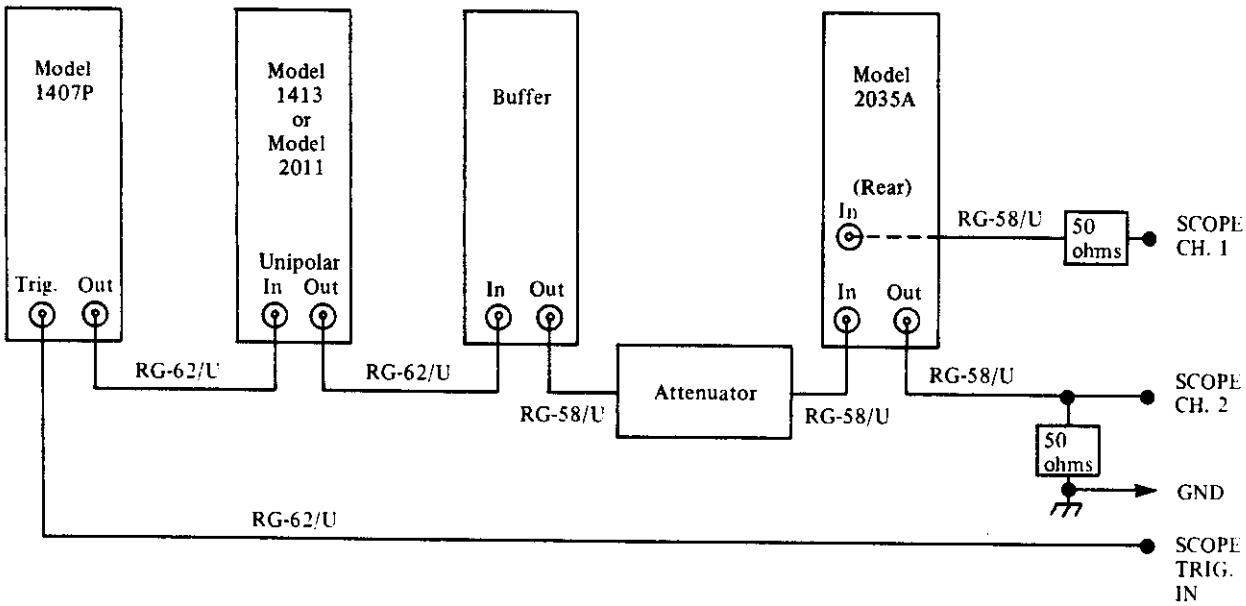
Using this procedure, the Timing SCA walk can be measured and trimmed properly. Extending the procedure, the user can then, of course, evaluate the relative walk behavior of several different amplifiers by substitution.

4.2 INITIAL SETUP

In order to perform the bench checkout procedure detailed below, the following equipment (or equivalents) will be required:

Canberra Model 2000 Bin/Power Supply
Canberra Model 1407P Pulse Pair Generator
Canberra Model 1413 or 2011 Spectroscopy Amplifier
Calibrated dual trace 100MHz oscilloscope (Tektronix 454, 475, etc.)
Attenuator, 50 ohm (Kay 432D, etc.)
Terminators, 50 ohm BNC

Install the Model 2035A, 1413 or 2011, and 1407P in the Bin with the power initially OFF.

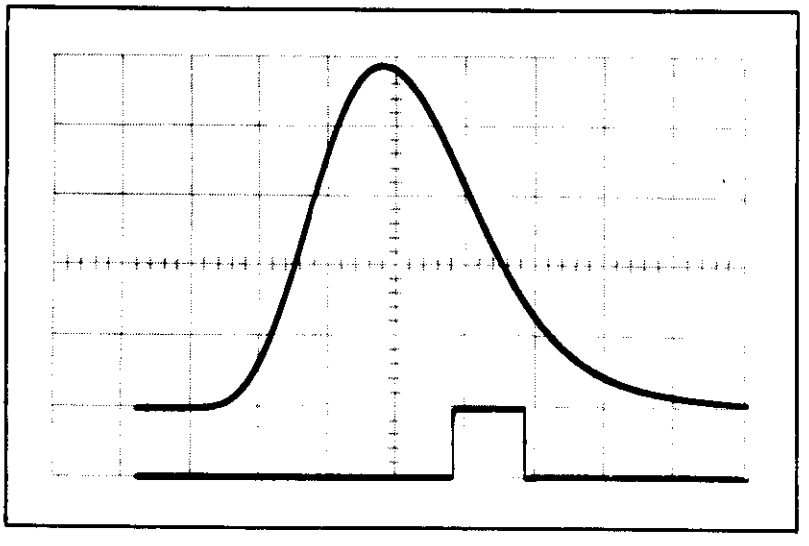


Reference control settings:

Model 1407P	RATE: Variable full CW Range 1-10kHz AMPLITUDES: full CW MODE: dual pulse ATTENUATION: out
Model 1413	* COARSE GAIN: x 30 * FINE GAIN: (see below) * SHAPING: 0.5μsec * POLARITY: positive RANGE: 10V RESTORER: low *for Model 2011
Model 2035A	WINDOW (Δ E): 10.0 LOWER LEVEL (E): 0.0 DELAY: 1.0 Δ E RANGE: 10V DELAY RANGE: 0.1-1.1μsec INPUT SHAPING: 0.1-0.5μsec LLD REF MODE (rear panel): INT
ATTENUATOR	All switches out
SCOPE	Channel 1: 2V/div Channel 2: 5V/div Time base: 1μsec/div, externally triggered

4.3 INITIAL CHECKOUT

Apply power to the Bin, and increase the amplifier output (FINE GAIN control) slowly to 10V peak, or just below the threshold of extinguishing the SCA output pulse as shown in the photo below. (NOTE: It is advisable for the user to verify that the Bin voltages are correct: ± 12.0VDC and ± 24.0VDC).



1. Now apply 6 dB attenuation to the input signal, and adjust the WINDOW (Δ E) control to display 1.0. The SCA output pulse will be extinguished.

2. Increase the LOWER LEVEL (E) (rotate the control clockwise) until the SCA output pulse just reappears. The LOWER LEVEL (E) control dial should now display 4.00 ± 0.03. If the threshold is beyond these limits, the source of error may be in the DC level at the amplifier output or the 10V full scale level set above.

3. Now increase the setting of the LOWER LEVEL (E) control again until the SCA pulse extinguishes. The LOWER LEVEL (E) control dial should now display 5.00 ± .03.

4. Change the Δ E RANGE switch to 1V. Reduce the setting of the LOWER LEVEL (E) control to about 4.5 and raise it again slowly until the SCA output pulse just reappears. Now the control dial should display 4.90 ± 0.03.

5. Now again increase the setting of the LOWER LEVEL (E) control until the SCA pulse extinguishes. The LOWER LEVEL (E) control dial should not display 5.00 ± .03.

   These tests demonstrate the functioning of the two discriminator thresholds in determining a wide or narrow window SCA logic output.

6. To verify operation of the ULD and LLD outputs move the cable presently at the front panel + SCA output to the rear panel BNC as desired. With the present setup, the ULD output pulse will be present for all settings of the LOWER LEVEL (E) control up to a dial display of 4.90 ± 0.03, or any combination of LOWER LEVEL (E) and WINDOW (Δ E) adding up to 5.00 maximum. The LLD output pulse will be present for all settings of the LOWER LEVEL (E) control below 5.00 ± 0.03, and is not influenced by any setting of the WINDOW (Δ E) control.

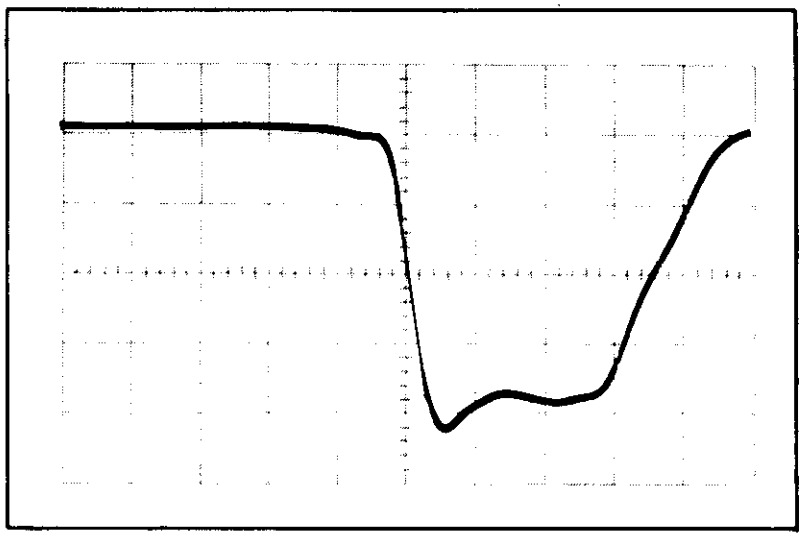
   As the Model 2035A has been carefully calibrated in factory test, the precision of this casual examination is limited by the calibration of the user's oscilloscope. The instrument may be exercised over its full rated range with this setup if the user wishes, but adjustments of internal trimpots should not be attempted without a more exacting test technique.

7. For walk evaluation, it is best to view the fast leading edge of the - SCA front panel output. A 50 ohm termination should be added at the scope input connector.

   The cable connections illustrated above, and the terminations as shown, are particularly important when attempting to observe the walk characteristics of the instrument. If the input signal is not monitored connect the 50 ohm terminator at the rear panel INPUT connector when the TSCA is driven at its front panel INPUT. Reflections from improperly terminated cables change the shaped pulse significantly enough to cause timing distortions by altering the constant fraction ratio.

   Best viewing of the - SCA output pulse may be had by selecting channel 2 display only, with the leading edge centered in the scope graticule. Use the delayed, expanded sweep mode to obtain a display time base of 5nsec/div. Time walk is now seen as a movement of the leading edge leftward (-) or rightward (+) as the input signal is attentuated.

   Set the front panel LOWER LEVEL (E) dial control to its counterclockwise minimum, and the WINDOW (Δ E) dial control to its clockwise maximum. Remove the 6 dB attenuation step applied earlier, and center the leading edge of the - SCA pulse in the display as shown below.

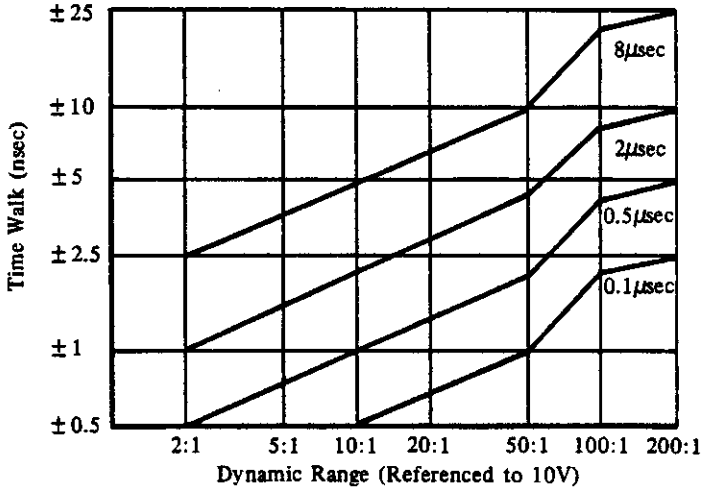


Apply a 6 dB (x2) attenuation step, and verify the walk to be less than ± 1nsec from center. Adjust the front panel WALK ADJustment potentiometer if necessary.

Next successively add or change to 20 dB (x10), 34 dB (x50) and 40 dB (x100) attenuation. Walk should be within ± 2, ± 4 and ± 8nsec respectively. With careful setup, the user should also be able to verify walk less than ± 10nsec from 0 to 46 dB (x200) attenuation, although minor adjustment of the WALK ADJustment potentiometer may again be necessary.

The user may note that if he adjusts the walk to be 0 at the end points (e.g., at 0 and 40 dB attenuation), the walk behavior at intermediate steps should still be within the specified limits (e.g., less than ± 8nsec). With proper setup and the specified equipment, the walk is typically less than 1/2 the guaranteed limits and is progressive with attenuation.

The walk behavior of the Model 2035A for other than 0.5μsec shaping used in this test is illustrated in the chart below.



The user should realize that at longer shapings, the effects of noise and slower pulse risetimes will cause more uncertainty in precise discrimination and therefore cause jitter in the output timing. Higher amplifier gain settings likewise are responsible for jitter aggravation which may limit the usable dynamic range to somewhat less than the capability of the instrument.

8. The use of the DELAY control and the DELAY RANGE switch on the front panel are straightforward. All logic outputs of the Model 2035A are synchronous and are therefore affected equally by the selected delay. The delay may be demonstrated by using the delayed sweep mode on the oscilloscope and lining up the leading edge of the output being observed with the left end graticule of the scope face, with the DELAY control set to minimum. Clockwise rotation of the dial will add a delay (the trace now moves to the right) linearly proportional to the dial setting for its 0.1-1.1 range.

4.4 APPLICATION SUGGESTIONS

TIME WALK

The initial checkout procedure detailed above examines the time walk behavior of the Timing SCA by maintaining a constant signal level in the amplifier. When the instrument is used in a typical spectroscopy system, of course, this is not the case, and the walk behavior of the amplifier must now be compensated for best experimental results. The user must again be cautioned in attempting this adjustment: the capacitive input characteristic of the pulse shaping amplifier will cause serious time walk errors when the attenuator drives the amplifier. The subtlety here is that the output impedance of the attenuator, when driven by a low source impedance, changes with attenuation and leads to pulse shape aberrations in the amplifier.

Correct procedure suggests that the attenuator (again it must be a 50 ohm type) be placed between a pulse source and the detector preamplifier test input, with that input padded to present a 50 ohm net resistive load impedance to the attenuator. The preamplifier then presents a fixed output impedance to the amplifier, and the various sources of walk can then be best compensated together. Again to minimize jitter effects, it is advisable to use as high a test signal level as can be handled linearly in the preamplifier.

Recognizing these details which influence proper alignment, the knowledgeable user can achieve best timing performance with a minimum of setup effort, using either an oscilloscope directly or a Multi-Channel Analyzer as his needs dictate.

TROUBLE-SHOOTING

The initial checkout procedure detailed above provides an adequate check of the basic functioning of the instrument. If after performing the checkout, the user cannot obtain the expected outputs, he should:

a) with an oscilloscope on the front panel test point, check that the input sisignal is received properly, is of sufficient amplitude and DC base;

b) verify that the rear panel LLD REF MODE switch is set as intended (INT to use the front panel control);

c) verify that the LOWER LEVEL (E) and WINDOW (Δ E) dial controls are set as intended;

d) verify that the Δ E RANGE switch is set as intended;

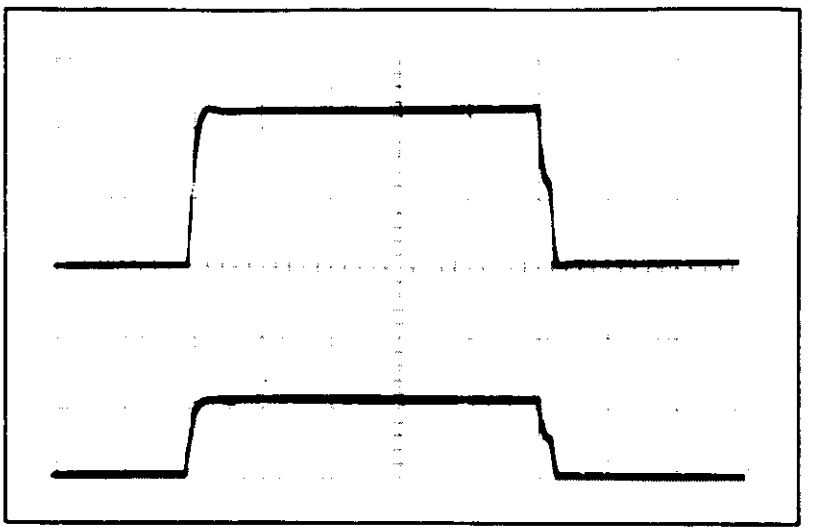
e) verify that the INPUT SHAPING switch is set to agree with the shaping selected on the Amplifier.

Most difficulties are related to the user's unfamiliarity with the functions and ranges of the instrument's controls.

4.5 REFERENCE DATA ON CABLES

The following photos depict a typical output pulse at the load end of the designated RG-58/U cable and the same point using RG-62 cable. In each case the photographs illustrate high impedance (1K ohm) and 50 ohm termination conditions. Clearly the fastest, cleanest pulse is realized with the RG-58/U cable. With the source match provided, loading effects are limited to amplitude changes only. RG-58/U cable is therefore recommended for best compatibility with the LLD, ULD and SCA outputs.

RG - 58 Cable with Rs = 50 ohms

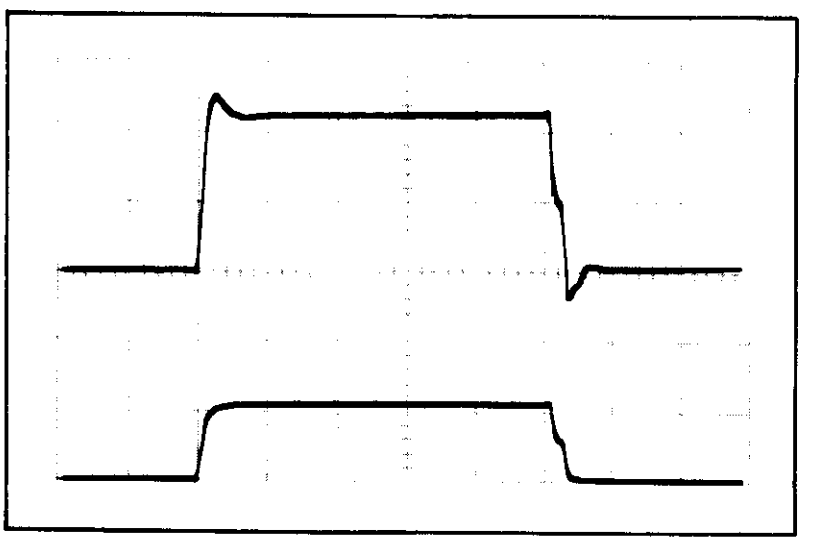


R_L = 1K ohms

R_L = 50 ohms

Horiz: 0.1μsec

RG - 62 Cable with Rs = 50 ohms



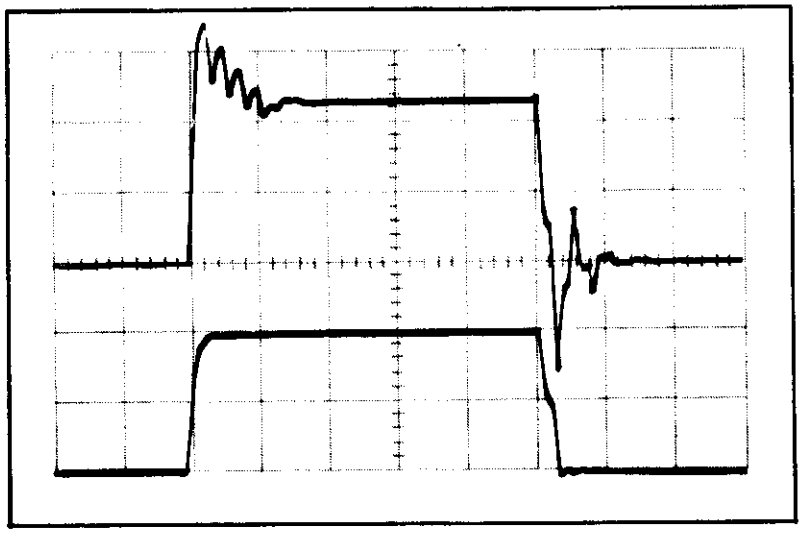
R_L = 1K ohms

R_L = 50 ohms

Horiz: 0.1μsec

The picture below illustrates the same pulses with a source mismatch caused by driving the cables with the transistor switches directly. The waveforms indicate how important and effective source matching is in eliminating instabilities which cause phenomena such as multiple counting or triggering. For this reason the Model 2035 provides source matched outputs, and load end terminations are not necessary.

RG - 58 or RG - 62 Cable Driven Directly



R_L = 1K ohms

R_L = 50 ohms

Horiz: 0.1μsec

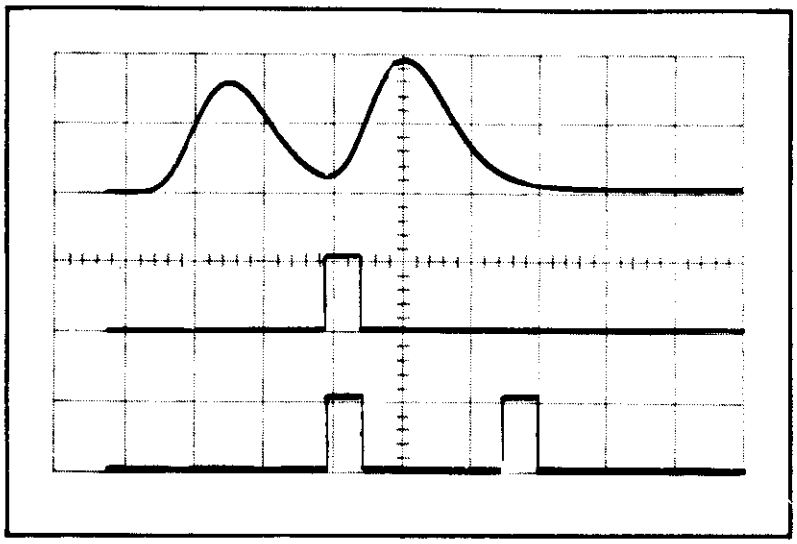
Section 5
THEORY OF OPERATION

The Model 2035A Constant Fraction Timing SCA analyzes nuclear energy pulses from spectroscopy amplifiers by comparing the peak voltage levels of those input pulses against stable D.C. reference voltages set by the instrument's front panel controls. Comparisons are made for a lower level discrimination (LLD) and an upper level discrimination (ULD). Pulses whose peak amplitude lies between the two levels (i.e., within the window) are recognized as the primary or SCA output. The Model 2035A provide all 3 outputs (ULD, LLD, and SCA) at a time referenced to a discrimination point that is derived as a constant fraction of the input pulse amplitude. This technique makes the timing of the output logic signals essentially insensitive to variations in the precise amplitude of the input signal.

Pulse energy discrimination takes place in the precision dual comparator A6. The LLD output is taken at A6 pin 7, which yields a negative (logic low) pulse whose width represents the time span in which the input signal exceeds the reference voltages set by the LOWER LEVEL (E) front panel control acting thru buffer amplifier A9. The front panel LED display is switched on by this pulse via Q14. The leading edge of this LLD pulse sets the LLD latch formed by A3a and A3b. As the latch is set, its $\overline{Q}$ output on A3 pin 3 is used to set 2 additional latches: one enables the ULD gate at A1 pin 9, and the other enables the timing comparator. This logic scheme allows the ULD and timing comparator to respond to only the first full pulse applied, and rejects any succeeding pulse arriving before the end of the analysis cycle to follow. This is a form of pileup rejection logic which prevents ambiguous timing information at the outputs.

The photograph below illustrates the operation of this logic with a representative piled up pulse in which the second pulse is of a lower energy than the first, and where the output pulse is set for minimum delay. The upper trace shows the input pulse waveform (a typical 0.5μsec shaped pulse pair) and the middle trace shows a single output. Here the discrimination is based upon the first lobe, and the second lobe is rejected for analysis because the LOWER LEVEL (E) was set to minimum, and the second lobe began before the first had recovered to the baseline. Using a higher setting of the LOWER LEVEL (E) control, the user can make the circuitry recognize the second lobe as a valid energy pulse despite the distorted energy peak due to pileup and improve the apparent pulse pair resolution. The lower trace then shows the output from this condition, a set of pulses each keyed to the constant fraction timing point.

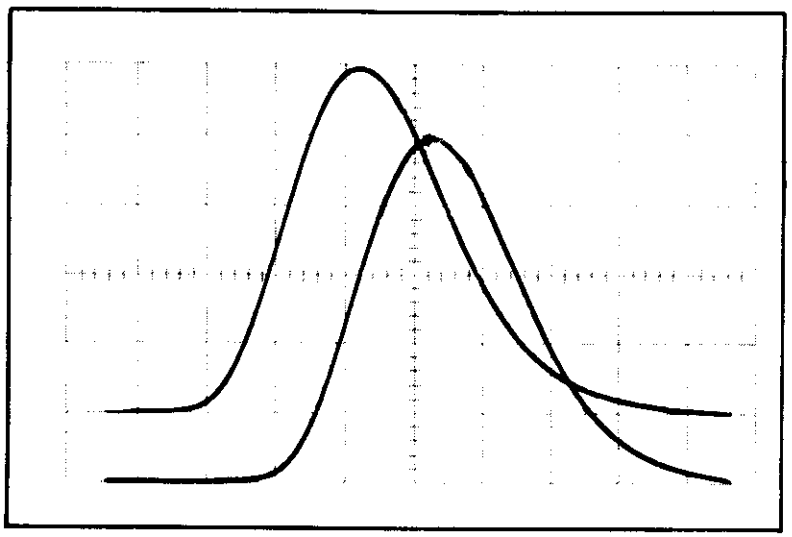
The photograph below illustrates another pileup condition in which the second lobe is higher than the first and the output pulse is delayed. Here the middle trace shows pileup rejection based upon the second lobe arriving during the analysis cycle of the first lobe, as well as being above the LOWER LEVEL (E). The lower trace shows how the second lobe is marginally accepted for analysis based upon the LOWER LEVEL (E) threshold being raised just above the valley between the peaks. Note that the use of the delayed output compromises the pulse pair resolution even for non-piled up pulses.

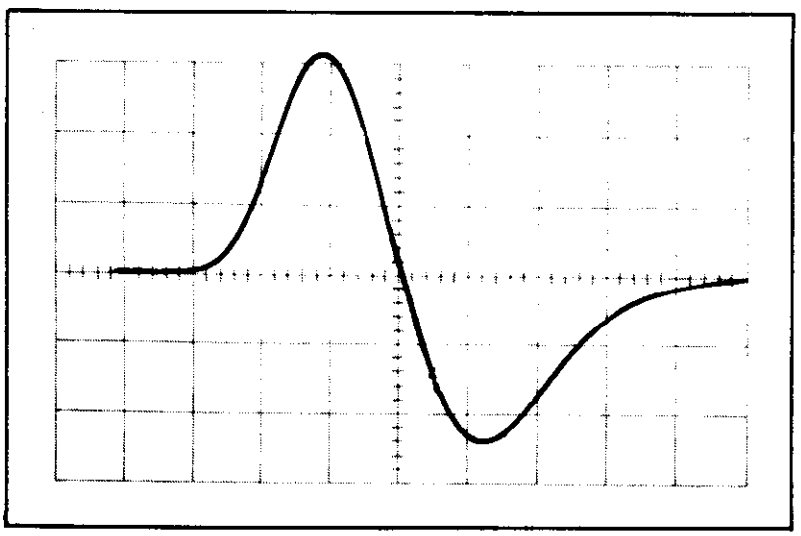


The ULD output is taken at A6 pin 12, which yields a positive logic pulse whose width represents the time span in which the input signal may exceed the reference voltage provided by A8. The latter is a summing amplifier which forms the ULD reference from the sum of the LOWER LEVEL (E) and WINDOW (Δ E) control settings. The gating at A1 pins 9 and 10 allows a ULD trigger pulse to set the ULD latch formed by A1a and A1b only during the time span of the first LLD pulse: the enable at A1 pin 9 is removed at the end of the first LLD pulse seen at A6 pin 7 because the end of the latter resets the latch via A1d.

The contents of the LLD and ULD latches are held until interrogated later in the analysis cycle.

The second latch set by the LLD latch, and used as the enable for the timing comparator, is formed in A4c and A4d. The Q output at A4 pin 11 is tied to the gate input of A11 at pin 4. The comparator A11 operates on the difference signal between the input pulse (as buffered thru Q13) and a delayed facsimile generated by the delay line section selected. The difference signal itself appears as a bipolar waveform, the zero crossing point of which is constant with variations of input signal (constant fraction) and thus forms a stable time reference point. The set of photographs below indicate the waveforms evident at the inputs to A11 from the normal and delayed pulses, and the difference waveform.





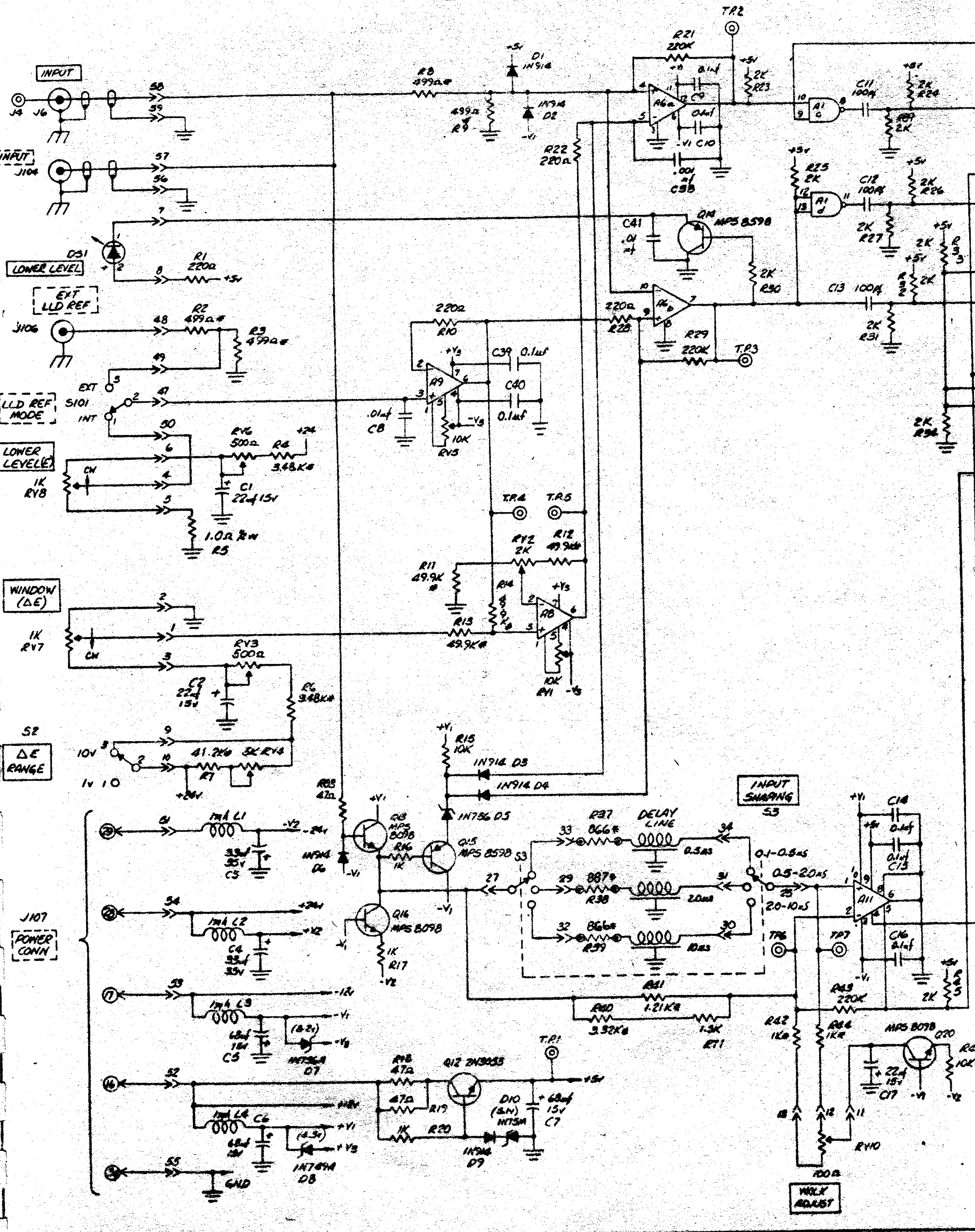
The comparator $\overline{Q}$ output on A11 pin 5 is used to reset the enable latch at A4 pin 9 so that again successive pulses or noise introduced at the input prior to completion of the analysis cycle underway do not cause erroneous multiple outputs, or affect the timing processes for the desired signal. The reset of the comparator enable signal is therefore used to trigger the delay one-shot A7. The delay provided covers 2 ranges: 0.1-1.1μsec, and 1-11μsec, each referenced to the $\overline{Q}$ output of the timing comparator A11.

At the end of the delay time, a second one-shot is initiated (A5 pin 13). This one-shot is set for 0.5μsec to interrogate the LLD and ULD latches and form the synchronous output for LLD, ULD and SCA as gated thru A2. As the 0.5μsec nominal pulse terminates, the reset one-shot at A5 pin 12 is generated. This logic low pulse is nominally 0.1μsec wide, and is used to reset the LLD and ULD latches (A3 pin 1, and A1 pin 1 respectively), thereby completing the analysis timing cycle.

A5 pin 2 is brought out as a gate control: held low via the jumper J-A and an external signal on the GATE/STROBE input, it blocks firing of the 0.5μsec one-shot and thus inhibits the output. A5 pin 3 is brought out via the jumper J-C for strobed mode: pulsed release of a low on the above input line allows momentary firing of the one-shot.

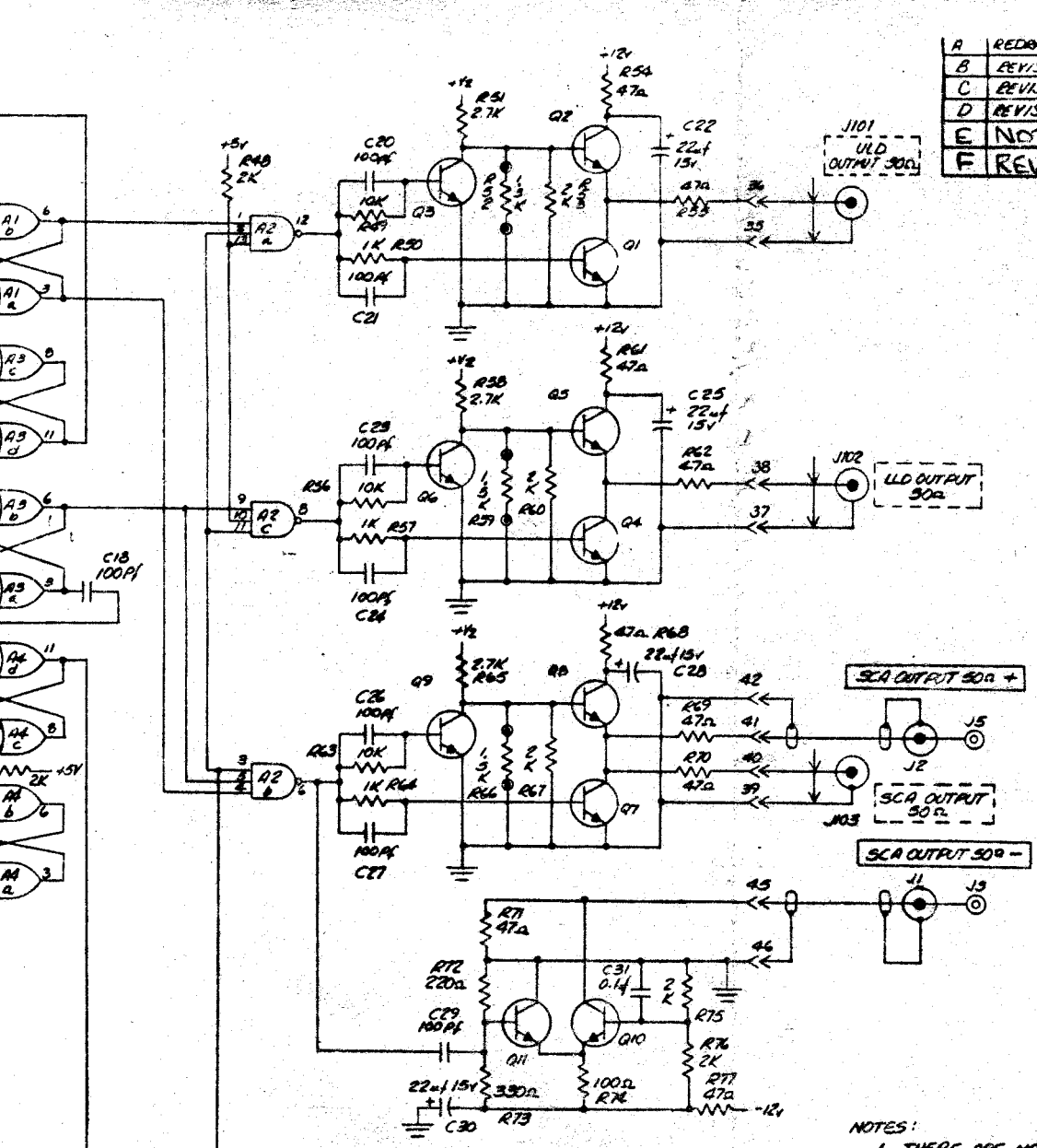
The LLD, ULD and + SCA outputs are provided as positive logic outputs whose amplitude is individually adjustable by use of socketed resistors, and whose pulse width is set by the interrogate pulse at A5 pin 13. The circuit is a variant on the standard totem pole configuration. When the gate at A2 pin 6, e.g., goes low, Q7 and Q9 are cut off, and Q8 sources the output pulse.

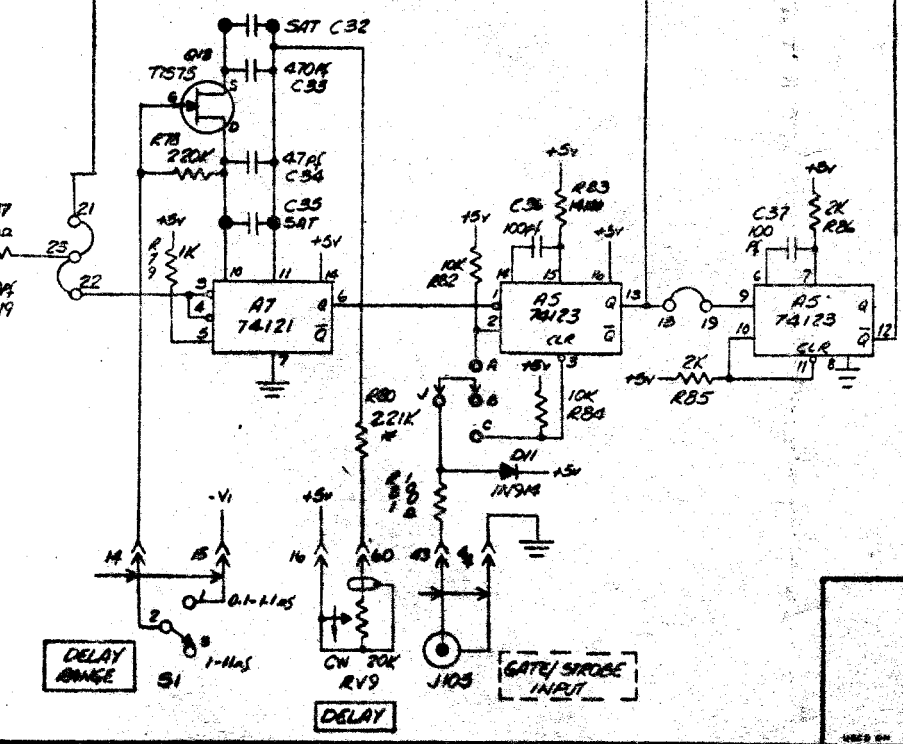
The - SCA output is derived by differentiating the start of the + SCA drive pulse for 20nsec. The output circuit is a current steering differential amplifier with Q11 biased on and Q10 cut off. The input negative pulse at A2 pin 6 is differentiated (C24) to cut off Q11 and allow Q10 to sink a measured 16mA.



INPUT
J4
J6
INPUT
J104
LOWER LEVEL
DS1
R1
220Ω
EXT
LLD REF
J106
R2
499Ω
R3
499Ω
EXT
LLD REF MODE
S101
INT
LOWER LEVEL(E)
1K
RV8
RV6
500Ω
R4
3.48K
C1
22uf 15v
1.0Ω
R5
WINDOW (ΔE)
1K
RV7
RV3
500Ω
C2
R6
3.48K
S2
ΔE RANGE
10V
1V
41.2K
5K RV4
R7
+24V
J107
POWER CONN
1mH L1
C3
1mH L2
C4
1mH L3
C5
1N756A
D7
1mH L4
C6
1N759A
D8
GND
R8
499Ω
D1
1N914
1N914
D2
R9
R21
220K
T.P.2
R23
2K
A6a
C9
0.1uf
C10
R22
220Ω
.001
C58
C41
.01
Q14
MPS 8598
R30
2K
A6b
220Ω
R28
R29
220K
T.P.3
220Ω
R10
A9
C39
0.1uf
C40
0.1uf
.01uf
C8
10K
RV5
T.P.4
T.P.5
RV2
2K
R12
49.9K
R11
49.9K
R14
A8
R13
49.9K
10K
RV1
R15
10K
1N914 D3
1N914 D4
1N756 D5
R65
47Ω
Q8
MPS 8098
1N914
D6
R16
1K
Q15
MPS 8598
Q16
MPS 8098
1K
R17
INPUT SHAPING
S3
R37
866
DELAY LINE
0.5ns
0.1-0.5ns
0.5-2.0ns
2.0-10ns
R38
2.0ns
R39
10ns
TP6
TP7
R41
1.21K
R40
3.32K
1.5K
RT1
R42
1K
R44
1K
R43
220K
T.P.1
Q12 2N3055
R18
47Ω
47Ω
R19
1K
R20
1N914
D9
D10
C7
15v
+5v
A11
C14
C15
C16
C17
Q20
MPS 8098
RV10
100Ω
WALK ADJUST
A1
C11
100pf
R24
2K
2K
C12
100pf
R25
2K
R26
2K
R27
C13
100pf
R31
2K
R33
2K
R34
2K

A	REDRAWN- WAS C-16360		MMC	12-9-76
B	REVISED		RNB	12/14/2
C	REVISED		RNB	1-2-77
D	REVISED - INT. RELEASE	1420	RNB	1-24-77
E	NOTE 10 ADDED	2619	J.C.	5-8-78
F	REVISED - ECN	6582	J.C.	8-14-78





I.C. REFERENCE CHART	
I.C. - TYPE - OPEN GATE	
A1	7400
A2	7410
A3	7400
A4	7400
A5	74123
A6	LM319
A7	74121
A8	72741
A9	72741
A10	DELETED
A11	LM361

LAST REFERENCE CHART	
INTEGRATED CIRCUITS	- A11
RESISTORS	- R87
CAPACITORS	- C41
DIODES	- D11
TRANSISTOR	- Q20
TEST POINTS	- T.P. 5
CONNECTORS - FRONT PNL	- J6
REAR PNL	- J107
VARIABLE RESISTORS	- RV10
LIGHTS	- DS1
SWITCHES - FRONT PNL	- S3
REAR PNL	- S101
THERMISTOR	RT1
INDUCTORS	L4

NOTES:

1. THERE ARE NO FOUR WAY TIES ON THIS SCHEMATIC.
2. →31 INDICATES WIRING POINT ON P.C. BOARD.
3. ALL UNMARKED TRANSISTORS ARE 2N3646.
4. 3 — 6 INDICATES WIRE POINTS USED AS JUMPERS.
5. ⑥ INDICATES PIN ON POWER CONN. w/ PIN NUMBER.
6. # INDICATES RNC60 RESISTORS.
7. ▭ INDICATES FRONT PANEL COMPONENT LOCATION.
8. ▭ INDICATES REAR PANEL COMPONENT LOCATION.
9. INDICATES TWISTED PAIR.

DRAWN	M.M.C.	12-9-76	SCHEMATIC CONSTANT FRACTION TIMING SCA MODEL 2095	CENTRONIC MERIDEN CONN.
ENGR		1-21-77		
CHK'D		1-24-77		
RELEASED				
USED ON			DO NOT TEMPLATE DRAWING	B-16360 F