TIME ANALYZER

Model 1443

Instruction Manual

CANBERRA INDUSTRIES, INC.
45 Gracey Avenue
Meriden, Connecticut 06450

Telephone: (203) 238-2351

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Section 1

INTRODUCTION

The Canberra Model 1443 Time Analyzer performs accurate time-to-amplitude conversion with subsequent single channel analysis of the resultant time spectrum. It offers unmatched flexibility for coincidence spectra applications, eliminating additional gating modules. Optimum time resolution can be obtained over a wide dynamic range when the Model 1443 is combined with the Model 1426 Extrapolated Zero Strobe.

The time-to-amplitude converter is used to analyze correlations between random nuclear events that occur within a selected interval of time. Output pulse amplitude is proportional to the time difference between an accepted Start and Stop input. Rectangular in appearance, the unipolar TAC output is essentially flat topped with very little droop for accurate measurement by a multichannel analyzer. Time resolution better than 0.01% of full range is obtainable for any time range (50, 100, 200, 500, and 1000 nanoseconds). Internal gating logic prevents a TAC output for: (1) overrange Start or Stop signals, (2) Stop signals prior to an accepted Start, (3) Start-Stop signals during the converter busy time.

Linear gating (coincidence or anticoincidence) of the TAC output is available to eliminate from spectra unwanted events not meeting imposed energy or timing restrictions. Essentially pedestal free, all converted pulses are passed without degrading amplitude information.

The versatility of the Time Analyzer is enhanced with its inhibit input capability. Upon receipt of a positive pulse or DC level at the front panel Reset/Inhibit Input connector, TAC reset is initiated and subsequent Start input signals are inhibited for its duration. A rear panel Stop Inhibit Range adjustment allows rejection of Stop input signals from 50 nanoseconds up to 100% of any selected TAC time range.

Valid Start and Valid Stop logic outputs are generated for each accepted Start and Stop input, respectively. The Valid Start output duration represents the converter busy time which is equal to the time interval between an accepted Start input and the end of TAC reset time. Converter reset occurs after generation of a TAC output, upon receipt of a Reset/Inhibit input, or at overrange (no Stop input received within selected time range).

The single channel analyzer section of the Model 1443 places timing restrictions on the time spectrum being accumulated and is useful in reducing the number of chance coincidences. A selectable 0 to 100% "time window" (i.e., time region within selected time range) is established with the front panel ten-turn Time and Δ Time controls. An SCA output is produced for every TAC output pulse amplitude greater than the Time dial setting but less than the sum of Time plus Δ Time settings. SCA timing jitter is nonexistent because its output is gated in time coincidence with the TAC output.

Both the TAC and SCA outputs are simultaneously adjustable in width (0.5 to 5 microseconds) and delay time (1 to 10 microseconds). The output delay time is referenced from either an accepted Start or Stop input according to the position of the front panel Output Timing switch.

DC coupled circuitry is incorporated in the Time Analyzer to ensure its count rate independence. The TAC output must be fed into the DC coupled input of a multichannel analyzer such as the Model 8100 for optimum high count rate performance. A front panel Period output supplies the necessary logic information to enable DC operation of many MCA's. Selectable TAC output polarity and full range output amplitude of 3, 5, or 10 volts guarantees maximum MCA compatiblity.

Section 2

SPECIFICATIONS

2.1 INPUTS

START

Polarity: accepts standard negative fast NIM logic signal, minimum amplitude ≈ -250 mV (± 100 V max.)
Pulse width: 2 nanoseconds, minimum
Input impedance: 50 ohms, DC coupled; leading edge initiates time conversion; succeeding Start Input signals are accepted only after the end of the converter busy time; front panel BNC connector

STOP

input specifications identical to Start Input; a TAC Output is generated only if an accepted Stop signal follows an accepted Start signal within the selected TAC Time Range

GATE

Polarity: accepts positive logic signal or DC level; amplitude ⩾ +3V (± 20V max.)
Width: ⩾ 100 nanoseconds
Input impedance: ≈ 1k ohms, DC coupled; provides external means of gating the TAC Output with Coincidence/Anticoincidence gated mode of operation; Gate Input must occur within Output Delay time period; front panel BNC connector

RESET/INHIB

Polarity: accepts positive logic signal or DC level; amplitude ⩾ +3V (± 100V max.)
Width: ⩾ 100 nanoseconds
Input impedance: ≈ 2k ohms; DC coupled; serves as anticoincidence Start Input gate; leading edge initiates TAC reset; enables acceptance of new Start Input signals after its time interval or after the internal reset time (whichever is greater); front panel BNC connector

2.2 OUTPUTS

TAC

Polarity: provides positive or negative flat topped rectangular unipolar pulse; constant pulse shape independent of Time Range or amplitude; amplitude proportional to accepted Start/Stop Input pulse time difference; selectable 3V, 5V, or 10V full scale Time Range amplitude
Delay: adjustable (1 to 10 microseconds)
Width: 0.5 to 5 microseconds
Rise time: ≈ 500 nanoseconds
Output impedance: < 1 ohm (front panel), < 93 ohms (rear panel), DC coupled; BNC connectors

VALID START (Converter Busy Time)	Polarity: provides positve 5V logic signal for each accepted Start Input Rise and fall time: ⩽ 25 nanoseconds Output impedance: < 25 ohms, DC coupled Duration: equal to time interval between accepted Start Input and end of reset time; front panel BNC connector
SCA	Polarity: provides positive 5V logic signal Rise and fall time: ⩽ 25 nanoseconds Output impedance: < 25 ohms, DC coupled; leading edge in time coincidence with TAC Output Duration: equal to TAC Output; an SCA Output is generated for every TAC Output occurring within a selectable 0 to 100% time window (i.e., time region within selected TAC Time Range) established with the Time and Δ Time controls; front panel BNC connector
PERIOD	Polarity: provides positive 5V logic signal Rise and fall time: ⩽ 25 nanoseconds Output impedance: < 25 ohms; DC coupled; leading edge in time coincidence with TAC Output Duration: equal to TAC Output, enables DC coupled operation of many multichannel analyzers requiring a second (coincidence) input; rear panel BNC connector
STOP INHIBIT MONITOR	Polarity: provides positive 3V logic signal; leading edge can be delayed from 50 nanoseconds to 100% of selected TAC Time Range Rise and fall time: < 25 nanoseconds Output impedance: 50 ohms, DC coupled; provides observation of Stop Inhibit Range adjustment; rear panel BNC connector

2.3 PERFORMANCE

TIME RESOLUTION	< 7 psec FWHM on 50 nanosecond Time Range: < 0.01% of full range for all higher ranges
TAC INTEGRAL NONLINEARITY	⩽ ± 0.1% from 15 nanoseconds to full range on 50 nanosecond and 100 nanosecond Time Ranges; ⩽ ± 0.1% from 10% to 100% of full range for all higher ranges
TAC DIFFERENTIAL NONLINEARITY	⩽ ± 2% from 15 nanoseconds to full range on 50 nanosecond and 100 nanosecond Time Ranges; ⩽ ± 2% from 10% to 100% of full range for all higher ranges
SCA TIME/Δ TIME INTEGRAL NONLINEARITY	⩽ ± 0.5% of full scale
TAC OUTPUT TEMPERATURE STABILITY	⩽ ±10 psec/°C for 50 nanosecond Time Range; ⩽ ± 0.01%/°C for all higher ranges

SCA TIME/ΔTIME TEMPERATURE STABILITY	⩽ ± 0.01%/°C of full scale
OUTPUT DELAY TEMPERATURE STABILITY	⩽ ± 0.6%/°C
OUTPUT WIDTH TEMPERATURE STABILITY	⩽ ± 0.6%/°C
TEMPERATURE OPERATING RANGE	0 to +50°C ambient
TAC OUTPUT DROOP	⩽ 8 psec/microsecond of Output Delay on 50 nanosecond Time Range; ⩽ 0.015%/microsecond of Output Delay on all higher ranges
TAC TIME RANGES	50, 100, 200, 500, and 1000 nanoseconds full scale, switch selectable; 10 volt full scale ramp amplitude; full scale calibration ⩽ ± 5%
TAC RESET TIME	fixed 2 microsecond recovery time; occurs after each TAC Output pulse, upon receipt of a Reset/Inhibit input or at overrange (no Stop input within selected TAC Time range)
GATE PEDESTAL	essentially zero pedestal, factory calibrated
SCA OUTPUT TIME WALK	none, with respect to TAC Output
MINIMUM CONVERSION TIME	≈ 15 nanoseconds, equal to circuit propagation delays
COUNT RATE CAPABILITY	all inputs and outputs are DC coupled for optimum count rate independence; maximum internal count rate is limited by the converter busy time (time interval between accepted Start Input and end of reset time)
INTERNAL GATING LOGIC	prevents TAC Output for: (1) overrange Start or Stop signals; (2) Stop signals prior to an accepted Start; (3) Start-Stop Inputs during converter busy time (eliminates pulse pileup)

2.4 CONNECTORS

START, STOP, GATE, RESET/ INHIB	front panel, BNC, UG-1094/U
TAC, SCA, VALID START, VALID STOP	front panel, BNC, UG-1094/U
TAC (Z = 93 Ω), PERIOD, STOP INHIBIT, MONITOR	rear panel, BNC, UG-1094/U

2.5 POWER REQUIREMENTS

+24V	–	160mA
+12V	–	340mA
- 24V	–	100mA
- 12V	–	225mA

2.6 PHYSICAL

SIZE	AEC standard double-width NIM module (2.70 x 8.714 inches) per TID-20893 (Rev).
WEIGHT	2.8 lb (1.3 kg.)

Section 3

CONTROLS AND CONNECTORS

3.1 GENERAL

This section describes the functions of the controls and connectors located on the front panel, rear panel, and inside of the Model 1443 Time Analyzer.

Complete understanding of the purpose of the various controls is essential for the proper operation of the Model 1443, and it is recommended that this section be read before proceeding with the operation of the module.

3.2 FRONT PANEL

RANGE
Selects TAC full scale conversion time; 5 ranges 50, 100, 200, 500, and 1000 nsec. Maximum full scale conversion amplitude, 10 volts.

GATE MODE
Selects COINCidence or ANTIcoincidence gate mode of operation; output is enabled (COINC) or inhibited (ANTI) upon receipt of a positive gate input signal (pulse or DC level) any time during the Output Delay time period.

TIME
Selects time from 0 to 100% of selected TAC range. Establishes minimum time restrictions for SCA output.

GATE
Accepts positive logic signal or DC ⩾+3 volts (max. 20V); width ⩾100nsec; input Z, 1k ohms, DC coupled. Provides external means of gating the TAC output with Coincidence or Anticoincidence gated mode of operation. Gate Input must occur within Output Delay time period.

RESET/INHIB
Accepts positive logic signal or DC ⩾+3V (±100V max.) width ⩾100 nsec; input Z ≈2k ohms, DC coupled. Resets the TAC conversion time and inhibits acceptance of new Start Input signals for the duration of the signal applied.

START
Accepts negative signals ⩾-250mV (±100 V max.), width ⩾2 nsec. Input Z = 50 ohms, DC coupled. Starts time conversion and enables stop input.

STOP
Specification identical to Start Input. A TAC output is generated if the accepted Stop signal follows an accepted Start pulse within the selected TAC Range time.

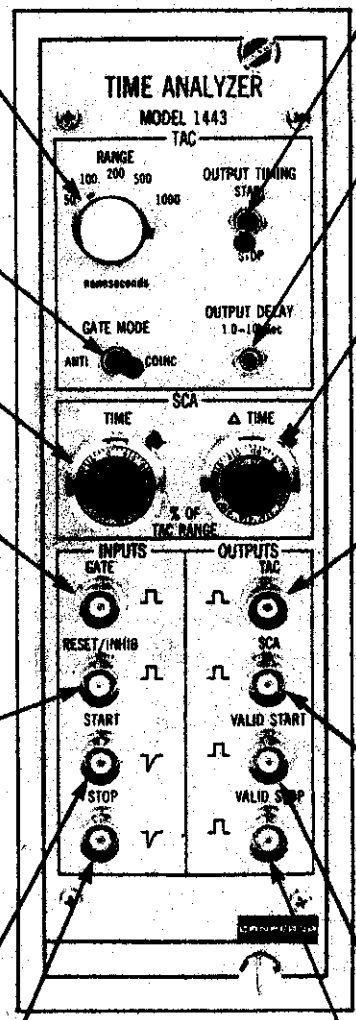


Figure 3-1.
Front Panel Controls
Model 1443.

OUTPUT TIMING
Selects whether TAC Output Delay is timed from an accepted Start or Stop input.

OUTPUT DELAY
Provides an adjustable TAC output delay time from 1.0 to 10 microseconds; timed from an accepted Start or Stop input, according to Output Timing switch selection.

ΔTIME
Selects time window width from 0 to 100% of selected TAC Range time; establishes maximum time restrictions for SCA. SCA output is generated whenever a TAC output signal is above the TIME setting and within the ΔTIME window setting.

TAC
Provides delayed (1 to 10 microsecond) positive or negative unipolar pulse with an amplitude proportional to the Start/Stop input time difference; selectable 3V, 5V, or 10V full range amplitude; adjustable width 0.5 to 5 microseconds (factory set at 2.0 microseconds); rise time ≈500 nsec; Z_O <1 ohm, DC coupled.

SCA
Positive 5 volt logic signal; rise and fall time ⩽25 nsec; Z_O <25 ohms, DC coupled; time coincidence with TAC output; width same as TAC output. Occurs whenever TAC output is above time setting and within the Δ Time window setting.

VALID START
Specification identical to SCA output; duration equal to conversion time + output delay + TAC output width + reset time.

VALID STOP
Specification identical to SCA output; duration equal to time interval between accepted stop input and beginning of reset time.

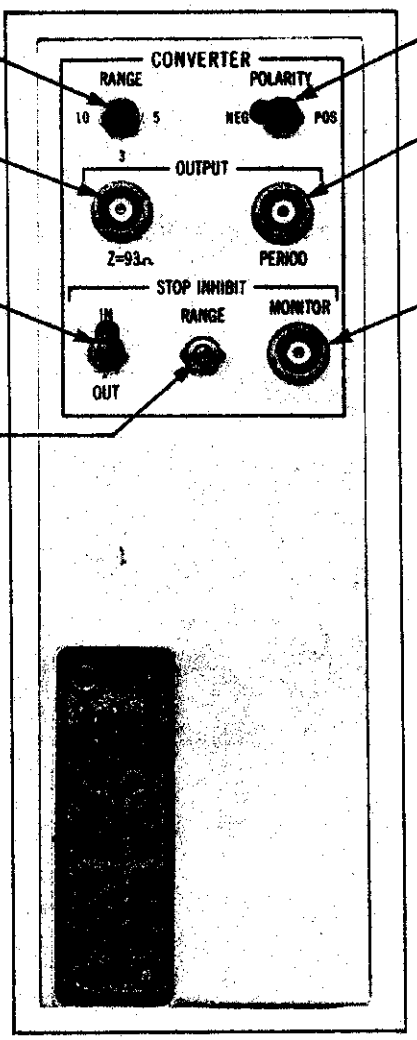
3.3 REAR PANEL

RANGE
Selects full range for TAC output amplitude; 3V, 5V, or 10V, available.

Z = 93 Ω
Identical to TAC output except Z = 93 ohms; for impedance matching of 93 ohm cable.

STOP INHIBIT
Enables (IN) or disables (OUT) Stop Inhibit Range adjustment from functioning.

RANGE
Provides a means to inhibit acceptance of Stop input signals from 50 nsec. to 100% of selected TAC Range time.



POLARITY
Selects either a POSitive or NEGative TAC output.

PERIOD
Positive 5 volt logic signal; rise and fall time $\leq$25 nsec; Z_o <25 ohms, DC coupled; leading edge in time coincidence with TAC output; duration equal to TAC output.

MONITOR
Positive 3 volt logic signal; rise and fall time $\leq$25 nsec; Z_o = 50 ohms, DC coupled; provides observation of Stop Inhibit Range adjustment time.

Figure 3-2. Rear Panel, Model 1443.

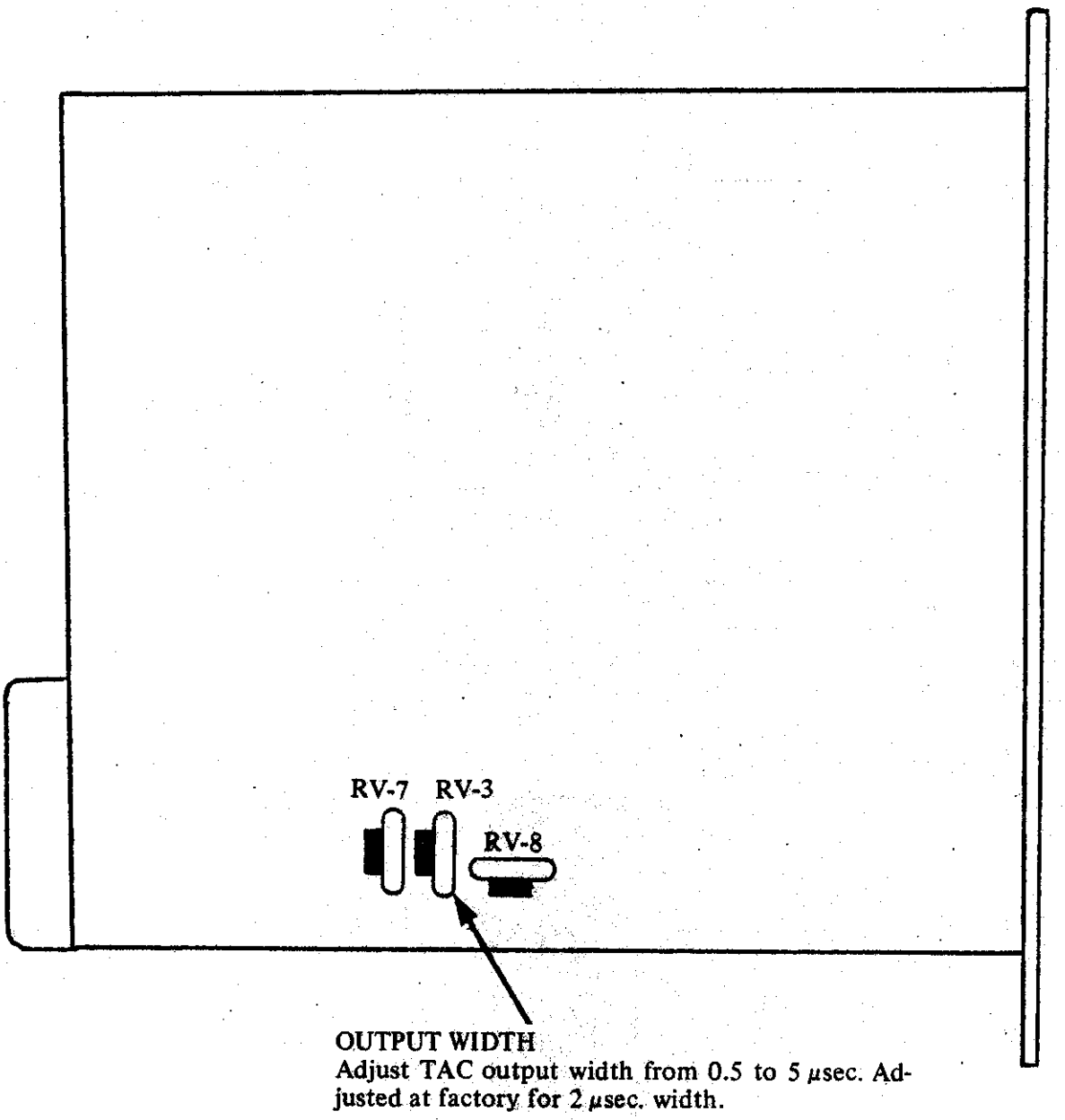


Figure 3-3. Internal Controls, Model 1443.

Section 4

OPERATING INSTRUCTIONS

4.1 GENERAL

The purpose of this section is to familiarize the user with the operation of the Model 1443 Time Analyzer and to check that the unit is functioning correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

4.2 INITIAL SETUP

4.2.1 REQUIRED EQUIPMENT

In order to perform the checkout procedures in this section, the following equipment will be required in addition to the Model 1443:

One Canberra Model 1407 Reference Pulse Generator (or equivalent)

One Canberra Model 1455A Logic Shaper and Delay (or equivalent)

Delay – any means of providing a negative pulse that is delayed from the Model 1455A output by a known period of time. Examples: Model 1458 Nanosecond Delay Module, Model 1455 or 1455A Logic Shaper and Delay Module, or a long piece of coaxial cable (93 ohm RG-62U cable or 50 ohm RG-58U cable = approximately 1.6 nanoseconds per foot).

4.2.2 SETUP

1. Insert the Model 1407, 1443, and 1455A modules in AEC compatible base unit/power supply such as the Canberra Model 1400. Interconnect and set the controls as in setup diagram (Figure 4-1).

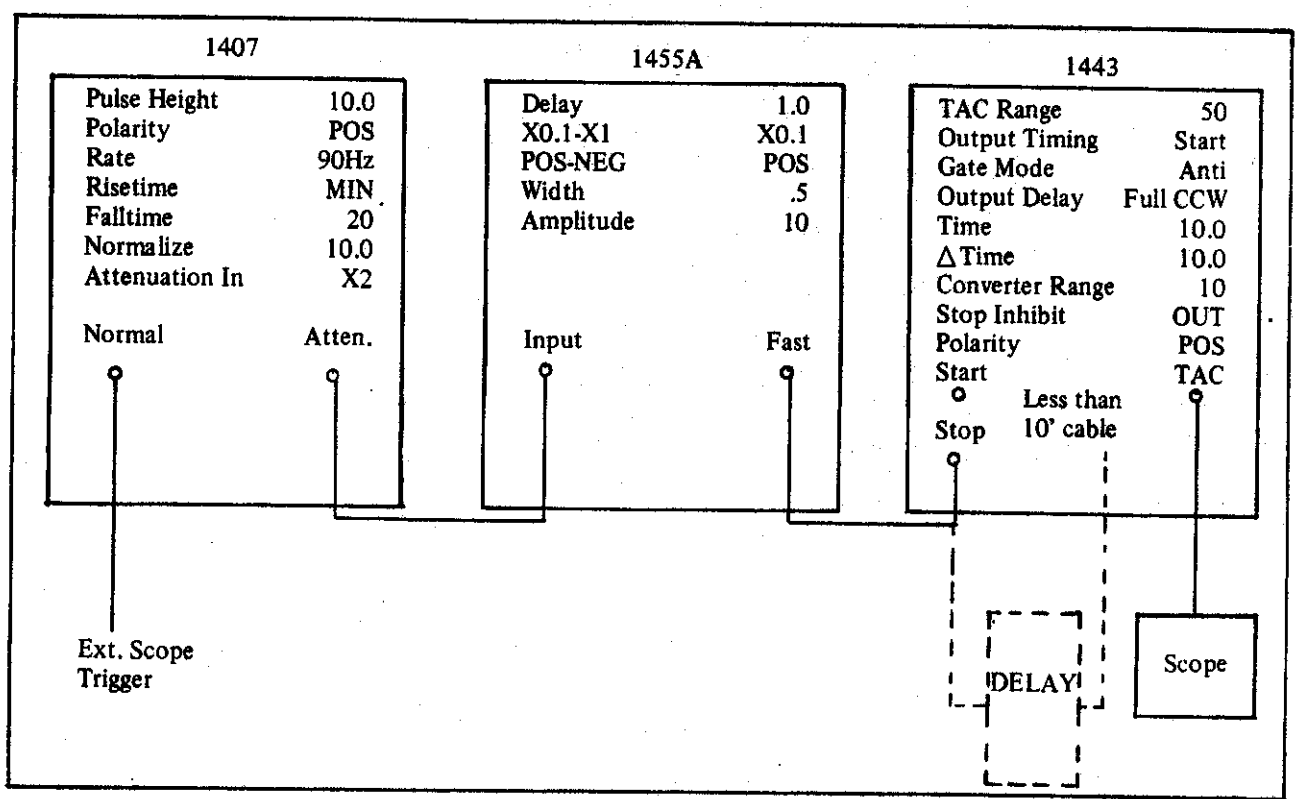


Figure 4-1. Set-up Diagram, Model 1443.

2. Turn on power switch. The Model 1407 should have approximately +5 volt tail pulse at the ATTN. OUTPUT. The Model 1455A should have a standard negative NIM logic signal at the FAST OUTPUT delayed from the leading edge of the Model 1407 tail pulse by 100 nanoseconds. The START and STOP INPUTS on the Model 1443 should be interconnected by a cable less than 10 feet.

4.3 INITIAL CHECKOUT

1. Observe the TAC OUTPUT. A ≈ +3 volt, unipolar pulse, 2 microseconds wide should appear with a rise time of ≈ 500 nanoseconds.

2. Remove the cable connection between the START and STOP input and insert a known delay greater than 15 nanoseconds (min. conversion time) between the START and STOP input. If the delay is greater than the selected TAC RANGE, an over-range will occur and no TAC OUTPUT will appear. Select a TAC RANGE in which the known delay period falls. Notice the TAC OUTPUT amplitude is directly proportional to the time difference between the START and STOP INPUT of the Model 1443.

3. Using known delays, check the other TAC RANGEs of the Model 1443. Set the delay to yield a +10 volt TAC OUTPUT. Change the CONVERTER POLARITY to NEG; a -10 volt TAC OUTPUT should be present. Return to POS. Change the CONVERTER RANGE to 5; a +5 volt TAC OUTPUT should be present. Changing the CONVERTER RANGE to 3 yields 3 volt TAC OUTPUT. Return CONVERTER RANGE to 10.

4. Observe the VALID START OUTPUT; a +5 volt logic signal should be present that starts at the leading edge of the START INPUT and ends ≈ 2 microseconds after the TAC OUTPUT.

5. Observe the VALID STOP OUTPUT; a +5 volt logic signal should be present that starts at the leading edge of the STOP INPUT and ends at the trailing edge of the TAC OUTPUT.

6. Observe the PERIOD OUTPUT; a +5 volt logic signal should be present that is in Coincidence with the TAC OUTPUT.

7. Observe the Z = 93 ohms OUTPUT; it is identical to the TAC OUTPUT except that its

8. Observe the STOP INHIBIT MONITOR output; place the STOP INHIBIT RANGE adjustment to mid point and set the STOP INHIBIT switch to IN. Change the delay between START and STOP to cause the STOP INPUT to occur during the STOP INHIBIT MONITOR (inhibits when MONITOR is low) time period. Notice that no TAC OUTPUT appears at this point. If the delay is increased so that the STOP INPUT appears after the STOP INHIBIT MONITOR, the TAC OUTPUT will reappear. To increase the STOP INHIBIT time, turn the STOP INHIBIT RANGE CW. Return the STOP INHIBIT switch to the OUT position.

9. Observe the TAC OUTPUT; increase the delay to yield a 5 volt TAC OUTPUT. Change the OUTPUT TIMING from START to STOP. Notice the TAC OUTPUT is delayed by the difference between the START and STOP inputs. This is because all timing is now started from the STOP input instead of from the START input. Return to START OUTPUT TIMING. Now adjust the OUTPUT DELAY Potentiometer CW and observe that the TAC OUTPUT can be delayed up to 10 microseconds. Return fully CCW.

10. Observe the TAC OUTPUT (+5 volt signal) and the SCA OUTPUT; decrease the TIME control to 40% (4.0). An SCA OUTPUT should be present (Δ TIME at 10.0); a 5 volt logic signal that is in coincidence with the TAC OUTPUT. Decrease the Δ TIME until the SCA OUTPUT just disappears. Δ TIME should be 1.0±.05 (TAC OUTPUT must be 5.0 volts). Increase Δ TIME to 20% (2.0) and increase TIME until the SCA OUTPUT can just disappear; it should be 5.0±.05. Notice TIME and Δ TIME are expressed in % of TAC RANGE.

11. Connect the POS OUTPUT of the Model 1455A through a variable delay to the GATE INPUT of the Model 1443. If the GATE INPUT pulse occurs during the OUTPUT DELAY period of the Model 1443 and the GATE MODE is ANTI, no TAC OUTPUT will appear. With the condition the same as above, changing the GATE MODE to COINC will cause the TAC OUTPUT to reappear. If the GATE INPUT does not occur during the Model 1443 OUTPUT DELAY period, the opposite will occur. Notice this input provides a means of gating the TAC OUTPUT either in a Coincidence or Anticoincidence mode of operation. Return GATE MODE to ANTI and disconnect the GATE INPUT. The TAC OUTPUT should be present.

12. Connect the GATE signal to the RESET/INHIB INPUT. This pulse will perform two functions. It will prevent the START INPUT and will reset the Model 1443 for the duration of the input pulse.

4.4 LIVE SYSTEM APPLICATION

1. Setup system as in Figure 4-2. Apply power to the P.M. Tube, Ge(Li) Detector and all modules.

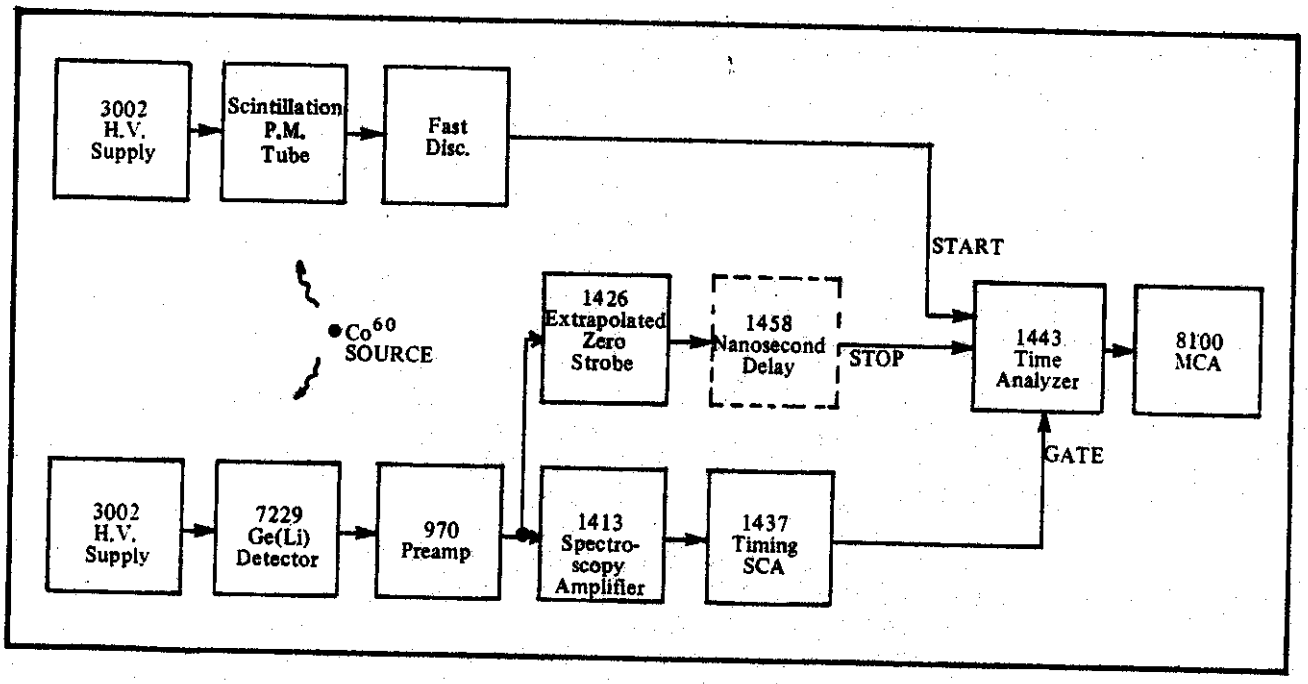


Figure 4-2. System Setup, Block Diagram.

2. Set the Model 1413 controls as follows:

DELAY (Internal)	OUT
RANGE	10V
DC LEVEL	0V
OUTPUT POLARITY	POS
RESTORER	LO (adjust POLE/ZERO - RESTORER OFF)
INPUT POLARITY	POS
SHAPING	1 microsecond

Adjust the GAIN so that the 1.33 MeV energy peak of the Co^{60} is at approximately +6.5 volts. Connect the UNIPOLAR OUTPUT to the Model 1437 INPUT.

3. Set the Model 1437 controls as follows:

SCA - DISC sw.	SCA
LE - CO sw.	LE
DELAY	0
BASELINE	1
WINDOW	10

Observing the POS OUTPUT adjust the RT pot so that the output pulse occurs just after the peak of the INPUT. Note: Output width should be at .5 microsecond (internal adjustment). Now increase the BASELINE until it is set just below the 1.17 MeV energy peak of the Co^{60}. Decrease the WINDOW until it is set just above the 1.33 MeV energy peak. These settings can be accomplished by triggering the scope externally from the SCA OUTPUT pulse and observing the Model 1413 OUTPUT on the oscilloscope. Now connect the POS OUTPUT of the Model 1437 to the GATE INPUT of the Model 1443.

4. Set the Model 1426 controls as follows:

PREAMP SIGNAL	POS

Adjust the THRESHOLD just above the noise level and connect the FAST OUTPUT through the Model 1458 to the STOP INPUT of the Model 1443. (The Model 1458 should have 20 nanoseconds of DELAY IN).

5. Set the FAST DISC as follows:

WIDTH	approximately 10 nanoseconds
THRESHOLD	just above the noise level

Connect the Fast Negative Output to the START INPUT of the Model 1443.

6. Set the Model 1443 controls as follows:

OUTPUT TIMING	START
GATE MODE	COINC
CONVERTER RANGE	10
CONVERTER POLARITY	POS
STOP INHIBIT	OUT
TAC RANGE	1000 nanoseconds

Now adjust the OUTPUT DELAY until the GATE INPUT signal occurs during the Delay period of the Model 1443. At this point a TAC OUTPUT should be present. Adjust the TAC RANGE until the TAC OUTPUT is between 4 to 8 volts. Connect to MCA and collect data. Note the peak channel of accumulated spectrum. Add 10 nanoseconds of DELAY IN to the Model 1458 and collect data again. Note the peak channel. The time calibration of the MCA now becomes:

$$\text{nanosecond/channel} = \frac{\text{peak channel \#2 - peak channel \#1}}{\text{10 nsec (add to 1458 DELAY)}}$$

This calibration will remain constant unless the TAC is changed.

Section 5

THEORY OF OPERATION

5.1 GENERAL

The Model 1443 Time Analyzer performs time to amplitude conversion. The output pulse amplitude is proportional to the time difference between the Start and Stop Inputs. Also provided is a means of gating the TAC output either in a coincidence or anticoincidence mode of operation. The Reset/Inhibit Input initiates a TAC reset and Start Input inhibit, while the Stop Inhibit provides an adjustable means of rejecting a Stop Input signal. The Single Channel Analyzer (SCA) section provides a selectable 0 to 100% "time window" (time between the TIME and Δ TIME selected) via the front panel TIME and Δ TIME settings.

The Model 1443 consists of start input, start input control, ramp circuit, high Z amplifier, linear gate, output amplifier, stop input, reset/inhibit, logic circuitry, gate input, over-range, stop inhibit, period output, valid stop, valid start, and SCA. A timing sequence (Figure 5-1) and block diagram (Figure 5-2) are provided at the end of this description. Also refer to the schematic diagram.

5.2 START INPUT

This circuit causes tunnel diode D3 to change from its low voltage state to its high voltage state (≈ - 0.5 volts) when Start Input signal exceeds - 250 millivolts: the tunnel diode will remain in this state until a reset signal from reset monostable or the Reset/Inhibit Input is furnished. Diodes D1, resistor R1 and Q3 form a voltage limiter, to limit the base voltage at Q1 to 700 millivolts for Start Input signals up to 100 volts. Q1 and Q2 amplify the Start Input signal and cause tunnel D3 to switch state.

5.3 START INPUT CONTROL

The Start Input Control provides three functions; first, it provides a signal to the Valid Start. next it removes the Ramp current source clamp, and also enables the Stop Input. These functions all occur when the base of Q4 goes to - .5 volts (tunnel diode D3 changes to a high state).

5.4 RAMP CIRCUIT

The Ramp Circuit provides a linear ramp voltage when the Start Input signal exceeds the threshold level. This causes the Ramp Current Source Clamp Q8 to be turned off and the Ramp Current Source Q26 to charge capacitor C33 at a rate selected by the Range switch. Because the voltage at the base of Q8 is limited to about -3.6 volts, the maximum voltage towards which the capacitor will be charged is limited to -3.6 volts through the Ramp Current Source ground reference Q9, Q10, which references C33 to zero.

Assuming that no Stop Input signal is received within the selected time range, the Over-Range Disc will fire when the ramp reaches a - 3 volts, causing the Start Circuit to be reset, and no output pulse will be generated.

5.5 HIGH Z AMPLIFIER

The High Z Amplifier is a unity gain amplifier with a high input impedance that presents the ramp from the ramp generator to the output amplifier, Over-Range Disc., Stop Inhibit Disc and the SCA. RV-1 is used to set the amplifier output to zero.

The Linear Gate allows a portion of the ramp signal to be fed to the output amplifier if all conditions are met in the logic circuitry. When the Gate Driver (Q60) signal is negative, all transistors (Q44-Q47) are saturated. The input to the operational amplifier is attenuated by 1000:1 or greater by the input resistors and the on resistance of the transistors. If the gate driver signal goes to ground, the gate transistors are turned off and signal is fed to the output amplifier. RV-6 is used to balance the input.

5.7 OUTPUT AMPLIFIER

This amplifier presents to the TAC output a portion of the ramp voltage proportional to the time between the Start and Stop inputs.

The output amplifier is a basic closed loop amplifier. A differential dual transistor (Q48) is located at the input for temperature stability. Located in the emitter of Q48 is a current source (Q49) used to provide a constant current and a high input impedance. The output of Q48 is then fed to a voltage gain stage (Q50, Q51) which in turn feeds a source follower, Q52. This then feeds a pair of complementary transistors (Q53, Q54) which provide fast switching and a low impedance for the output. The output is then fed back to the input through a resistor to provide a fixed gain. At the input to the amplifier is located a three position range switch, a polarity switch, and the linear gate.

The range switch does nothing more than change the input resistance to the amplifier, thereby changing the overall gain of the amplifier. This switch provides three output ranges of 10, 5, and 3 volts.

The polarity switch takes the output of the ramp generator and feeds it either to the inverting or non-inverting input of the amplifier. Thus, a negative or positive signal can be obtained at the output depending on the polarity selected.

5.8 STOP INPUT

This circuit is identical to the Start Input Disc and will fire tunnel diode D6 when the input exceeds - 250 millivolts. Assuming a Start Input has been received the Stop Clamp (Q19) is cut off (no Stop/Inhibit signal). Then the Stop Input will switch the Ramp Current Source Control (Q20, Q21) causing the Ramp Generator to stop charging the capacitor C33. At this point, the capacitor will hold its charge voltage until the Start Input is reset. Thus, at the capacitor C33, we have a voltage that is proportional to the difference in time between the Start and Stop input. This voltage is then fed through the High Z Amplifier, Linear Gate, and Output Amplifier to the TAC output. The Stop Input Disc also provides a signal to the Valid Stop Buffer.

5.9 RESET/INHIBIT

The Reset/Inhibit Disc provides a means of resetting the Start Input and all the other circuitry. To initiate this process, the Reset/Inhibit input must exceed +2 volts at which point the start clamp (Q16) will reset the Start Input discriminator and Q64 will present a pulse to the other logic circuitry causing it to be reset. As soon as the Reset/Inhibit signal falls below ±2 volts the Start Input is ready to receive a valid input signal.

5.10 LOGIC CIRCUITRY

This circuit processes the Start and Stop input and generates a pulse with variable delay and width to the Linear Gate located at the input of the output amplifier. This provides a means of delaying the TAC output and varying its width. This circuitry also prevents the TAC output from occurring, and resets the Start and Stop inputs.

The Start or the Stop input will initiate the delay monostable depending upon the output timing mode selected. The width of the delay monostable is variable via the front panel output delay pot from 1 to 10 microseconds. Assuming no gate input, at the end of the delay pulse, the width monostable will be initiated. The width of this monostable is adjustable by RV-3. This pulse opens the Linear Gate, provides a signal to the period output buffer and the trailing edge fires the reset monostable (Q34, Q37). This monostable resets the Start Input, Stop Input and provides a signal to the Valid Start Buffer.

Assume a Stop Input is not received within the selected time range. Again the delay monostable is fired but the pulse that fires the width monostable is prevented by gate A5 when the over-range disc pulse is generated. This over-range pulse also fires the reset mono. Therefore, the inputs are reset and no TAC output will appear because the Linear Gate was not opened by the width mono pulse.

5.11 GATE INPUT

This input provides a means of gating the TAC output for coincidence or anticoincidence operation. A signal that exceeds +3 volts will switch the Gate Input Disc (Q55) which will change the state of Bistable A3c, A4d. The output of this bistable is tied to gate A5a, which will prevent or allow the output width mono to fire if the bistable is fired at the proper time. Therefore, in the Anticoincidence, if the gate input occurs during the output delay mono period, the output width mono is prevented and the Start and Stop Inputs are reset. If it occurs at any other time, the TAC output will appear. If in the coincidence mode of operation, the TAC output will only appear if the gate input signal occurs during the delay monostable period.

5.12 OVER-RANGE

The over-range disc provides a pulse to reset all circuitry if the Stop Input does not occur during the selected range time period. A14 is a comparator which compares the ramp generator voltage to a fixed reference developed by current source Q65. Therefore, when the ramp voltage exceeds the reference voltage, approximately - 3 volts, a pulse appears at the output of A14. This output fires a monostable (A17c, A16c) which provides the pulse needed to prevent the width mono from firing and also fires the reset monostable.

5.13 STOP INHIBIT

The stop inhibit circuit provides a means of preventing the Stop Command from occurring for a set amount of time. The Stop Inhibit Disc A8 is a comparator similar to A14 which provides a pulse when the ramp voltage exceeds the reference voltage. The reference voltage in this case is set by Stop Inhibit range potentiometer. The output of A8 through Q66 activates the stop clamp (Q19) and prevents the Stop Input from firing.

This pulse is also presented to the Stop Inhibit Buffer (Q67). The buffer provides a means of observing the Stop Inhibit time period at the Monitor Output. The inhibit period is whenever the monitor output is in a low state (0 volts).

5.14 PERIOD OUTPUT

This output provides a logic pulse that is in coincidence with the TAC output pulse. The output width monostable pulse is presented to the period output buffer (Q61-Q63). This buffer provides a positive low impedance fast rise and fall time pulse to the Period Output BNC.

5.15 VALID STOP

The Valid Stop provides a logic pulse with a duration equal to the time between the Stop Input and the Start of the Reset time. This pulse is derived when the Stop Input Disc fires the Ramp Current Source Control. It is then presented to the Valid Stop Buffer (Q38-Q40) which yields a positive low impedance fast rise and fall time pulse to the Valid Stop BNC.

5.16 VALID START

The Valid Start yields a pulse with a period equal to the time from the Start Input to the end of the reset time. This pulse is derived from the Start Input control signal and the reset monostable signal. These signals are ORed through A1d and presented to the Valid Start Buffer as one signal. This buffer (Q13, Q23, Q24) yields a positive low impedance fast rise and fall time pulse to the Valid Start output.

5.17 SCA

This circuit generates an SCA output for every TAC output occurring within the selected % of time. The time region selected is established with the TIME and Δ TIME controls. This pulse is generated by comparing the ramp voltage to some reference voltage. The reference being established by TIME potentiometer. The voltage selected by the TIME pot is fed through unity gain amplifiers A13 and A11. The voltage selected by the Δ TIME pot is fed through a unity gain amplifier, A12. At amplifier A10, the TIME and Δ TIME voltages are summed to yield the time plus Δ TIME at the output. The TIME voltage is fed through the lower level discriminator (LLD-A9) where it is compared to the ramp voltage. The TIME plus Δ TIME voltage is fed to the upper level discriminator (ULD-A18) and compared to the ramp voltage.

When the ramp voltage exceeds the voltage established by Voltage Summing Amplifiers, the discriminator yields a pulse. If the ramp exceeds the time voltage and not the TIME plus Δ TIME voltage, gate A17b is opened for the period of the output width monostable. Thus presented to the SCA Buffer is a pulse whose period is equal to the TAC output and in time coincidence. This buffer provides a pulse with characteristics similar to the Valid Start and Stop Buffers to the SCA Output.

If the ramp exceeds the TIME and TIME plus Δ TIME voltage, both discriminators are fired and gate A17b is closed by the ULD. No SCA pulse occurs at the output. Also, if the ramp never exceeds the TIME voltage, no SCA pulse will occur.

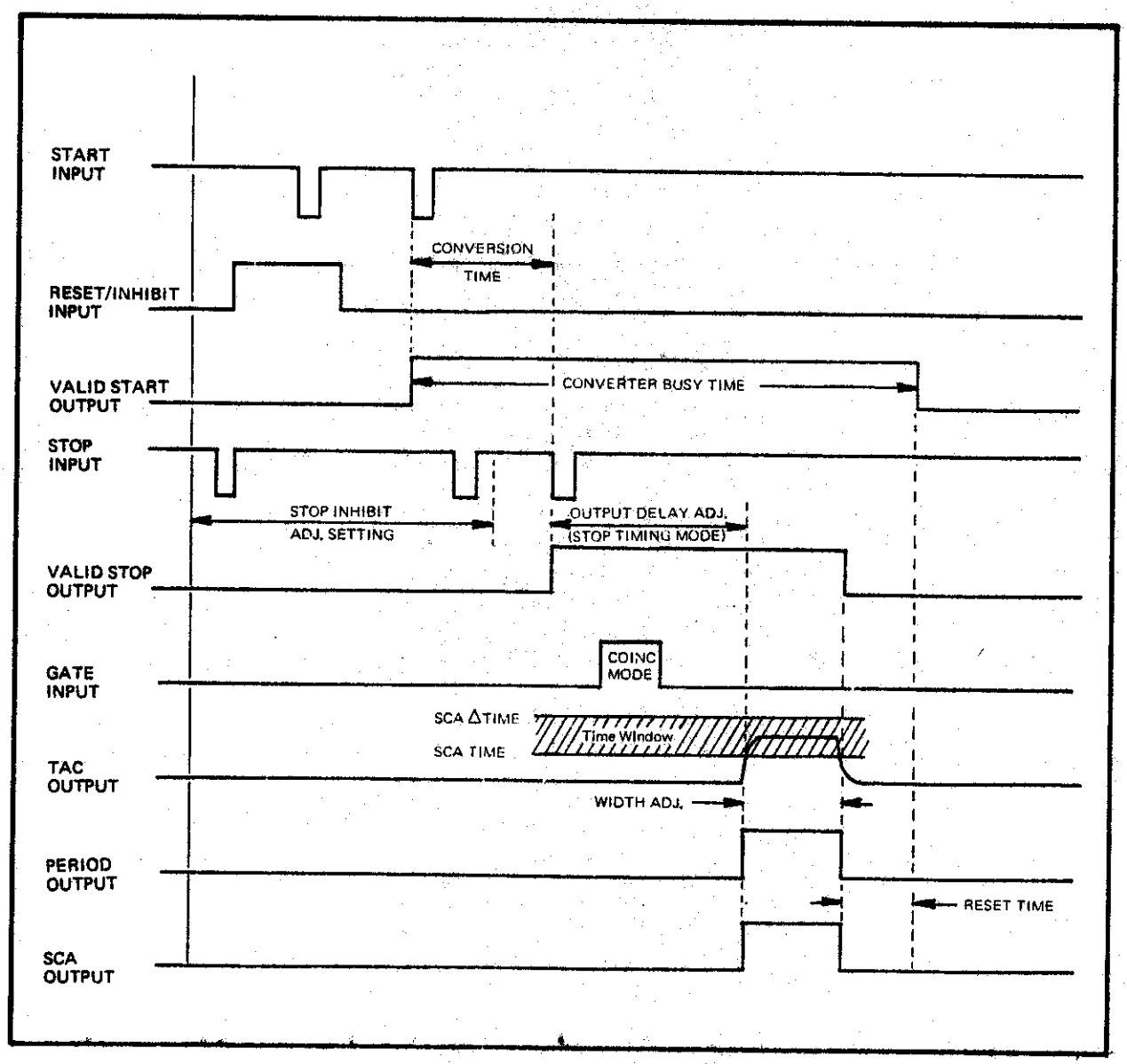


Figure 5-1. Timing Diagram, Model 1443.

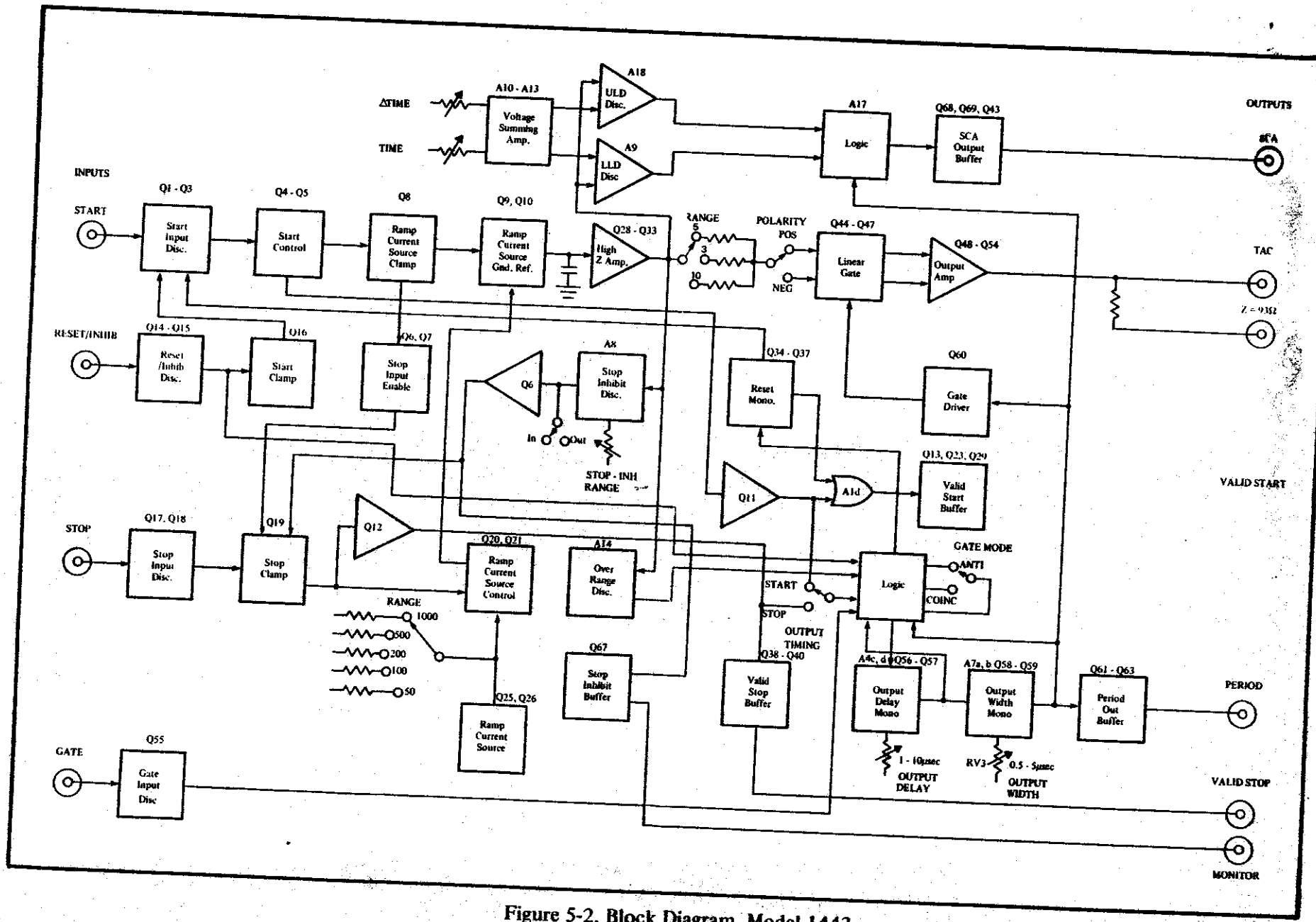
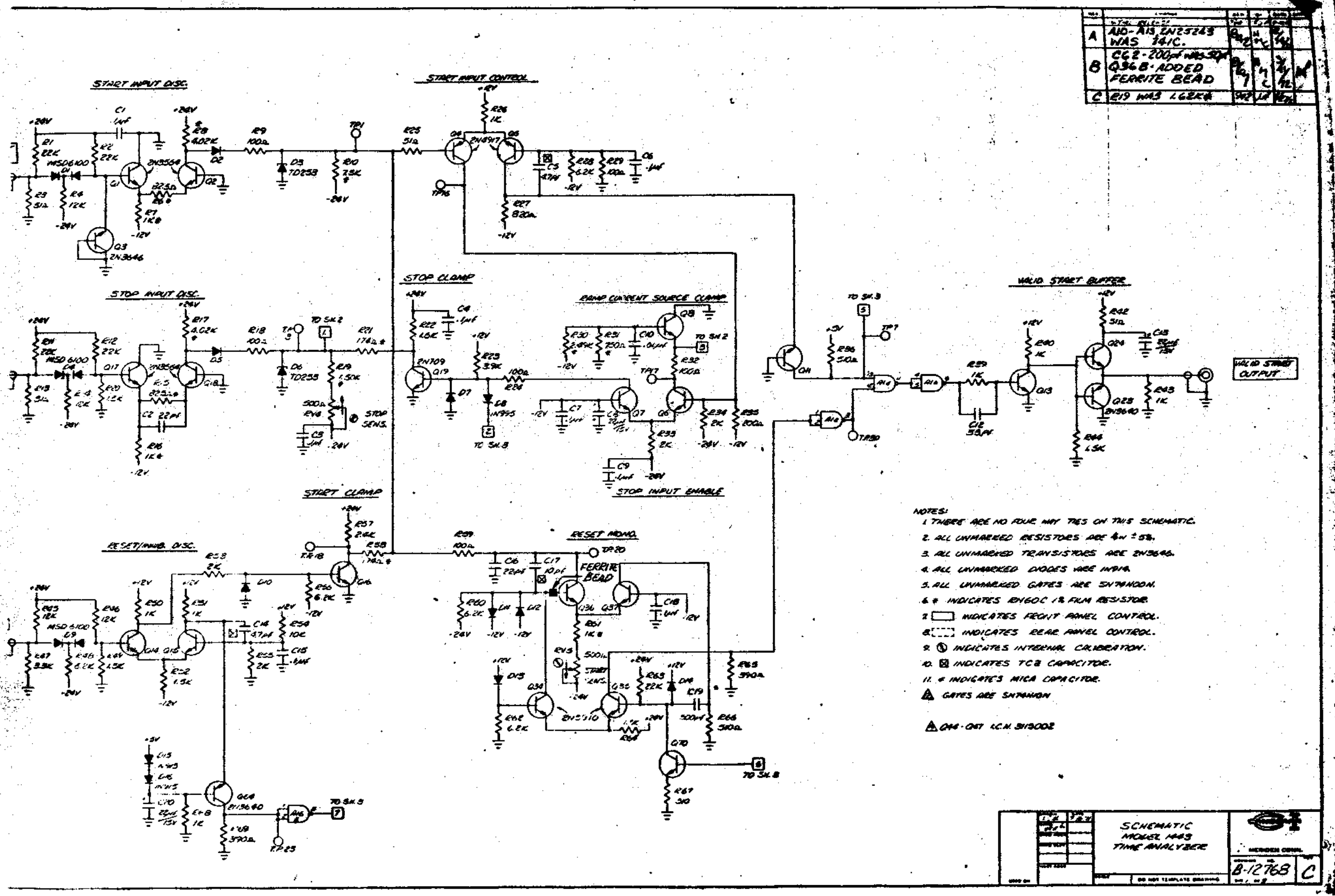
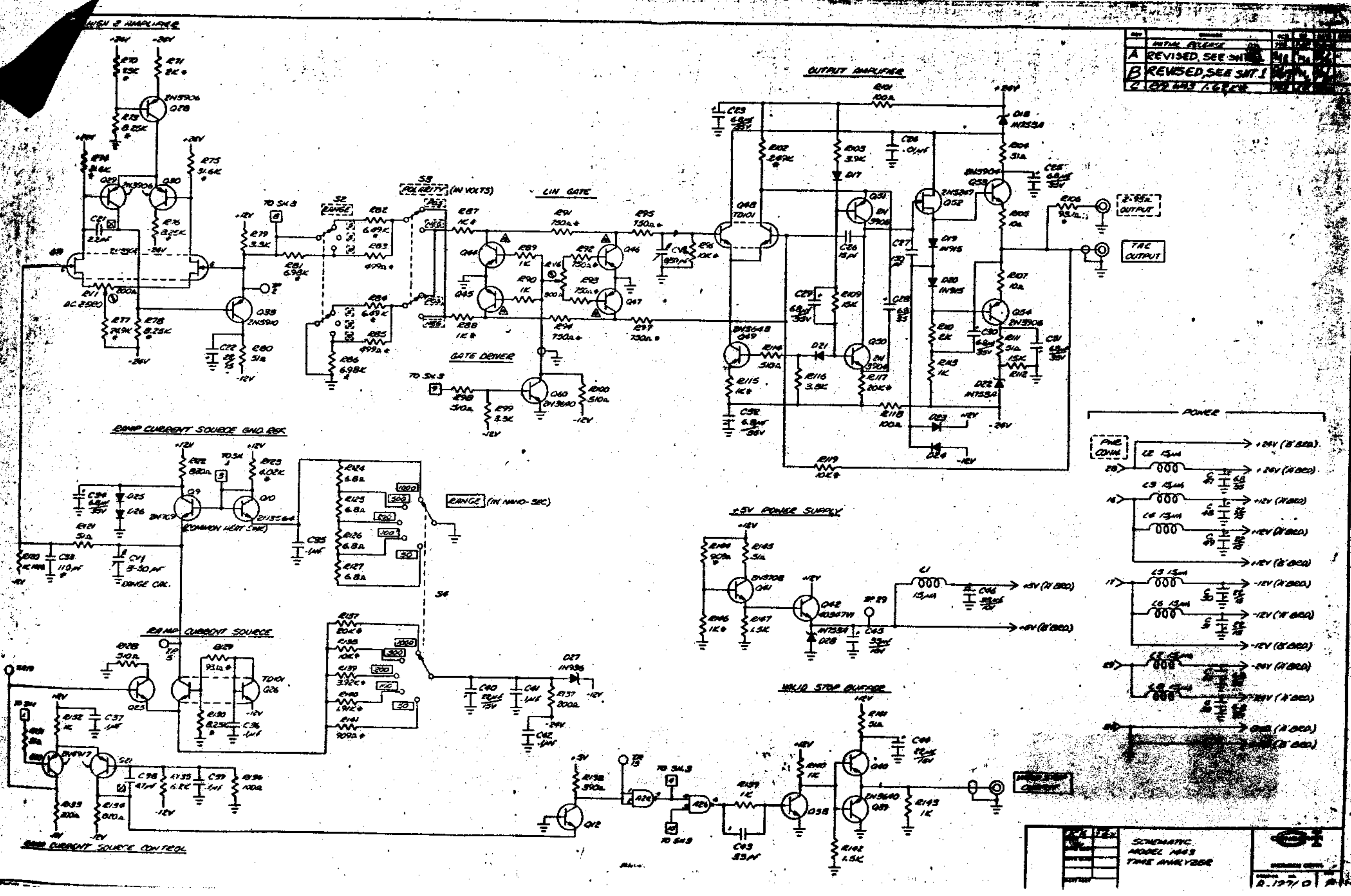
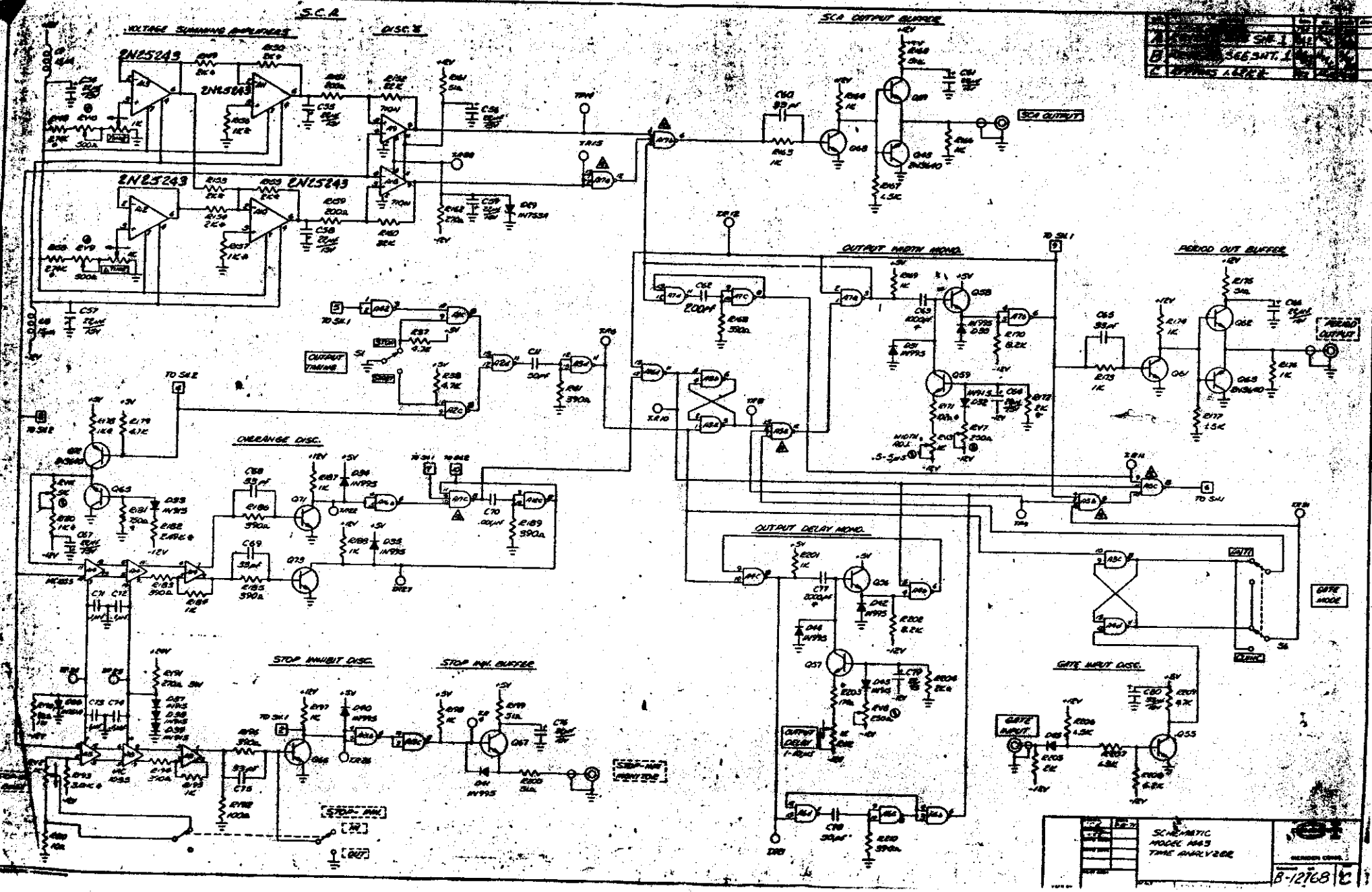


Figure 5-2. Block Diagram, Model 1443.


A AIO-AIS 2N25243 WAS 14IC.
B CC2-200pf WAS 50pf Q36B ADDED FERRITE BEAD
C R19 WAS 1.62K
START INPUT DISC.
START INPUT CONTROL
STOP CLAMP
STOP INPUT DISC.
RAMP CURRENT SOURCE CLAMP
STOP INPUT ENABLE
VALID START BUFFER
VALID START OUTPUT
START CLAMP
RESET/INHIB. DISC.
RESET MONO.
FERRITE BEAD
STOP SENS.
START SENS.
TO SH.2
TO SH.3
TO SH.5
TO SH.8
NOTES:
1. THERE ARE NO FOUR WAY TIES ON THIS SCHEMATIC.
2. ALL UNMARKED RESISTORS ARE ¼W ± 5%.
3. ALL UNMARKED TRANSISTORS ARE 2N3646.
4. ALL UNMARKED DIODES ARE IN914.
5. ALL UNMARKED GATES ARE SN7400N.
6. * INDICATES RN60C 1% FILM RESISTOR.
7. INDICATES FRONT PANEL CONTROL.
8. INDICATES REAR PANEL CONTROL.
9. INDICATES INTERNAL CALIBRATION.
10. INDICATES TC2 CAPACITOR.
11. # INDICATES MICA CAPACITOR.
GATES ARE SN7400N
Q44-Q47 I.C.N. 313002
SCHEMATIC
MODEL 1443
TIME ANALYZER
B-12768
C



INITIAL RELEASE
A REVISED, SEE SHT. 1
B REVISED, SEE SHT. 1
OUTPUT AMPLIFIER
LIN GATE
S3 POLARITY (IN VOLTS)
S2 RANGE
GATE DRIVER
TAC OUTPUT
RAMP CURRENT SOURCE GND REF
(COMMON HEAT SINK)
RANGE (IN NANO-SEC)
RANGE CAL.
RAMP CURRENT SOURCE
+5V POWER SUPPLY
POWER
SCHEMATIC
MODEL 1443
TIME ANALYZER


S.C.A.
VOLTAGE SUMMING AMPLIFIERS
DISC'R
SCA OUTPUT BUFFER
SCA OUTPUT
OUTPUT WIDTH MONO.
PERIOD OUT BUFFER
PERIOD OUTPUT
OVERANGE DISC.
OUTPUT DELAY MONO.
STOP INHIBIT DISC.
STOP INH. BUFFER
GATE INPUT DISC.
GATE INPUT
GATE MODE
OUTPUT TIMING
TO SH.1
TO SH.2
SCHEMATIC
MODEL 1443
TIME ANALYZER
B-12768