

# SINGLE CHANNEL ANALYZER

model 1431

**CANBERRA**

**NUCLEAR ELECTRONICS**

## Features

- Built-in DC Restoration
- 500nsec Pulse Pair Resolution
- Three Operating Modes: 100%  $\Delta E$ , 10%  $\Delta E$ , Dual Discriminator
- External Baseline Input
- Adjustable Output Pulse Widths
- LLD and ULD Nonlinearity  $<0.25\%$

## Description

The Canberra Model 1431 Single Channel Analyzer is used to analyze the pulse heights of pulses from shaping nuclear pulse amplifiers, by generating one or more logic pulse outputs when the input analog pulses meet the conditions imposed by the front panel controls.

The Model 1431 offers unprecedented flexibility and performance in a low cost, single width module. There are three modes of operation which, combined with three outputs, result in flexibility heretofore unattainable in a single instrument.

The available modes of operation are (1) Dual Discriminator, (2) the SCA with 100% Window, and (3) SCA with 10% Window.

The Dual Discriminator mode is particularly useful to replace two independent integral discriminators operating on the output of a single amplifier. In this mode, the ULD and LLD controls are completely independent, as are the ULD and LLD outputs. Each output fires whenever the input pulse exceeds the appropriate corresponding dial setting. In Dual Discriminator mode both the Lower Level Discriminator control and the Upper Level Discriminator control are referenced to ground. Their range is 25mV to 10 volts and both have ten-turn dials.

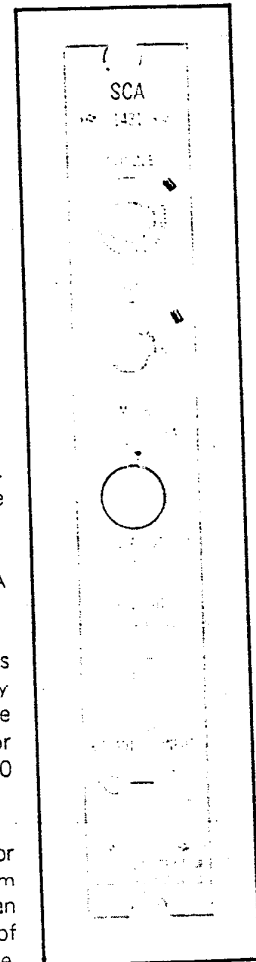
The 100%  $\Delta E$  mode is normally used with coarse resolution detectors and electronics, such as NaI(Tl) or gas proportional detectors. In this mode the upper level (ULD/  $\Delta E$ ) control selects a window width from 0% to 100% of the full scale (normally ten volts). This window rides on the baseline (LLD) setting. Thus, an SCA output is generated whenever the input pulse is greater than the LLD setting, but less than the sum of LLD plus  $\Delta E$ . In this mode, the LLD and ULD outputs operate exactly as in the Dual Discriminator mode.

The 10%  $\Delta E$  mode is normally used with high resolution spectrometers, such as Ge(Li) or silicon surface barrier or lithium drifted detectors. This mode is exactly the same as the  $\Delta E$  mode, except the upper level (ULD/  $\Delta E$ ) control selects a window width from 0% to 10% of the full scale (normally 10 volts).

The Model 1431 features a built-in DC Restorer for improved performance at high count rates. A front panel rise time control allows optimization of timing to attain the best pulse pair resolution for a given input wave shape. This, in addition to ultra fast recovery monostables, makes it possible to attain 0.5  $\mu\text{sec}$  pulse pair resolution (with output pulse widths of 0.4  $\mu\text{sec}$ ).

An external baseline input on the rear panel can be used in place of the Lower Level Discriminator control for applications requiring external sweeping of the window over the energy range. This input is compatible with the Canberra Model 833 Baseline Sweep.

As an option, an additional independent SCA output can be provided on the rear panel (Model 1431A).



# Specifications

## INPUTS

SIGNAL INPUT - .025 to 10 volts, unipolar or bipolar (positive lobe leading), input impedance 20k  $\Omega$  for signals above  $\approx 0.3$  volts, essentially 250  $\Omega$  for signals below 0.3 volts; DC restorer coupled, any pulse width available from commercial spectroscopy amplifiers

EXTERNAL BASELINE - 0 to 10 volts positive DC voltage

## OUTPUTS

LOWER LEVEL DISCRIMINATOR - positive 8 volt pulse, internally adjustable from 0.4 to 2.5 microseconds wide; rise time and fall times less than 25 nanoseconds; output impedance less than 10  $\Omega$

UPPER LEVEL DISCRIMINATOR - positive 8 volt pulse, internally adjustable from 0.4 to 2.5 microseconds wide; rise time and fall times less than 25 nanoseconds; output impedance less than 10  $\Omega$

SCA - positive 8 volt pulse internally adjustable from 0.4 to 2.5 microseconds wide; rise time and fall times less than 25 nanoseconds; output impedance less than 10  $\Omega$ ; (for second independently driven rear panel output, specify Model 1431A, additional charge \$25)

## CONTROLS

MODE - front panel rotary switch to select Dual Discriminator, 10% Window, or 100% Window modes

RISE TIME - front panel screwdriver adjust to match internal delay strobe to input waveform rise time

LOWER LEVEL DISCRIMINATOR (LLD) - front panel ten-turn dial to set lower discriminator level

UPPER LEVEL DISCRIMINATOR (ULD/  $\Delta E$ ) - front panel ten-turn dial to set upper discriminator (Dual Disc Mode) or Window width (SCA Mode)

PULSE WIDTH - three internal controls provide output pulse widths of 0.4 to 2.5 microseconds on each output (factory set at 0.4  $\mu$ sec width)

BASELINE SELECT - rear panel toggle switch to select Internal (LLD control) or External (DC voltage) control of the baseline

## PERFORMANCE

LINEARITY - less than 0.25% nonlinearity (integral) for both Lower Level and Upper Level Discriminators

TEMPERATURE STABILITY - both Lower and Upper Level Discriminators change less than 3mV/ $^{\circ}$ C, Window width stable to 0.5mV/ $^{\circ}$ C; 20 $^{\circ}$ C to 50 $^{\circ}$ C

PULSE PAIR RESOLUTION - better than 0.5 microseconds with output pulse width of 0.4 microsecond

## CONNECTORS

SIGNAL INPUT, LLD OUTPUT, ULD OUTPUT, SCA OUTPUT - front panel, BNC, UG-1094/U

EXTERNAL BASELINE INPUT, SCA OUTPUT (Model 1431A) - rear panel, BNC, UG-1094/U

## POWER

+24V - 10mA +12V - 140mA

-24V - 5mA -12V - 40mA

## PHYSICAL

SIZE - standard single-width NIM module (1.35 X 8.714 inches) per TID-20093 (rev)

WEIGHT - 2.2 lb (1.0 kg)

**SINGLE CHANNEL ANALYZER**

**MODEL 1431**

**CANBERRA INDUSTRIES, INC.**

**Nuclear Division**

**45 Gracey Avenue**

**Meriden, Connecticut 06450**

**Telephone: 203-238-2351**

Serial No. \_\_\_\_\_

SINGLE CHANNEL ANALYZER  
MODEL 1431

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# SINGLE CHANNEL ANALYZER

## SECTION 1 INTRODUCTION

### 1.1 GENERAL

The Canberra Model 1431 Single Channel Analyzer is used to analyze the amplitude of pulses from pulse shaping nuclear amplifiers by generating one or more logic pulse outputs when the input analog pulses meet the conditions imposed by the front panel controls.

The Model 1431 offers unprecedented flexibility and performance in a low cost, single width module. There are three modes of operation which, combined with three outputs, result in flexibility heretofore unattainable in a single instrument.

The available modes of operation are: (1) Dual Discriminator, (2) SCA with 100% Window, and (3) SCA with 10% Window.

The Dual Discriminator mode is particularly useful to replace two independent integral discriminators operating on the output of a single amplifier. In this mode, the upper level discriminator (ULD) and lower level discriminator (LLD) controls are completely independent, as are the ULD and LLD outputs. Each output fires whenever the input pulse exceeds the appropriate corresponding dial setting, as long as the setting of the ULD is above that of the LLD. In Dual Discriminator mode both the Lower Level Discriminator control and Upper Level Discriminator control are referenced to ground. Their range is 25mV to 10 volts; both have ten-turn dials covering this range.

The 100%  $\Delta E$  mode is normally used with coarse resolution detectors and electronics such as the NaI(Tl) or gas proportional detectors. In this mode the upper level (ULD/ $\Delta E$ ) control selects a window width from 0% to 100% of the full scale (normally ten volts). This window rides on the baseline (LLD) setting. Thus, an SCA output is generated whenever the input pulse is greater than the LLD setting, but less than the sum of LLD plus  $\Delta E$ . In this mode, the LLD and ULD outputs operate exactly as in the Dual Discriminator mode, except that the ULD is referenced to the LLD setting, not to ground. Thus, a ULD output is obtained when the input pulse is above the window (i.e., is greater than LLD plus  $\Delta E$ ).

The 10%  $\Delta E$  mode is normally used with high resolution spectrometers, such as Ge(Li) or silicon surface barrier or lithium drifted detectors. This mode is exactly the same as the 100%  $\Delta E$  mode, except the upper level (ULD/ $\Delta E$ ) control selects a window width from 10% of the full scale (normally ten volts).

The Model 1431 features a built-in DC Restorer for improved performance at high count rates. A front panel rise time control allows optimization of timing to obtain the best pulse pair resolution for a given input wave shape. This, in addition to ultra-fast recovery monostables, makes it possible to attain 0.5  $\mu$ sec pulse pair resolution with output pulse widths of 0.4  $\mu$ sec.

An external baseline input on the rear panel of the Model 1431 can be used in place of the lower level discriminator control for applications requiring external sweeping of the window over the energy range; this input is compatible with the Canberra Model 833 SCA Sweep.

## 1.2 SPECIFICATIONS

### 1.2.1 INPUTS

#### SIGNAL INPUT

0.25 to 10 volts, unipolar or bipolar (positive lobe leading), input impedance 20K ohms for signals above  $\approx 0.3$  volts, essentially 250 ohms for signals below 0.3 volts; DC restorer coupled, any pulse width available from commercial spectroscopy amplifiers

#### EXTERNAL BASELINE

0 to 10 volts positive DC voltage

### 1.2.2 OUTPUTS

#### LOWER LEVEL DISCRIMINATOR

positive 8 volt pulse, internally adjustable from 0.4 to 2.5 microseconds wide; rise time and fall times less than 25 nanoseconds; output impedance less than 10 ohms

#### UPPER LEVEL DISCRIMINATOR

positive 8 volt pulse, internally adjustable from 0.4 to 2.5 microseconds wide; rise time and fall times less than 25 nanoseconds; output impedance less than 10 ohms

#### SCA

positive 8 volt pulse, internally adjustable from 0.4 to 2.5 microseconds wide; rise time and fall times less than 25 nanoseconds; output impedance less than 10 ohms. For second independently driven rear panel output, specify Model 1431A, additional charge \$25

### 1.2.3 CONTROLS

#### MODE

front panel rotary switch to select Dual Discriminator, 10% Window, or 100% Window modes

#### RISE TIME

front panel screwdriver adjust to match internal delay strobe to input waveform rise time

#### LOWER LEVEL DISCRIMINATOR (LLD)

front panel ten-turn dial to set lower discriminator level

#### UPPER LEVEL DISCRIMINATOR (ULD/ $\Delta E$ )

front panel ten-turn dial to set upper discriminator (Dual Discriminator, 10% Window, or 100% Window modes)

#### PULSE WIDTH

three internal controls provide output pulse widths of 0.4 to 2.5 microseconds on each output

#### BASELINE SELECT

rear panel toggle switch to select Internal (LLD control) or External (DC voltage) control of the baseline

1.2.4 PERFORMANCE

LINEARITY

less than 0.25% nonlinearity (integral) for both Lower Level and Upper Level Discriminators

TEMPERATURE STABILITY

both Lower and Upper Level Discriminators change less than 0.5mV/°C, Window Width stable to 0.5mV/°C; 20°C to 50°C

PULSE PAIR RESOLUTION

better than 0.5 microseconds with output pulse width of 0.4 microsecond

POWER REQUIREMENTS

+24V	10mA	- +12V	140mA
-24V	0mA	- -12V	40mA

1.2.5 PHYSICAL

SIZE

standard single-width module (1.35 inches wide) per TID-20893

WEIGHT

2.2 lbs.

## SECTION 2

### CONTROLS AND CONNECTORS

#### 2.1 GENERAL

This section describes the functions of the controls and connectors located on the front and rear panels of the Model 1431 Single Channel Analyzer. It is recommended that this section be read before proceeding with the operation of the module.

#### 2.2 CONTROLS

##### 2.2.1 MODE

This front panel rotary switch permits selection of the three modes of operation of the Model 1431—Dual Discriminator, 10% Window, and 100% Window.

a. Dual Discriminator mode: This mode provides two independent integral discriminators operating on the output of a single amplifier. When the Dual Discriminator mode is selected, the Upper Level Discriminator control and the Lower Level Discriminator control function completely independently, as do their respective outputs.

Both control potentiometers are referenced to ground potential, and each output fires whenever an input pulse exceeds the appropriate dial setting as long as the setting of the ULD is above that of the LLD. Range of each of the discriminators is continuously variable from 25mV to 10 volts. (See Section 2.2.3 and 2.2.4).

b. 10% Window: This SCA mode provides high resolution capability, and has been designed for use with high resolution spectrometers, such as Ge(Li), silicon surface barrier, or lithium drifted detectors. The baseline is set by the Lower Level Discriminator (LLD), or externally via the EXTERNAL BASELINE input. Window width is set by the Upper Level Discriminator (ULD/ $\Delta E$ ) from 0% to 10% of full scale (normally ten volts).

An SCA output is generated whenever an incoming signal is greater than the LLD (baseline) setting, but less than the sum of LLD plus  $\Delta E$ .

In this mode, the LLD and ULD outputs operate exactly as in the Dual Discriminator mode, except that the ULD/ $\Delta E$  level is referenced to the LLD setting, and not to ground. Thus, a ULD output is obtained when the input pulse is above the window (i.e., greater than LLD plus  $\Delta E$ ).

c. 100% Window: This mode is normally used with coarse resolution detectors and electronics, such as NaI(Tl) or gas proportional detectors. In this mode, the Upper Level Discriminator (ULD/ $\Delta E$ ) selects a window width from 0% to 100% of full scale (normally ten volts). This window rides on the baseline (LLD) setting. An SCA output is generated whenever the incoming signal is greater than the LLD setting, but less than the sum of LLD plus  $\Delta E$ .

Both the LLD and ULD outputs operate exactly as in the Dual Discriminator mode, except that the ULD/ $\Delta E$  level is referenced to the LLD setting, and not to ground.

##### 2.2.2 RISE TIME

This front panel screwdriver adjustment potentiometer permits the user to match the strobe time of the Model 1431 to the rise time of the input waveform; proper utilization of this control results in the



best possible pulse pair resolution for any given input wave shape. Section 3.3.1 should be consulted for details concerning proper adjustment of the RISE TIME setting.

### 2.2.3 LOWER LEVEL DISCRIMINATOR (LLD)

This front panel ten-turn potentiometer sets the lower discriminator level. When the BASELINE SELECT switch is in the INTERNAL position, the setting of the LLD control determines the baseline.

### 2.2.4 UPPER LEVEL DISCRIMINATOR (ULD/ $\Delta E$ )

This front panel ten-turn potentiometer sets the upper discriminator level (in the Dual Discriminator mode), or the window width (in either of the SCA modes).

### 2.2.5 BASELINE SELECT

This rear panel toggle switch permits selection of internal (LLD) or external (DC voltage) control of the baseline setting. In the EXTERNAL position, the Lower Level Discriminator continues to function, but the LLD front panel control is disabled, and an externally applied DC voltage level determines the baseline setting (See Section 2.3.2). When the BASELINE SELECT switch is in the INTERNAL position, the baseline setting is determined by the LLD control (See Section 2.3.3).

### 2.2.6 PULSE WIDTH

The PULSE WIDTH controls are three internal potentiometers which permit adjustment of the width of each of the three output pulses (LLD, ULD, and SCA) over a range of 0.4 to 2.5 microseconds. RV-11 controls the SCA output width; RV-13 controls the ULD output width; RV-12 controls the LLD output width.

## 2.3 CONNECTORS

### 2.3.1 SIGNAL INPUT

This front panel BNC connector accepts incoming pulses between 0.025 and 10 volts, unipolar or bipolar (positive lobe leading). The SIGNAL INPUT is fully DC restorer coupled for improved performance at high counting rates, and will accept pulses of any width available from commercial spectroscopy amplifiers. The input impedance for signals above  $\approx 0.3$  volts is 20K ohms or greater; for signals below 0.3 volts, the input impedance is approximately 250 ohms.

### 2.3.2 EXTERNAL BASELINE INPUT

This rear panel BNC connector accepts an externally applied signal from 0 to +10 volts DC, and is used in conjunction with the BASELINE SELECT switch to permit external control of the baseline setting. Typically, external baseline control is required for external sweeping of the SCA window over the energy range, as when the Model 1431 is used with the Canberra Model 833 SCA Sweep. Input impedance of this connector is greater than 5000 ohms.

### 2.3.3 LOWER LEVEL DISCRIMINATOR OUTPUT

This front panel BNC connector furnishes a positive 8 volt logic pulse whenever the Lower Level Discriminator fires. Pulse width is internally adjustable from 0.4 to 2.5 microseconds; rise and fall times are less than 25 nanoseconds, and the output impedance is less than 10 ohms.

#### 2.3.4 UPPER LEVEL DISCRIMINATOR OUTPUT

This front panel BNC connector furnishes a positive 8 volt logic pulse whenever the Upper Level Discriminator fires. Pulse width is internally adjustable from 0.4 to 2.5 microseconds; rise and fall times are less than 25 nanoseconds, and the output impedance is less than 10 ohms.

#### 2.3.5 SCA OUTPUT

This front panel BNC connector furnishes a positive 8 volt logic pulse whenever an incoming signal exceeds the level set by the LLD control, but is less than the sum of LLD plus  $\Delta E$  in the SCA modes, or whenever the signal is between the LLD control setting and the ULD control setting in the Dual Disc mode. Pulse width is internally adjustable from 0.4 to 2.5 microseconds; rise and fall times are less than 25 nanoseconds, and the output impedance is less than 10 ohms.

## SECTION 3 OPERATING INSTRUCTIONS

### 3.1 GENERAL

The purpose of this section is to familiarize the user with the controls of the Model 1431 Single Channel Analyzer, and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand.

### 3.2 INITIAL SETUP

#### 3.2.1 REQUIRED EQUIPMENT

In order to perform the checkout procedures in this section, the following equipment will be required, in addition to the Model 1431.

- One Canberra Model 1407 Test Pulse Generator (or equivalent)
- One Canberra Model 1417 Spectroscopy Amplifier (or equivalent)
- One oscilloscope (Tektronix 535, or equivalent)

#### 3.2.2 SETUP

Insert modules in an AEC compatible base unit/power supply, such as the Canberra Model 1400, and interconnect as in Figure 3-1; turn on power switch.

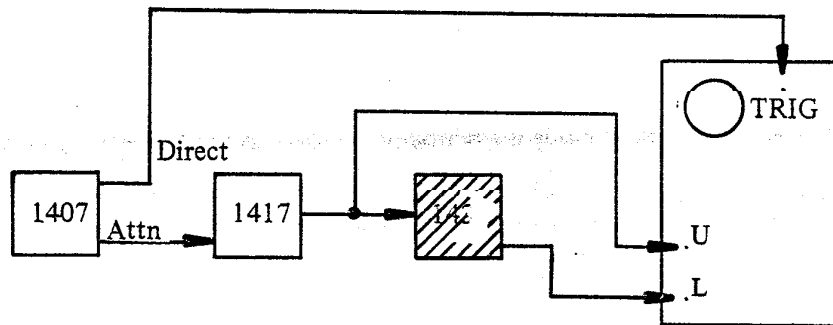


Figure 3-1

- Set shaping of Model 1417 to 1 microsecond.
- Set gain of Model 1417 for 5 volt peak pulse output.
- Set Mode control of Model 1431 to 100% Window position.
- Set LLD control to 4.0 volts.
- Set ULD/ $\Delta E$  control to 2.0 volts.
- Set BASELINE SELECT switch to INTERNAL position.

### 3.3 INITIAL CHECKOUT

#### 3.3.1 ADJUSTMENT OF RISETIME CONTROL

Observe the SCA OUTPUT on the lower trace of the oscilloscope, and the amplifier output on the upper trace.

Adjust the RT (Risetime) control of the Single Channel Analyzer so that the SCA output occurs just after the peak of the input pulse. (This control will require readjustment if other main shaping amplifier time constants are used.)

#### 3.3.2 WINDOW MODE

Observe the SCA OUTPUT to be a positive 8 volt, 0.4 microsecond wide pulse.

Vary the Pulser amplitude, and observe that the SCA output disappears when the amplifier output is below 4.0 volts and above 6.0 volts.

Observe the LLD output to be a positive 8 volt, 0.4 microsecond wide pulse (i.e., identical to the SCA output).

Vary the Pulser amplitude, and observe that the LLD output disappears when the amplifier output is below 4.0 volts.

Observe the ULD output to be identical to the SCA output and the LLD output.

Vary the Pulser amplitude, and observe that the ULD output appears when the amplifier output is 6.0 volts or more.

#### 3.3.3 10% WINDOW MODE

Checkout for the 10% Window mode is essentially the same as for 100% Window mode, except that the window width (with the same control settings) will be 0.2 volts. Thus, the SCA output will disappear when the amplifier output is below 4.0 volts and above 4.2 volts; the LLD output will disappear when the amplifier output is below 4.0 volts; and the ULD output will appear when the amplifier output is 4.2 volts or above.

#### 3.3.4 DUAL DISCRIMINATOR MODE

Set LLD control to 4.0 volts and ULD control to 6.0 volts.

Repeat the steps outlined in Section 3.3.2, observing the same results.

#### 3.3.5 EXTERNAL BASELINE CONTROL

Set Mode control to 100% Window mode.

Set BASELINE SELECT switch to EXTERNAL position.

Using a variable DC voltage having a source impedance less than 100 ohms, apply a voltage of 4.0 volts to the EXTERNAL BASELINE INPUT on the rear panel of the Model 1431.

Repeat the steps outlined in Section 3.3.2.

Change the voltage on the EXTERNAL BASELINE INPUT to 2.0 volts.

Observe the SCA output disappear when the input signal is above 4.0 volts or below 2.0 volts.

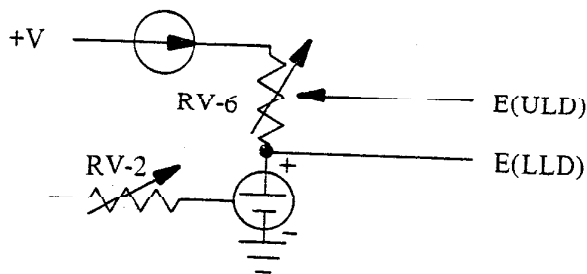
## SECTION 4 CIRCUIT DESCRIPTION

### 4.1 DC RESTORER INPUT

The input circuit is a Robinson type DC restorer (Q1, Q2, D2, D3) followed by a noninverting amplifier Q3 which provides a high impedance input for the DC restorer.

### 4.2 REFERENCE VOLTAGE GENERATION

Reference voltages for the LLD and the ULD are provided by RV-2 and by RV-6 respectively. The LLD reference is a voltage source which is fed by a constant current passing through the ULD potentiometer RV-6 as shown below:



RV-1 is used to calibrate the LLD on the upper end of its range; RV-4 is used to calibrate the LLD on the lower end of its range. RV-7 is a trim for 10%  $\Delta E$  in the window mode. RV-5 is a trim for 100%  $\Delta E$  in the window mode. RV-9 is a trim for the ULD in the DUAL DISC mode. RV-8 is used to calibrate the ULD on the lower end of its range in either WINDOW mode.

The reference voltages go to comparators A1 and A2.

### 4.3 COMPARATORS

A1 and A2 change output states when the input signal exceeds the setting of the LLD and ULD controls respectively. A1, the LLD comparator, fires a monostable A3A, A3B, and Q21, the ULD comparator A2, fires a flip flop (A4A and A4B).

### 4.4 "EXCLUSIVE OR"

If the ULD has not fired A4D is enabled, and the interrogation pulse will fire the SCA output monostable A6C, D and Q12. A4C on the other hand, is inhibited and the interrogation pulse does not get through to fire the ULD monostable (A5C, D and Q23).

If the ULD has fired, A4D is inhibited and prevents firing of the SCA monostable. A4C is now enabled, and the interrogation pulse fires the ULD monostable. In either case the LLD monostable is triggered if the LLD comparator fires.

### 4.5 OUTPUT DRIVERS

The LLD, ULD and SCA outputs are generated and driven by identical monostables and drivers. The monostables have active charging circuits to improve rise and fall times and to minimize recovery time. The output pulse widths are adjustable from 0.4  $\mu\text{sec}$  to 2.5  $\mu\text{sec}$  by means of RV12, RV13, and RV-11.

SECTION 5  
CALIBRATION PROCEDURE

5.1 EQUIPMENT REQUIRED

Tail Pulse Generator – Canberra Model 1407 or equivalent

Main Shaping Amplifier – Canberra Model 1417 or equivalent

Oscilloscope – Tektronix Type 453 or equivalent

5.2 TEST SETUP

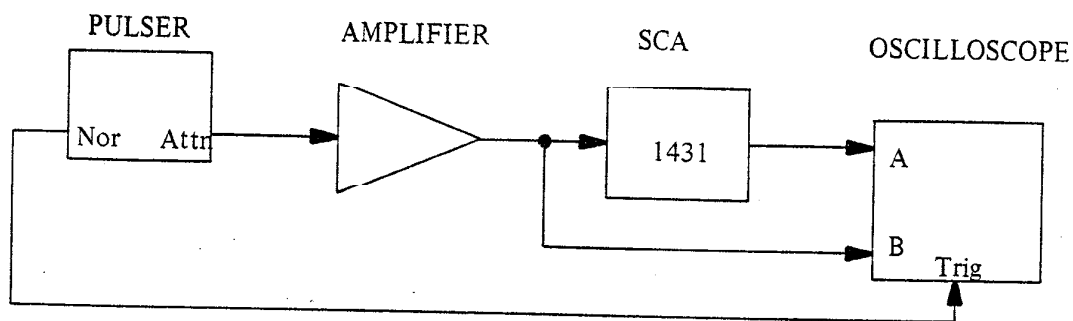


Figure 1

5.2.1 Connect instruments as shown in Figure 1.

5.2.2 Set amplifier for 0.25  $\mu$ sec. shaping, unipolar, high count rate. (Note: correctly Pole-Zero the Amplifier output.)

5.3 CALIBRATION

5.3.1 DIAL SETTINGS

Set LLD control stop to read 25mV maximum CCW direction. Set ULD control stop to read 0mV at maximum CCW direction.

5.3.2 LLD CALIBRATION

1. Width mode switch to 100%  $\Delta E$  and REAR LLD switch to INT, set LLD control to 0.2 volt. Adjust RT (Risetime) control fully clockwise. Apply a 0.2 volt pulse from the amplifier to the SCA input. Observe the LLD output and adjust RV-4 until the LLD fires for about 50% of the input pulses.

2. Set LLD control to 7.00 volts and increase input voltage to 7.00 volts. Adjust RV-1 until the LLD fires for about 50% of the input pulses.

3. Steps 5.3.3.1 and 5.3.3.2 must be applied alternately to arrive at the optimum setting for both high and low inputs.

### 5.3.3 ULD CALIBRATION (100% Window)

1. Apply a 0.1 volt pulse to the input and lower the LLD control until the LLD fires for each input pulse.
2. Turn the ULD/ $\Delta$ E control fully counterclockwise. Observe the LLD output and adjust RV-8 until the ULD just begins to fire for all input pulses. Observe that no pulses appear on the SCA output.
3. Increase the input pulse height to 8.0 volts and adjust the ULD/ $\Delta$ E control to 7.9 volts. Adjust RV-5 until the ULD fires for about 50% of the input pulses.
4. Step 5.3.4.2 and 5.3.4.3 must be applied alternately to arrive at the optimum setting for both high and low inputs.

### 5.3.4 ULD CALIBRATION (10% Window)

1. Set mode switch to 10%  $\Delta$ E. Apply a 7.0 volt pulse to the SCA input and adjust the LLD control downward toward 7 volts until the LLD fires for each input pulse. Set the ULD/ $\Delta$ E control to 0. (Note that the SCA output does not fire and that the ULD fires for each input pulse. If this is not the case, repeat 5.3.4).
2. Change the input pulse height to 7.5 volts and adjust the ULD/ $\Delta$ E control to 0.5 volts (5 on dial). Adjust RV7 until the ULD fires for about 50% of the input pulses.
3. Check the unit again in accordance with 5.3.4 and make alternate adjustments if necessary until the requirements of both 5.3.4 and 5.3.5 are met.

### 5.3.5 ULD CALIBRATIONS (DUAL DISC)

Set Mode switch to DUAL DISC and apply a 0.1 volt pulse to the input. Set LLD control to 25mV and the ULD/ $\Delta$ E control to 0.1 volt. Observe the ULD output and adjust RV-9 until an output pulse appears for about 50% of the input pulses.

### 5.3.6 OUTPUT PULSE WIDTHS

Observe each of the outputs in turn and adjust RV-13, RV-11, and RV-12 for the desired pulse widths on the ULD, SCA and LLD outputs respectively.