DOUBLE DELAY LINE AMPLIFIER

Model 1411

June, 1970

CANBERRA INDUSTRIES
45 Gracey Avenue
Meriden, Connecticut 06450

Telephone: 203-238-2351

WARRANTY

canberra analytical instruments

This equipment is warranteed by Canberra to be free from defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in this instruction manual. Repairs or replacement, at Canberra's option, will be made without charge at the Canberra plant during this warranty period. Except for the case of defects discovered upon initial operation, shipping expense to Canberra is to be paid by the customer; shipping expense to return the repaired equipment will be paid by Canberra.

Canberra reserves the right to modify its products without incurring the responsibility for modifying previously manufactured products.

Canberra does not assume any liability for the results of particular installations, as these circumstances are not in our control.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, notify Canberra and the carrier making delivery immediately, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in damage claims.

REPAIRS

Any Canberra instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. All such work will be done at the least possible expense to the customer. All equipment thus repaired or realigned will pass through our normal preshipment checkout procedure and will meet or surpass its original specifications when returned. Return shipping expense will, in this case, also be charged to the customer.

CANBERRA INDUSTRIES, INC.
45 Gracey Avenue
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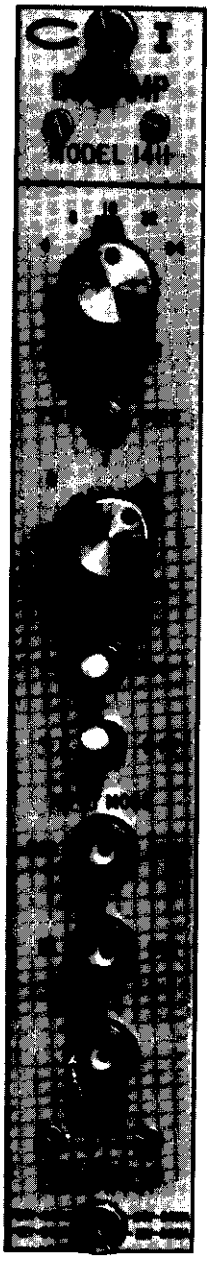


DOUBLE DELAY LINE AMPLIFIER

Model 1411

SECTION 1
INTRODUCTION

1.1 GENERAL

The Canberra Model 1411 Double Delay Line Amplifier accepts the preamplified positive or negative output signals from proportional counters, scintillation detectors, or semiconductor detectors. It yields in turn output signals suitable for single channel or multichannel analysis, and for leading edge or zero crossing timing.

The Model 1411 exhibits less than one nanosecond of crossover walk over a 20:1 dynamic range (0.5 to 10 volt output). It is thus unmatched when precise fast coincidence timing using the zero crossing technique is desired. The Model 1411 DDL Amplifier offers both prompt (DDL OUT) and delayed (DL OUT) signals, to preserve a unipolar signal for energy analysis after timing and coincidence evaluation has taken place. The unipolar signal thus available has an integration time constant of 700 nanoseconds (with 1 microsecond shaping delay lines) for optimum energy analysis.

1.2 APPLICATIONS

The DDL Amplifier is especially well suited for applications requiring:

High counting rates, as DDL shaping offers the most rapid baseline recovery.

Heavy overload conditions, as DDL shaping yields unsurpassed overload performance.

The most accurate leading edge or zero crossing timing over a wide dynamic range, as DDL shaping exhibits minimum timing jitter when compared to alternative shaping approaches.

When these requirements are not present, DDL shaping is not recommended, as it has the disadvantage of slightly greater inherent amplifier noise than RC shaping, leading to loss of system resolution.

The Model 1411 has been designed to optimize its performance in those applications for which DDL shaping is best suited. It offers adjustable pole/zero cancellation to optimize baseline recovery and maximize overload performance. The Model 1411 will recover from a 500X overload in less than 2.5 microseconds, when using 0.4 microsecond delay lines.

1.3 SPECIFICATIONS

INPUT SIGNAL

Polarity: positive or negative tail pulse from associated preamplifier.

Amplitude: 0 to 5 volts.

Risetime: 0 - 1000 nanoseconds.

Fall Time: 30 - 1000 microseconds.

Impedance: 1000 ohms, DC coupled.

Connector Type: BNC UG-1094/U.

OUTPUT SIGNALS

DDL OUT

Polarity: bipolar (positive lobe leading).

Amplitude: 0 - 10 volts linear, 10.5 volts saturation into 93 ohms.

Risetime: less than 100 nanoseconds, double delay line clipped.

Width per Lobe: 1.0 microsecond (0.2, 0.4, 0.6, 0.8, 2.5 microseconds optional).

Impedance: less than 1 ohm, DC coupled.

Connector Type: BNC UG-1094/U.

DL OUT

Polarity: positive, unipolar.

Amplitude: 0 - 10 volts linear, 10.5 volts saturation into 93 ohms.

Risetime: 700 nanoseconds, nominal, for optimum energy analysis.

Delay: delayed from DDL OUT by 2.5 microseconds.

Impedance: less than 1 ohm, DC coupled.

Connector Type: BNC UG-1094/U.

GAIN STABILITY	Better than 0.01%/°C; better than 0.02% over 24 hours with constant temperature and supply voltages.
LINEARITY	Better than 0.1% integral from 0.3 to 10 volts output.
OVERLOAD RECOVERY	Recovers to within 2% of baseline from 500X overload in less than 2 nonoverloaded pulse widths at full gain.
DC LEVEL STABILITY	Better than 2mV/°C; better than 10mV over 24 hours.
CROSSOVER WALK	Less than 1 nanosecond crossover jitter over a 20:1 output amplitude range(0.5 - 10 volts).
NOISE	Less than 10 microvolts referred to the input at full gain (DL output).
GAIN	Maximum gain: 1000; adjustable by means of front-panel controls over 640:1 range.
CONTROLS	COARSE GAIN: front-panel rotary switch providing a 16:1 range in 4 binary steps. FINE GAIN: front-panel single-turn precision potentiometer providing a 4:1 range. POLE/ZERO: front-panel screwdriver adjustment to optimize amplifier baseline recovery and overload for the preamplifier fall time constant used. INPUT POLARITY: front-panel toggle switch, POS and NEG positions. INPUT ATTENUATION: front-panel toggle switch, ÷1 and ÷10 positions. DC LEVELS: two side-panel screwdriver adjustments to set output DC levels to zero volts.
POWER REQUIREMENTS	+24V - 60mA, -24V - 60mA +12V - 60mA, -12V - 60mA

PHYSICAL

Size: standard single-width module (1.35 inches wide) per TID-20893.

Weight: 2.3 lbs.

SECTION 2
CONTROLS AND CONNECTORS

2.1 GENERAL

This section describes the functions of the controls and connectors located on the module. It is recommended that this section be read before proceeding with the operation of the module.

2.2 CONTROLS

2.2.1 COARSE GAIN Switch

This switch selects the factor by which the input is to be amplified. The gain positions are 4, 8, 16, 32, and 64. It provides a 16:1 range.

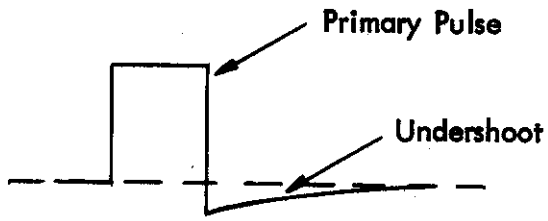
2.2.2 FINE GAIN Potentiometer

This control varies the output voltage, as set by the COARSE GAIN switch, by a factor of 1:1/4. It is a single-turn potentiometer. The COARSE GAIN and FINE GAIN settings allow a gain of 16 to 1000 to be selected.

2.2.3 POLE/ZERO Adjustment

This front-panel screwdriver adjustment permits the precise elimination of undershoots on the amplifier pulse after the first differentiation, for all input pulses whose fall time constant exceeds 30 microseconds.

Nominally, singly-differentiated pulses actually have two differentiations: the first by the amplifier first-differentiation circuitry (whose time constant may range from 100 nanoseconds up to 10 microseconds), the second by the preamplifier circuitry (whose fall time constant usually ranges from 40 to 1000 microseconds). The "singly-differentiated" pulse actually appears as



where the undershoot has an amplitude roughly equal to the amplitude of the primary pulse times the ratio of the amplifier differentiating time constant to the preamplifier fall time constant.

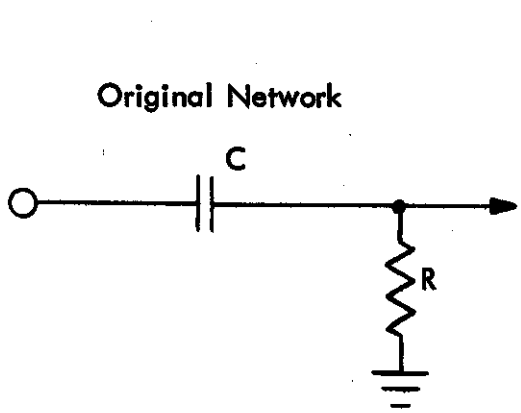
For example, if the preamp fall time constant is 70 microseconds, a one-microsecond first-differentiated pulse, ten volts in amplitude, will have an undershoot equal to

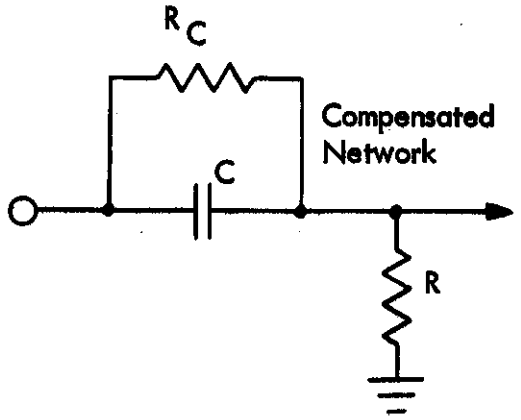
$$\frac{(10)(1)}{70} = 142\text{mV}$$

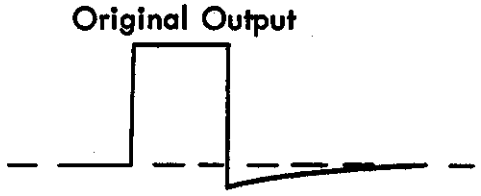
This undershoot causes two effects. If the undershoot saturates under amplifier overload conditions, the amplifier is blocked not only until the primary lobe recovers, but also until the undershoot recovers (at the much slower rate of the preamp fall time constant).

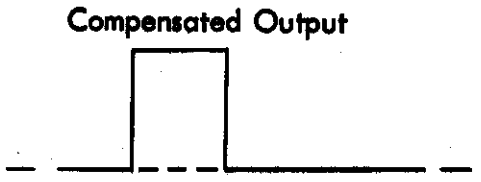
Second, if the count rate is sufficiently high, succeeding pulses may fall into the undershoot of preceding pulses, subtracting from their apparent pulse height and causing peaks to broaden on the low energy side.

In its simplest form the original differentiating network is compensated by the addition of a single resistor. Refer to the following diagrams:









This technique is fully effective only if the input pulse to the network is composed of a single exponential fall time constant - thus, problems will be encountered in trying to compensate the fall time constants contained in the more complex pulse arising when a pulse generator with fall time constant T_1 feeds a preamplifier with fall time constant T_2, which in turn feeds the main amplifier. One may compensate for either time constant, but not both simultaneously.

The compensation circuit must in practice be variable, to permit adjustment for the range of fall time constants that may be encountered in the field. In the Canberra Double Delay Line Amplifier, this compensation range extends from 30 microseconds upward, covering all commercially available preamplifiers.

In the practical case, adjustment is best done live, by observing the unipolar pulses (DL OUT) from the amplifier with the detector and preamplifier attached. System noise will obscure the undershoots when the adjustment is reasonably close. One aid is to increase the amplifier gain by X8 or more for the purposes of this adjustment. If low energy tailing is observed on spectral peaks, it may be a sign that the Pole/Zero adjustment is incorrect.

2.2.4 POS/NEG Switch

This switch determines the polarity of the signal input which will be accepted by the module.

2.2.5 ÷1/÷10 Switch

The input signal will be attenuated by the factor selected by this switch. The ÷10 position should not be used unless absolutely necessary, as the amplifier signal to noise ratio is decreased by a factor of ten when the input signal is attenuated.

2.3 INPUT REQUIREMENTS

Positive or negative tail pulse from associated preamplifier, 0 to 5 volts; 0 - 1000 nanoseconds risetime, 30 - 1000 microsecond fall times; input impedance 1000 ohms, DC coupled.

2.4 OUTPUT SIGNALS

2.4.1 DDL OUT Connector

Bipolar (positive lobe leading), 0 - 10 volts, 10.5 volts saturation into 93 ohms; double delay line clipped, risetime less than 100 nanoseconds; width per lobe, 1.0 microseconds (0.2, 0.4, 0.6, 0.8, and 2.5 microseconds optional); output impedance less than 1 ohm, DC coupled.

2.4.2 DL OUT Connector

Positive unipolar 0 - 10 volts, 10.5 volts saturation into 93 ohms, single delay line clipped, risetime approximately 700 nanoseconds for optimum energy analysis; delayed from DDL OUT by 2.5 microseconds; output impedance less than 1 ohm, DC coupled.

2.4.3 PREAMP POWER Connector (Rear Panel)

Type Amphenol 17-10090 connector provides the low voltage DC necessary to power Canberra 1400 Series Preamplifiers. The voltages required are ±24VDC and ±12VDC.

SECTION 3
OPERATING INSTRUCTIONS

3.1 GENERAL

The purpose of this section is to familiarize the user with operating the controls and to check that the module is operating correctly. Since it is impossible to determine exactly how the user will operate his module in a specific experiment, explicit operating instructions can not be given. However, if the following procedures are performed, the user will become as familiar with the operation of the module as is possible.

3.2 SET UP

1. Insert the module in an AEC compatible bin such as the Canberra Model 1400.

2. Connect a +50mV output from a tail pulse generator to the INPUT connector of the module; observe the input specifications detailed in paragraph 1.3.

3. Connect an oscilloscope to the DDL OUT connector of the module. Terminate the amplifier output with 93 ohms at the oscilloscope input. This is done to prevent possible spurious ringing when driving a high load impedance with a long coaxial cable from the extremely low output impedance of the Model 1411.

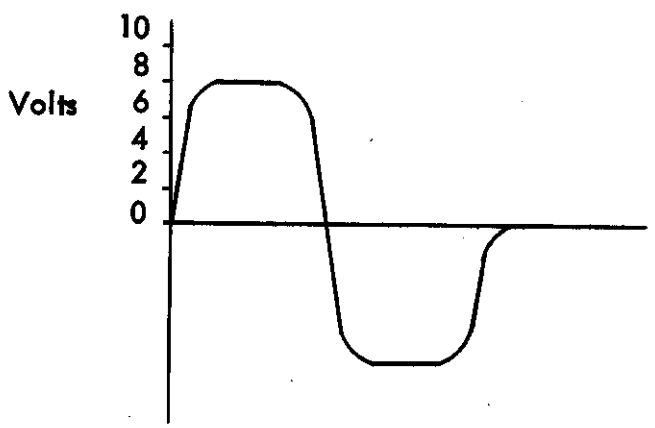
4. Set the COARSE GAIN control at 16.

5. Set the FINE GAIN control to the point at which the output pulse just saturates.

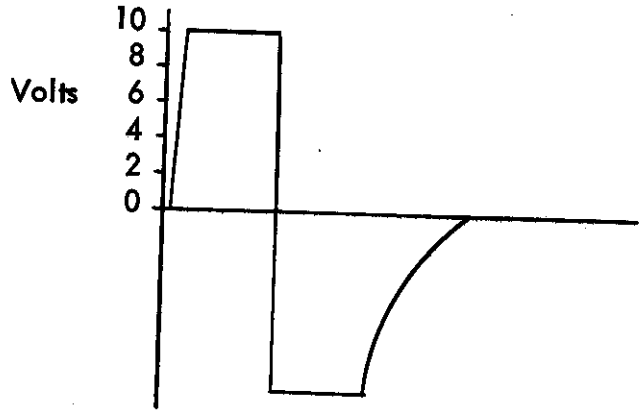
3.3 CHECKOUT PROCEDURE

3.3.1 INITIAL CHECKOUT

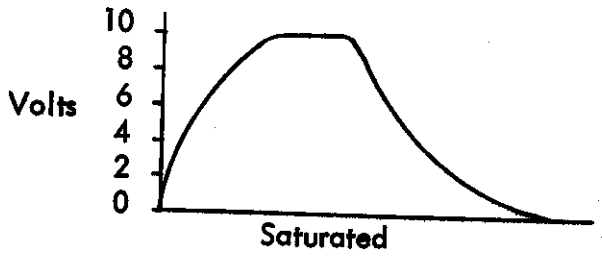
1. Having performed the operations in paragraph 3.2, observe that the DDL pulse shape is as follows:

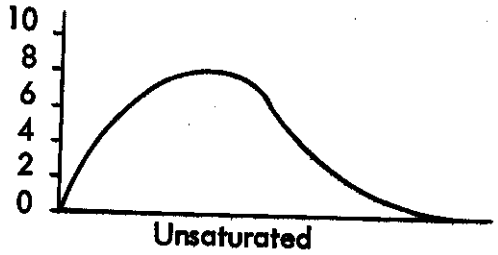


2. Increase the gain controls until the amplifier saturates; the pulse shape should appear as follows:



3. Connect the oscilloscope to the DL OUT connector. Note that the output signal is now unipolar (positive). Note also that the pulse has a longer rise due to delay line limitations.





4. Return to the DDL OUT connector.

5. Reduce the COARSE GAIN control to 8. Observe that the output is attenuated by a factor of 2. Rotate the FINE GAIN control and note that the output ranges from about 6 volts to about 1.5 volts, a 4:1 range.

6. Reduce the input amplitude to ten millivolts. Switch the COARSE GAIN control to 4, 8, 16, 32, and 64 noting that the output increases by factors of 2. Rotate the FINE GAIN control at each setting of the COARSE GAIN control and note that the output is variable from 1/4 maximum to full maximum at each COARSE GAIN setting.

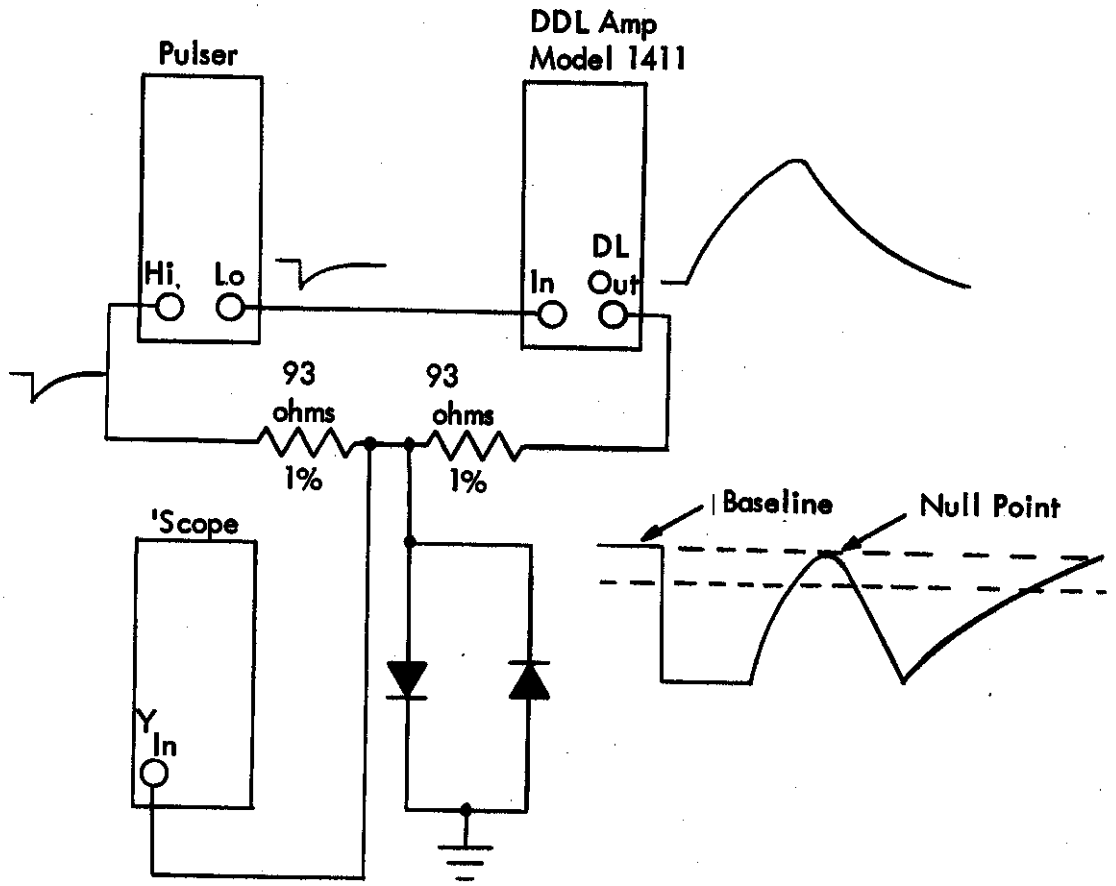
7. Set the gain controls at their maximum settings. The overall gain is approximately 1000. Observe an output of approximately ten volts for the ten-millivolt input.

8. Disconnect the input to the amplifier. Connect the DDL OUT to a Hewlett-Packard 400H or 400D (or equivalent) RMS voltmeter. Observe an RMS reading of less than 32 millivolts, or 32 microvolts referred to the input. Repeat for the DL OUT connector. Observe an RMS reading of less than ten millivolts, or ten microvolts referred to the input.

9. Insert a Kay attenuator (or equivalent) between the pulser and amplifier inputs. Terminate the input and output of the attenuator in 93 ohms (a pulser which has an output impedance of 93 ohms will serve as the attenuator input termination). Trigger the oscilloscope with the high-level output of the pulser. Adjust the output so that the amplifier just reaches saturation with no input attenuation. Switch 26db of attenuation in and out. With the oscilloscope set at maximum sensitivity (e.g., 0.05 volts/cm) and maximum time base which will allow crossover point to be observed, check that the crossover walk is less than ± [illegible] nanoseconds over 26db of attenuation (20:1 input range).

3.3.2 LINEARITY TEST

1. Set up the system as follows:



2. This test is performed by adjusting the pulser attenuator and amplifier gain so that with a ten volt high-level (Direct) output from the pulser, the output from the amplifier is also exactly ten volts. This may be ascertained by adjusting the attenuator and amplifier gain so that the null point observed on the oscilloscope (using the highest vertical gain) is at exactly the same level as the baseline.

3. When the condition described in step 2 is obtained, turn the pulser pulse height control down from ten volts to the lowest level that will still trigger the oscilloscope and observe the maximum difference between the baseline and the null point. The integral linearity of the amplifier under test is then equal to:

$$\frac{(\text{Maximum deviation, in volts}) \times 2 \times 100\%}{10\ (\text{volts})}$$

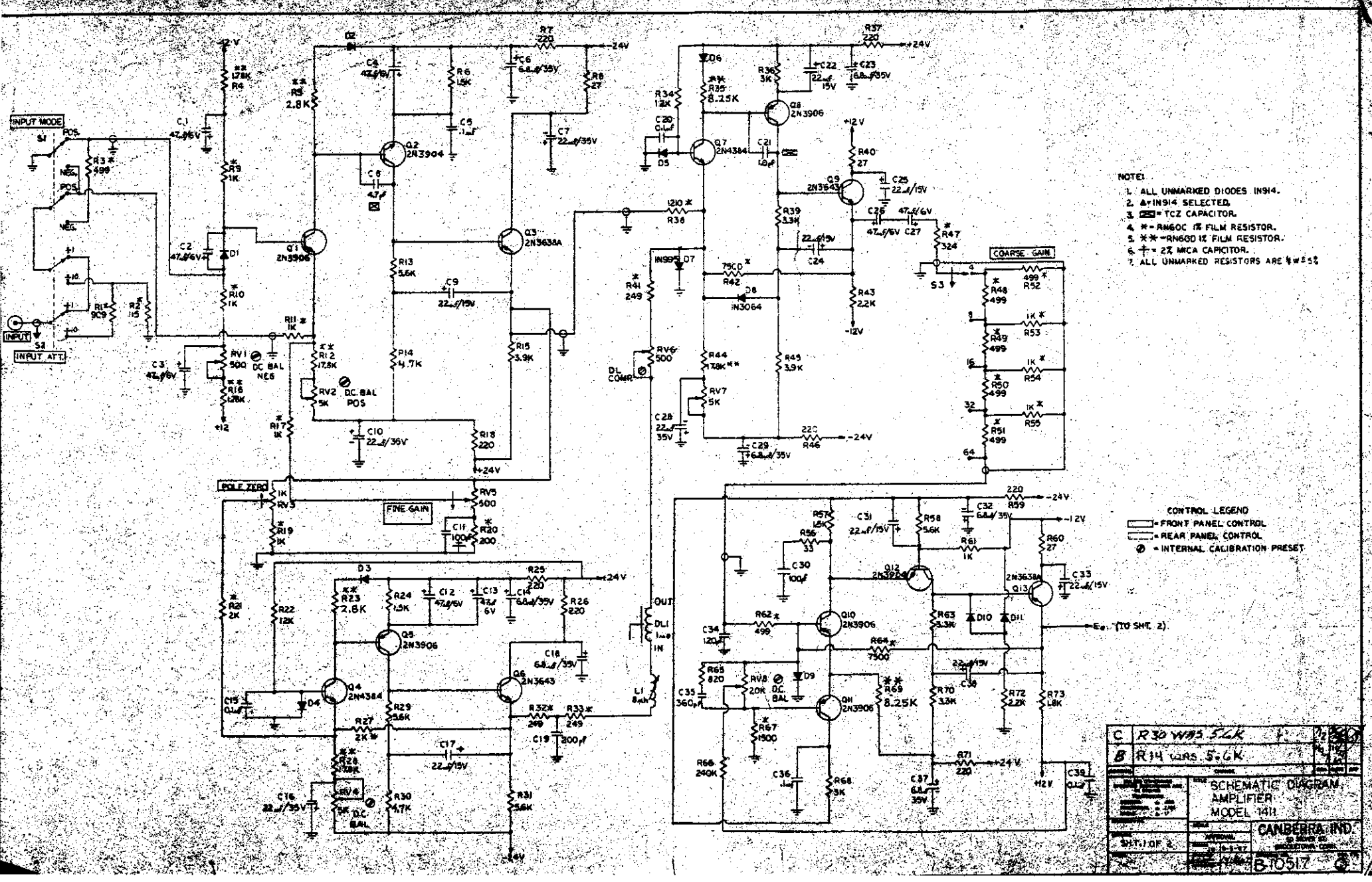
The maximum deviation must thus be less than 5mV in order to meet the 0.1% specification. The additional factor of two is added to compensate for the voltage division performed by the test circuitry.

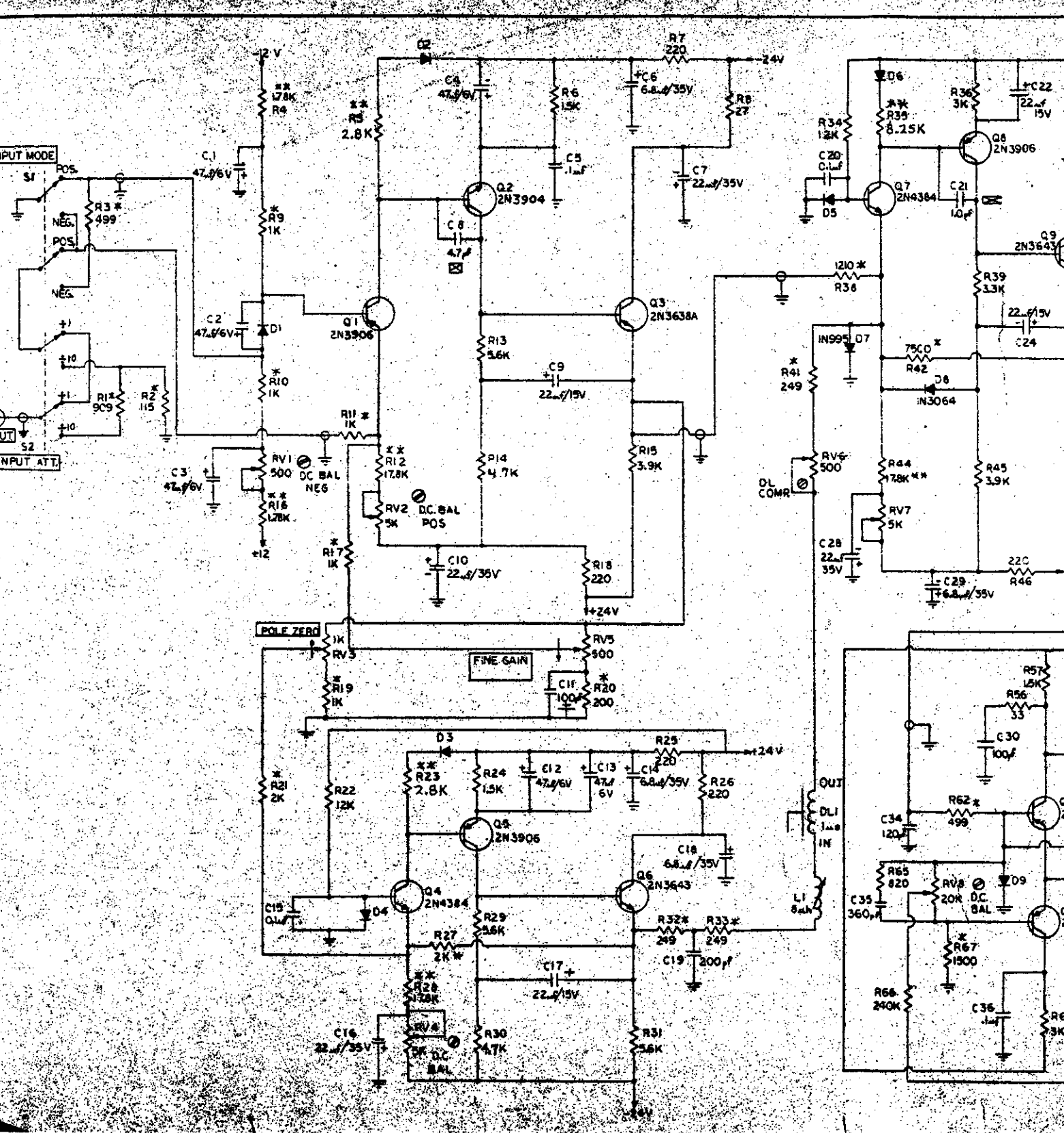
3.3.3 GAIN STABILITY TEST

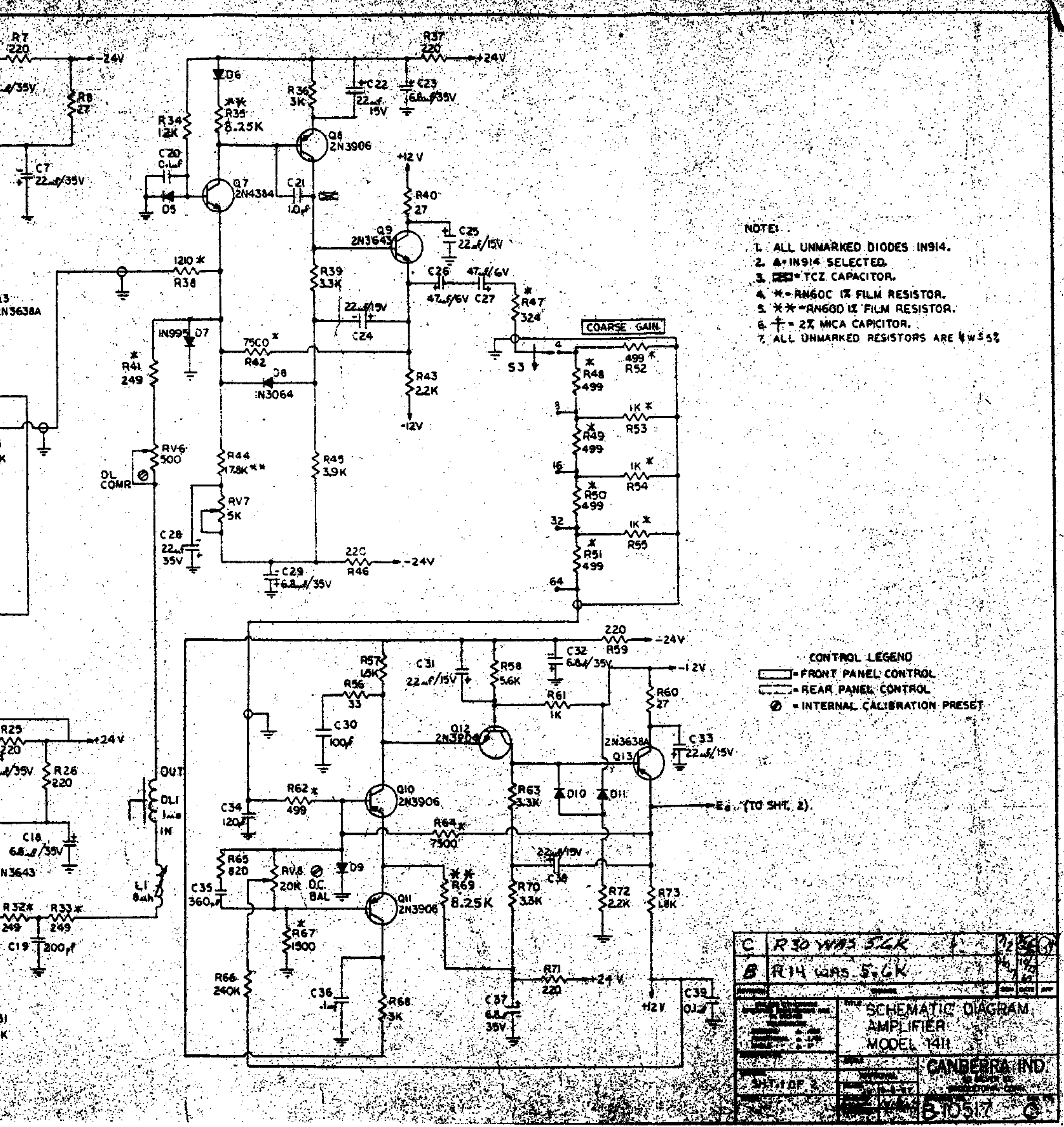
Because of the difficulty of assuring that the measuring instruments are stable and because of the relatively long test periods required, this test is extremely difficult to perform without somewhat elaborate test equipment.

Temperature stability can most simply be observed by duplicating the test setup of paragraph 3.3.2. However, it is necessary to place the Model 1411 in a temperature chamber. The effect of temperature changes may be observed by plotting the deviation between the baseline and null point versus chamber temperature. The calculation is performed as in paragraph 3.3.2 if the output of the Model 1411 is initially ten volts. A long-term stability test can also be performed in this manner if the pulser attenuator resistors and the summing circuit resistors are protected from temperature variations during the test period. This test is extremely tedious, as the oscilloscope does not record any excursions over time, and only the situation at the moment can be observed. Thus, constant observation is required.

The maximum deviation permitted for temperature is ± 0.5mV/°C; the maximum deviation over 24 hours is ± 1.0mV at constant temperature and power supply voltages if the initial amplifier output is ten volts.


INPUT MODE
S1
POS.
NEG.
INPUT
S2
INPUT ATT.
POLE ZERO
FINE GAIN
COARSE GAIN
S3
DC BAL NEG
DC BAL POS
DC BAL
DL COMP
OUT
DL
IN
CONTROL LEGEND
= FRONT PANEL CONTROL
= REAR PANEL CONTROL
= INTERNAL CALIBRATION PRESET
NOTE:
1. ALL UNMARKED DIODES IN914.
2. Δ=IN914 SELECTED.
3. TCZ = TCZ CAPACITOR.
4. * = RN60C 1% FILM RESISTOR.
5. ** = RN60D 1% FILM RESISTOR.
6. ┼ = 2% MICA CAPICITOR.
7. ALL UNMARKED RESISTORS ARE ¼W ±5%
C R30 WAS 5.6K
B R14 WAS 5.6K
SCHEMATIC DIAGRAM, AMPLIFIER MODEL 1411
CANBERRA IND.
SHT. 1 OF 2
B-10517


-12 V
D2
R7 220
+24V
C4 47µf/6V
R6 1.5K
+C6 6.8µf/35V
R8 27
R4 178K
R5 2.8K
C5 .1µf
C7 22µf/35V
Q2 2N3904
C8 4.7pf
C1 47µf/6V
R9 1K
INPUT MODE
S1
POS.
NEG.
R3 499
C2 47µf/6V
D1
Q1 2N3906
Q3 2N3638A
R13 5.6K
R10 1K
C9 22µf/15V
R11 1K
R1 909
R2 115
S2
INPUT ATT.
RV1 500
DC BAL NEG
C3 47µf/6V
R16 1.78K
R12 17.8K
RV2 5K
DC BAL POS
R14 4.7K
R15 3.9K
+12
R17 1K
C10 22µf/35V
R18 220
+24V
POLE ZERO
1K
RV3
RV5 500
FINE GAIN
R19 1K
C11 100pf
R20 200
D3
R25 220
+24V
R21 2K
R22 12K
R23 2.8K
R24 1.5K
C12 47µf/6V
C13 47µf 6V
C14 6.8µf/35V
R26 220
Q5 2N3906
C18 6.8µf/35V
Q4 2N4384
Q6 2N3643
C15 0.1µf
D4
R29 5.6K
R27 2K
R32 249
R33 249
C19 200pf
C17 22µf/15V
R28 178K
RV4 5K D.C. BAL
C16 22µf/35V
R30 4.7K
R31 5.6K
-24V
D6
R34 12K
R35 8.25K
R36 3K
+C22 22µf 15V
C20 0.1µf
Q7 2N4384
Q8 2N3906
D5
C21 10pf
Q9 2N3643
1210
R38
R39 3.3K
22µf/15V
C24
IN995
D7
7500
R42
R41 249
D8
IN3064
RV6 500
DL COMR
R44 178K
R45 3.9K
RV7 5K
C28 22µf 35V
220
R46
C29 6.8µf/35V
R57 1.5K
R56 33
C30 100pf
OUT
DLI 1µs
IN
R62 499
C34 120pf
R65 820
RV8 20K D.C. BAL
D9
C35 360pf
R67 1500
R66 240K
C36 .1µf
L1 8µh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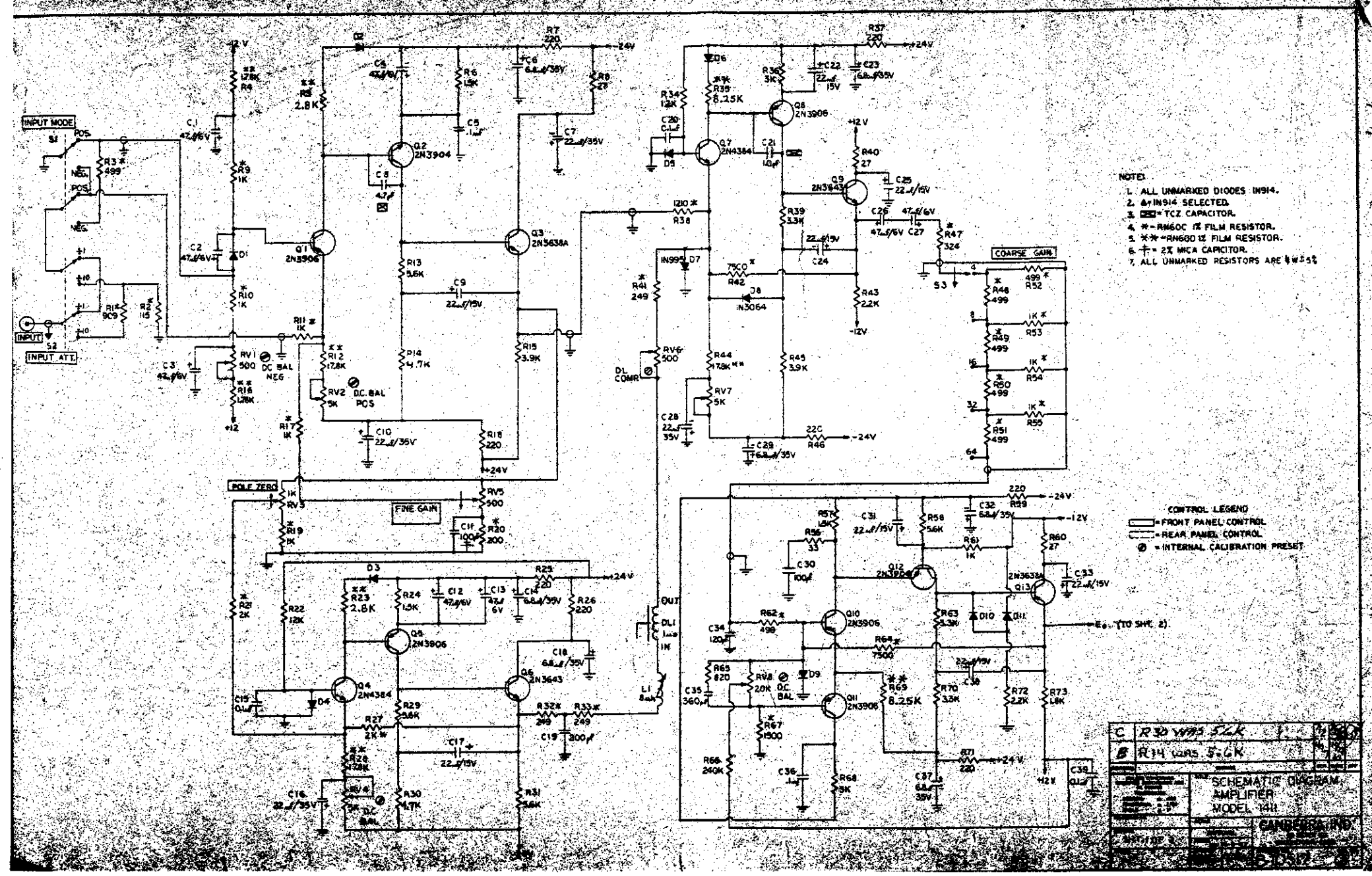
CONTROL LEGEND
= FRONT PANEL CONTROL
= REAR PANEL CONTROL
⊘ = INTERNAL CALIBRATION PRESET
COARSE GAIN
S3
DL COMR
DC BAL
E₀ (TO SHT. 2)
C R30 WAS 5.6K
B R14 WAS 5.6K
SCHEMATIC DIAGRAM
AMPLIFIER
MODEL 1411
CANBERRA IND.
SHT. 1 OF 2
B10517


INPUT MODE
S1
POS.
NEG.
INPUT
S2
INPUT ATT.
DC BAL NEG
DC BAL POS
POLE ZERO
FINE GAIN
COARSE GAIN
DL COMP
DC BAL
OUT
DLI IN
LI
CONTROL LEGEND
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= REAR PANEL CONTROL
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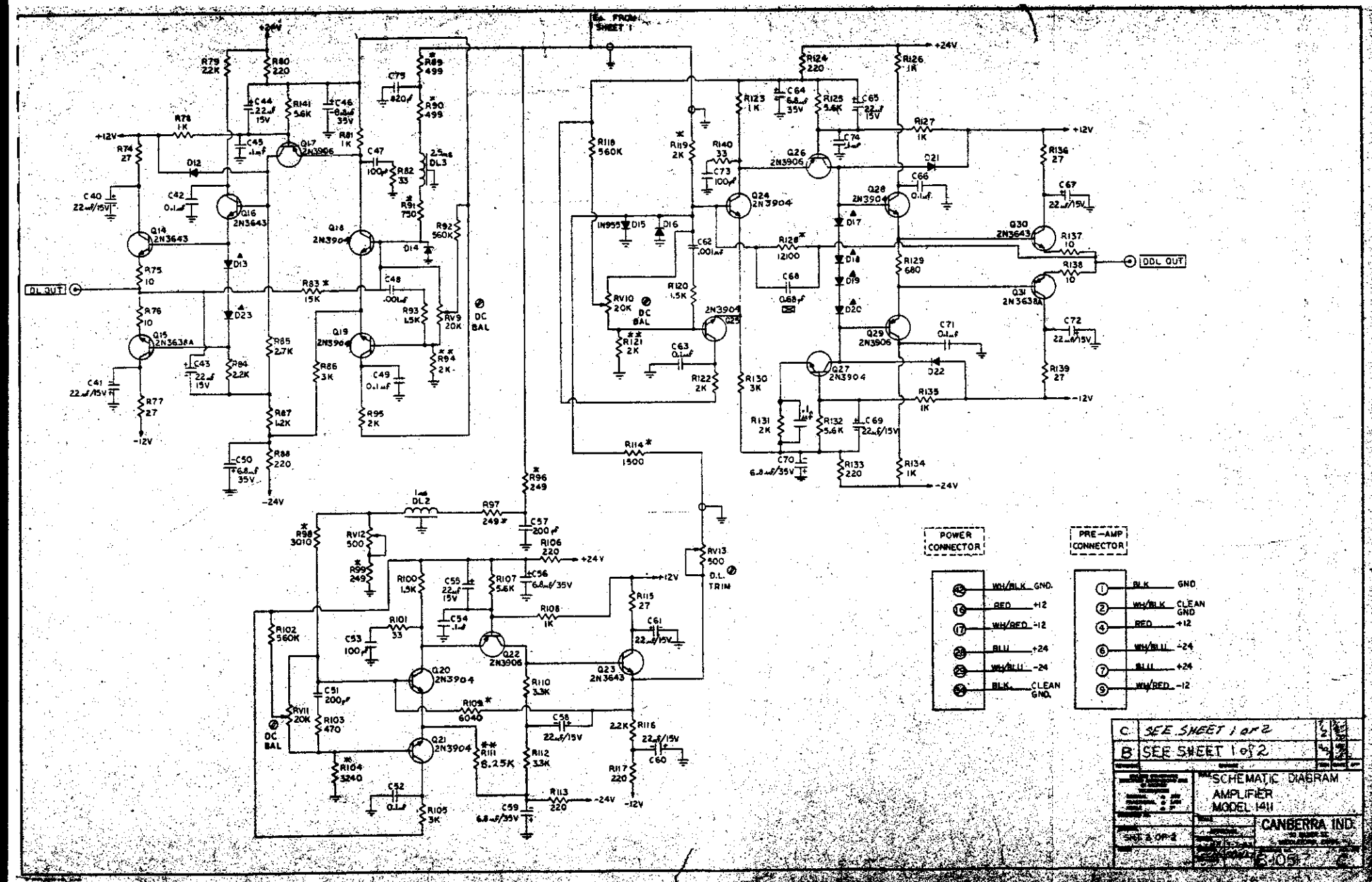
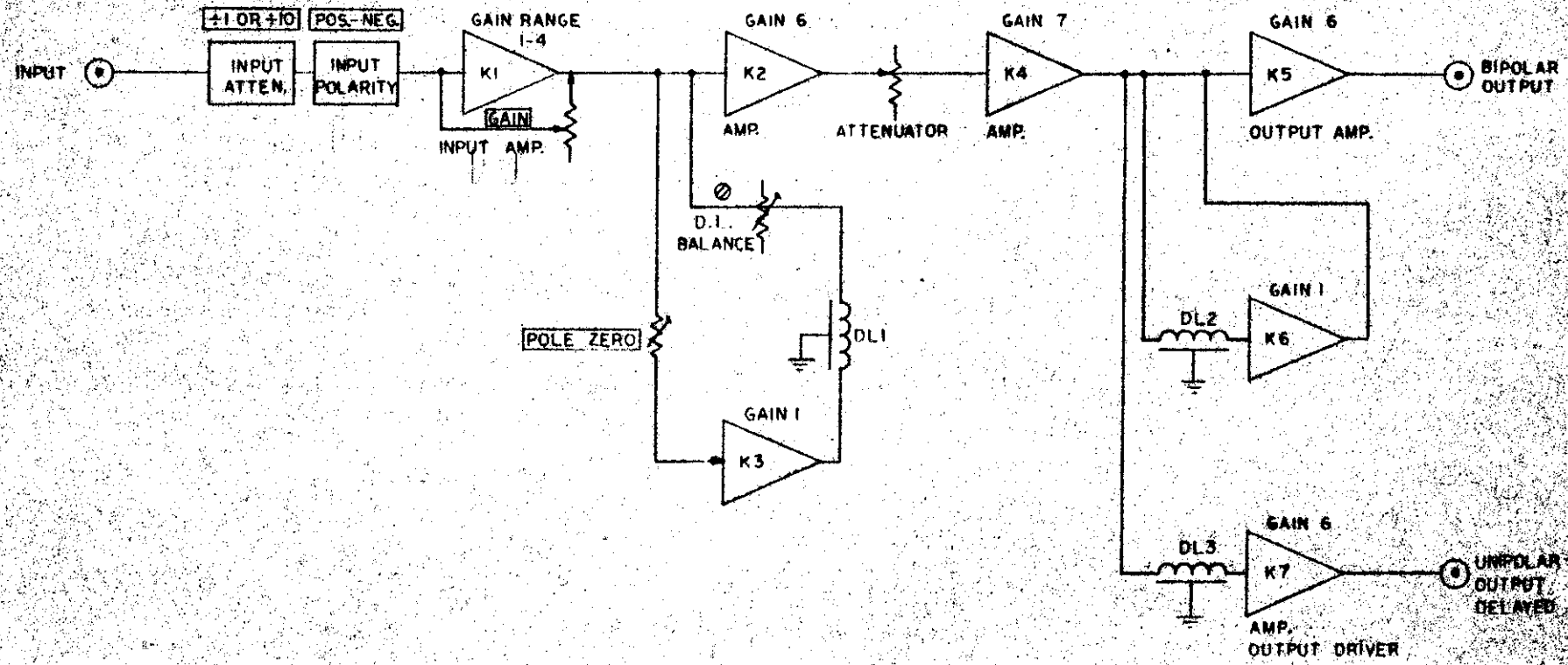
SCHEMATIC DIAGRAM
AMPLIFIER
MODEL 1411
CAMBRIDGE, MD.


FROM SHEET 1
+24V
+12V
-12V
-24V
DL OUT
DDL OUT
DC BAL
D.L. TRIM
POWER CONNECTOR
PRE-AMP CONNECTOR
16 WH/BLK GND.
16 RED +12
17 WH/RED -12
28 BLU +24
29 WH/BLU -24
9 BLK CLEAN GND.
1 BLK GND
2 WH/BLK CLEAN GND
4 RED +12
6 WH/BLU -24
7 BLU +24
5 WH/RED -12
C SEE SHEET 1 of 2
B SEE SHEET 1 of 2
SCHEMATIC DIAGRAM
AMPLIFIER
MODEL 1411
CANBERRA IND.
8105



BLOCK DIAGRAM
AMPLIFIER
MODEL 1411

CANBERRA IND.

C-10958