

The EG&G/ORTEC RC014 Real Time Clock is a very versatile preset counter designed to solve almost any timing problem encountered in experimental work. Unlike most real time clocks available from computer manufacturers, the RC014 is directed toward the experimental environment; it works as a link between the physical world and the program.

The key to the flexibility of RC014 is its ability to control and sense every operational step by Dataway commands and/or by front panel signals.

The experimenter and engineer will find the RC014 useful in preset-count and preset-time arrangements. The clock generator mode of the RC014 not only interrupts the processor at regular time intervals but also has pulses and other controls available for the experimental equipment. Still another unusual capability of the module is its function as an elapsed time meter.

Some of the valuable features of the RC014 are as follows:

1. The preset-time range is from 3.8  $\mu$ sec to 18.2 hr.
2. The preset-count range is from 1 count to  $2^{34}$  counts (more than  $17 \times 10^9$ ).
3. The resolution is 16 bits.
4. The clock generator rates are from 4 Hz to 1 cycle in 18.2 hr.
5. Readout on the fly allows the elapsed time after a start command to be monitored by Dataway operation while the timing cycle is still in progress.

6. Start and stop commands are by Dataway operations or by external pulses for high precision timing.

7. The start pulse and gate are available at the front panel even if started by a Dataway command.

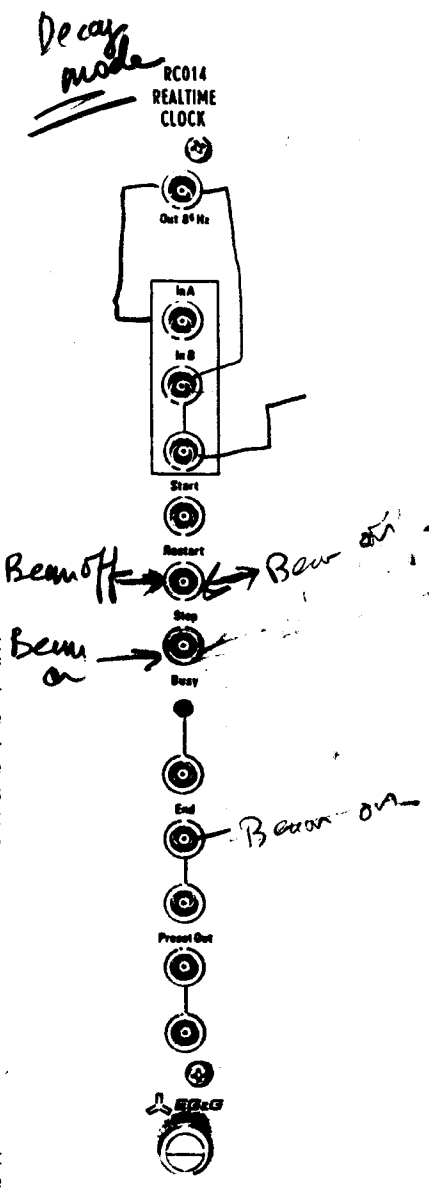
8. A front panel gate input is provided to control the flow of clock pulses into the counter for live-timing application.

9. All front panel signals are NIM-compatible to ease interfacing with fast nuclear instrumentation.

Figure 1 is a functional block diagram of the module. Some Dataway commands are shown, but a complete list appears in the Specifications.

A Dataway command loads the 16-bit counter with the one's complement of the word on the W bus. When the counter goes through zero again, it generates the End output. In front of the preset counter, a frequency divider steps down the input rate, and a control register holds the current step-down ratio. The input circuit is an arrangement that can be found in other scalars: In A is a normal  $50\Omega$  input; In B is a high-impedance bridging input, which maintains a "1" (-0.8 V) if left open and a "0" state if terminated in  $50\Omega$ . Since both inputs enter an AND-gate, either In A or In B can be used to feed count pulses or gate signals. An ungated mode of operation results when count pulses are fed into In A and In B is left open.

The crystal oscillator is an independent section; in all timing applications of the



RC014, the dotted line connection to In A must be made on the front panel.

Input of the counter is under control of the Busy flag. An externally supplied Start (or Restart) pulse or a Dataway command sets Busy, which starts the timing or the preset-count operation. The

end of the preset-time/count operation clears the Busy flag and sets the Done flag, which might issue an L request. For a more thorough discussion of the "busy-done" philosophy, please refer to the CT021 Data Sheet.

The Start input simply sets the Busy flag;

the counter is supposed to be correctly loaded. Restart also turns on Busy but clears the counter, too. In preset-time/count operations, the Start pulse, if not supplied by the physical equipment, can be derived from the counter load command through the dotted line connection to Start.

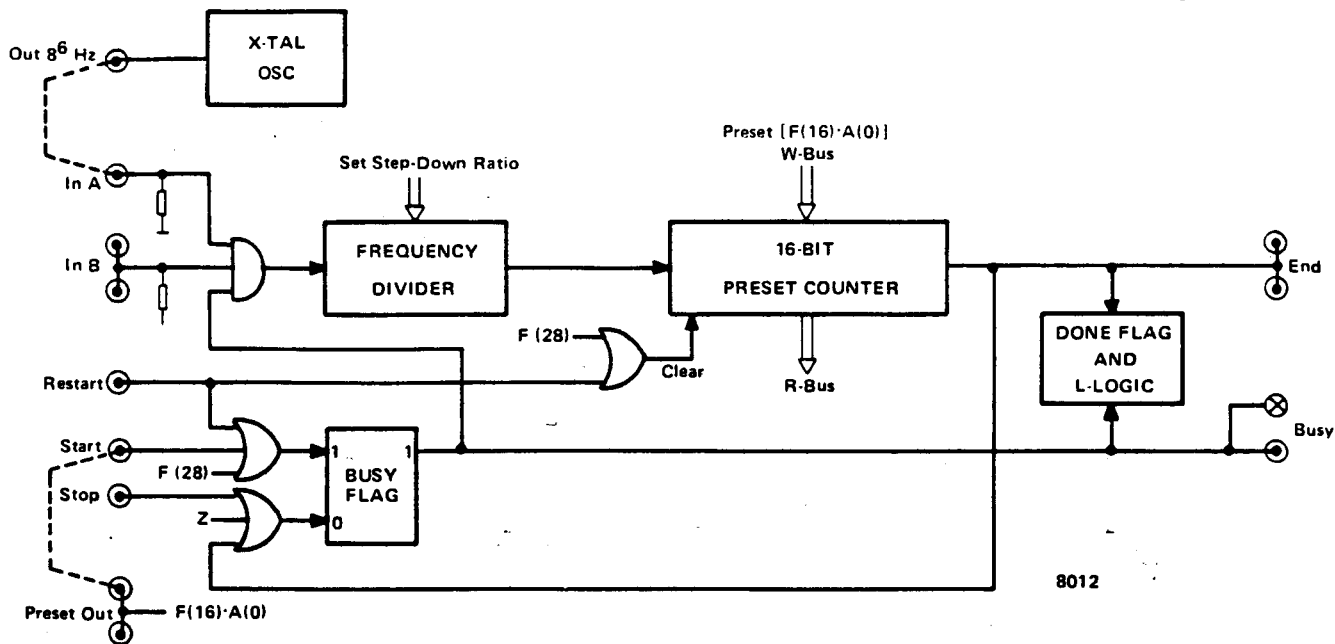


Figure 1

## SPECIFICATIONS

All inputs and outputs of the RC014 accept or deliver NIM-compatible levels or pulses. Output drivers sink 16 mA in the 1 state, and inputs accept  $-800$  mV as 1. (For more details refer to Table IX in TID-25875.) All connectors are LEMO RA 00 C50.

### INPUTS

**IN A** Input to the frequency divider; maximum pulse rate, 15 MHz at 50% duty ratio; minimum pulse width, 30 nsec; 50Ω impedance.

**IN B** Dual high-impedance input to the frequency divider; assumes 1 state when open. Maximum pulse rate, 15 MHz at 50% duty ratio; minimum pulse width, 30 nsec.

**START** Sets the Busy flag; 50Ω impedance; minimum pulse width, 50 nsec.

**RESTART** Sets the Busy flag and clears the preset counter; 50Ω impedance; minimum pulse width, 50 nsec.

**STOP** Clears the Busy flag; 50Ω impedance; minimum pulse width, 50 nsec.

### OUTPUTS

**OUT 8<sup>6</sup> Hz** Crystal oscillator,  $262,144 \pm 5$  Hz, generates an approximately symmetrical square wave. Overall stability:  $5 \times 10^{-4}$  (10 to 40°C).

**BUSY** Busy flag for external use, gives the exact duration of the timing or preset operation; a lamp shows the state of the busy flag.

**END** Generated whenever the preset counter is clear, especially at the completion of any preset operation or after a Restart pulse; double output (32 mA sink capability).

**PRESET OUT** Delivers a pulse with a width equal to S2 when the preset counter is loaded [F(16)·A(0)], double output (32 mA sink capability)

### CAMAC CODES

Note: F(16)·A(a) = Function (ff) with sub-Address (a).

**F(16)·A(1)** Write into the control register of the frequency divider; clear the frequency divider; produce a Q. Only one bit of the control register is allowed to be nonzero at a time. Step-down ratios are as follows:

Control Register* Bit	Step-Down Ratio	FULL SCALE
W1 1	$2^0$ (1)	1/4 Sec
W2 2	$2^3$ (8)	2
W3 4	$2^6$ (64)	16
W4 8	$2^9$ (512)	128
W5 16	$2^{12}$ (4096)	1024
W6 32	$2^{15}$ (32,768)	8192
W7 64	$2^{18}$ (262,144)	65536

\*If the Control Register is 0, the frequency divider will be inhibited.

**F(16)·A(0)** Write into the preset counter from W1 to W16; produce a Preset Out pulse, clear the Done flag; produce a Q.

**W1-W16** A binary integer; the number of time increments or pulses to be counted (multiplied by the step-down ratio). After this command,

the counting register holds the one's complement of this integer.

**F(28)-A(0)** Clear the preset counter; set the Busy flag; i.e., start counting. Clear the Done flag.

**F(0)-A(0)** Read the preset counter into R1 to R16; produce a Q.

**READ PROCESS** Stops the counter for a fraction of the Dataway operation (from  $t_0$  to  $t_1$ ; refer to Fig. 9 of TID-25875) in order to avoid ambiguous reading. A single pulse occurring during this interval is restored to the counter at S2. Thus readout on the fly is possible without loss if the reciprocal of the

pulse rate (after the divider) is larger than the interval  $t_0 - t_1$ . At higher rates the losses are generally negligible.

**F(27)-A(0)** Test the Busy flag; i.e., produce  $Q = 1$  if Busy is on.

**F(8)-A(0)** Test L produced by the Done flag; i.e.,  $Q = 1$  if Done is set and L is enabled.

**F(10)-A(0)** Test L as in F(8); clear the Done flag.

**F(26)-A(0)** Enable L.

**F(24)-A(1)** Disable L.

**Z** Initialize clears Busy and Done flags; clears the preset counter and the frequency divider; disables L.

## ELECTRICAL AND MECHANICAL

### POWER REQUIRED

+6 V, 640 mA;  
-6 V, 90 mA.

**PHYSICAL** Single-width CAMAC module with sheetmetal covers, Fiberglass circuit board and all TTL integrated circuits, meets all electrical and mechanical requirements of EUR 4100e and TID-25875.

## APPLICATIONS

### TIMER

After Start, Busy is on and available as a gate to external equipment (see Fig. 2). The completion of the timing operation is signaled to the program by an L request and to the experimenter by End and Busy. The Start command is supplied by either a pulse or a programmed command. In the latter case a connection Preset Out-Start must be established. Figure 3 shows the effect of a Stop command during the timing operation.

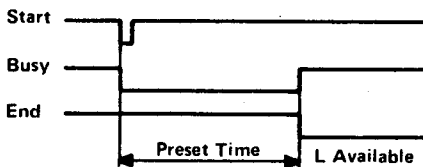


Figure 2

The output of the time base oscillator, Out 8<sup>6</sup> Hz, should be connected to In A. When a pulse train other than the time base oscillator is supplied to In A (or In B), the timer becomes a preset counter.

### CLOCK GENERATOR

Making a connection from Out 8<sup>6</sup> Hz to

In A and feeding End back to Restart provide a free-running clock generator. Pulses of about 100-nsec duration are available at the End output. The clock rate is dependent only upon the step-down ratio:

Step-Down Ratio	Clock Period
2 <sup>0</sup>	1/4 s
2 <sup>3</sup>	2 s
2 <sup>6</sup>	16 s
2 <sup>9</sup>	128 s
2 <sup>12</sup>	1024 s
2 <sup>15</sup>	8192 s
2 <sup>18</sup>	65536 s

At the end of every period, an L request is issued which may be used to interrupt the current program in the processor. Provision must be made to service the

interrupt before the next clock period.

### ELAPSED TIME METER AND DAYTIME CLOCK

The readout on the fly and the front panel commands allow many useful arrangements. The elapsed time meter measures the time between an initial event ( $t_0$ ) and a second event ( $t_1$ ). The instants  $t_0$  and  $t_1$  are sometimes given by pulses ( $t_0$  into Restart and  $t_1$  into Stop) or are defined by the program, say, in response to a certain interrupt routine. The program then uses F(28) at  $t_0$  and reads the counter on the fly at  $t_1$  by function 0. High-resolution timing, however, is possible only with pulse commands. Once started at  $t_0$ , the current counter content can be transferred to the processor as often as desired. A hardware daytime clock results.

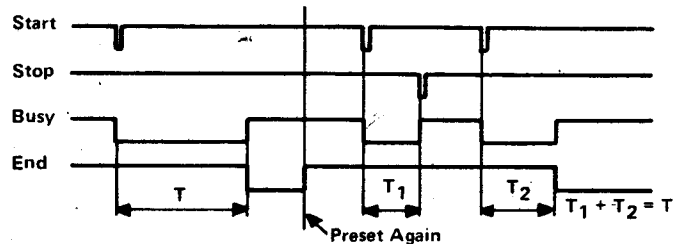


Figure 3