ORTEC

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INSTRUCTION MANUAL

437 TIME TO PULSE HEIGHT CONVERTER

ORTEC®

INSTRUCTION MANUAL
MODEL 437
TIME TO PULSE HEIGHT CONVERTER

Serial No. ____________________

Purchaser ____________________

Date Issued ____________________

ORTEC INCORPORATED
P. O. BOX C
OAK RIDGE, TENNESSEE 37830
Telephone (615) 483-8451
TWX 810-572-1078

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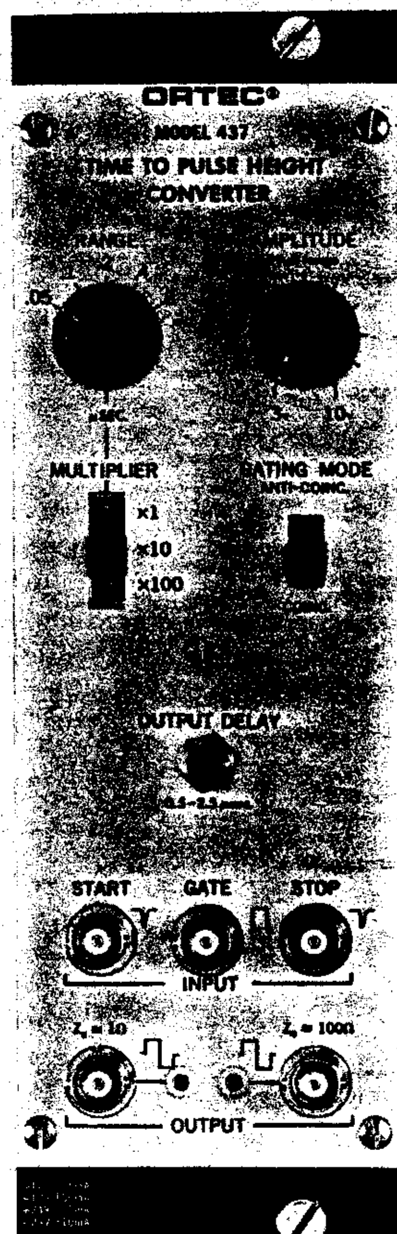

ORTEC®
MODEL 437
TIME TO PULSE HEIGHT CONVERTER
RANGE
AMPLITUDE
MULTIPLIER
×1
×10
×100
GATING MODE
ANTI-COINC.
OUTPUT DELAY
START
GATE
STOP
INPUT
OUTPUT

MODEL 437
TIME TO PULSE HEIGHT CONVERTER

1. DESCRIPTION

The Model 437 Time to Pulse Height Converter is a general-purpose laboratory instrument capable of providing output signals which have their amplitudes linearly proportional to the time difference between start and stop inputs. Design features of the ORTEC converter permit unique versatility for a wide variety of experiments. The instrument combines excellent time resolution, temperature stability, linearity, and dc coupling, in a start-stop converter of very wide dynamic range; with such features as a bipolar output signal with continuously variable amplitude and delay, and built-in fast discriminators which may be externally gated either in the coincidence or anti-coincidence mode.

At the start and stop inputs of the 437, 250 millivolt or larger negative signals are accepted. These signals need no preliminary limiting or discrimination. The start pulse, after amplification and inversion, switches a tunnel diode to its high voltage state (see block diagram, Dwg. No. 437-0101- B). The start tunnel diode in this state performs two functions. The first function is to allow the acceptance of a stop pulse. The second function is to switch the conversion clamp permitting a constant current to charge a capacitor. This constant current charge continues until either a stop pulse is received or until the capacitor charges to a voltage indicating full range. Receipt of a timely stop pulse switches the stop tunnel diode to its high voltage state. The stop tunnel diode in this state switches the current source off holding the voltage on the capacitor until a read interval has been completed. Completion of a read interval or indication of a full range charge without a stop triggers a reset of the start and stop tunnel diodes to their no input signal states. The converter is then ready to accept another start pulse.

At the gate input, 2.0 volt or larger positive signals are accepted. With the GATING MODE on coincidence, only start signals coincident with the gate signal are accepted as valid starts. With the GATING MODE on anticoincidence, the start input is normally accepted, but may be disabled by a coincident gate input. Both of these modes function by control of the current level of the start tunnel diode.

The amplification and processing of the converted signal on the capacitor provides a very versatile output signal. Variable gain control and variable delay on the gated time signal makes available a 3 to 10-volt full scale signal delayed 0.5-2.5 μsec following receipt of an accepted stop signal. Also, the signal is rendered bipolar by delay line shaping.

The ORTEC 437 is a double-width standard module (2.35 inches wide and 8.75 inches high). Power is obtained from a Model 402 Power Supply via an ORTEC 401 modular bin, which is capable of providing power and rack space for twelve module widths.

2. SPECIFICATIONS

General

Time Ranges: Switch selectable, 15 range choices — 0.05, 0.1, 0.2, 0.4, 0.8 µsec, X1, X10, X100

Time Resolution: 10 ps fwhm or 0.01% range, (whichever is greater)

Temperature Stability: ≤±0.015% or 10 psec/°C (the greater of), 0-50°C

Linearity: ≤2% differential, from the larger of 15 ns or 10% of range to 100% of range; integral, ~0.1%

Input Count Rate: Limited only by input pulse width. All inputs are direct-coupled and non-paralyzable.

Start Rate: Max ≥3 x 10^6 c/sec random rate

Stop Rate: ≥30 x 10^6 c/sec fixed rate

Gating Modes: Start input may be coincidence or anticoincidence gated, switch selectable

Output Signal Delay: ≈0.5 to 2.5 µsec

Controls

Range: 5 position switch, 0.05, 0.1, 0.2, 0.4, 0.8 µsec

Range Multiplier: 3 position switch (X1, X10, X100)

Gating Mode: 2 position switch (coincidence-anticoincidence)

Amplitude: 1-turn potentiometer (3V to 10V FR)

Output Delay: 1 turn potentiometer (≃ 0.5 — 2.5 µsec)

Inputs

Start: Negative threshold ~250 mV, dc-coupled, impedance 50 ohms ±10% to ±100V, width ≥2 nsec; time slewing ~0.8 nsec from 2X to 20X threshold

Stop: Same as start input, but enabled only by start of a conversion. Valid stop generates a "Read" signal which allows analysis of conversion.

Gate: Positive, dc-coupled, 2V minimum, protected to ±100V, impedance ~1K, gates START input, controlled by GATING MODE switch. Analyzer "Busy" or "$\overline{\text{Busy}}$" may be used as input.

Outputs:

Delayed, (continuously variable 0.5-2.5 µsec) following usable stop, constant pulse shape, independent of range or amplitude

Output A: Bipolar, positive portion leading, variable amplitude, 3V to 10V full range (open circuit) 1.5 to 5V full range (100 ohm load), Z_o = 100 ohms

Output B: Same as Output A, except 1 ohm source impedance

Connectors: All signals are BNC, UG-1094/U

Power Requirements:	74 mA at +24V
	107 mA at - 24V
	92 mA at +12V
	98 mA at - 12V

3. INSTALLATION INSTRUCTIONS

3.1 General

The 437, used in conjunction with ORTEC 401/402 Bin and Power Supply, is intended for rack mounting, and therefore it is necessary to ensure that vacuum tube equipment operating in the same rack has sufficient cooling air circulating to prevent any localized heating of the all-transistor circuitry used throughout the 437. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are taken; The 437 should not be subjected to temperatures in excess of 120°F (50°C).

3.2 Connection to Power — Nuclear Standard Bin, ORTEC 401/402

The 437 contains no internal power supply, and therefore must obtain power from a Nuclear Standard Bin and Power Supply such as the ORTEC 401/402. It is recommended that the Bin power supply be turned off when inserting or removing modules. The ORTEC 400 Series is designed so that it is not possible to overload the Bin power supply with a full complement of modules in the Bin; however, this may not be true when the Bin contains modules other than those of ORTEC design. In this case, power supply voltages should be checked after the insertion of modules. The 401/402 has test points on the power supply control panel to monitor the dc voltages.

3.3 Connection Into A System

Start and stop signals should be provided to the time converter via 50-ohm coaxial cables. Connection of either output should be performed using 93-ohm signal cable. In this case, the 1-ohm output provides a 3V to 10V full range signal and the 100-ohm output provides a 1.5V to 5.0V full range signal, when the cable is terminated at the receiving end. No input or output connectors need to be terminated when not in use.

In any experiment where the count rate on one input is very much greater than the count rate on the other input, the low count rate should be used as a start signal. This assures that the converter spends the least amount of time processing unnecessary data and therefore its dead time is reduced. The time measured is then the delay time minus T, which is the so-called inverted time spectrum. This same rule holds true for fixed stop rates such as with electrostatic pulsed accelerators. The reasoning behind this is that for each signal which is accepted as a start signal, there must be a conversion; however, for each signal which enters as a stop signal, there need not be a conversion. For each start signal which enters the converter and which is not accompanied by a corresponding stop signal, the converter will measure a time equal to the range selected, even though the information is not presented to the output.

3.4 Linear Output Signal Connections and Terminating Impedance Considerations

The source impedance of the 0-10 volt standard linear outputs of most 400 Series modules is approximately 1 ohm. Interconnection of linear signals is, thus, non-critical since the input impedance of circuits to be driven is not important in determining the actual signal span, e.g., 0-10 volts, delivered to the following circuit. Paralleling several loads on a single output is thereofre permissible while preserving the 0-10 volt signal span. Short lengths of interconnecting coaxial cable (up to approximately 4 feet) need not be terminated. However, if a cable longer than approximately 4 feet is necessary on a linear output, it should be terminated in a resistive load equal to the cable impedance. Since the output impedance is not purely resistive, and is slightly different for each individual module, when a certain given length of coaxial cable is connected and is not terminated in the characteristic impedance of the cable, oscillations will generally be observed. These oscillations can be suppressed for any length of cable by properly terminating the cable either in series at the sending end or in shunt at the receiving end of the line. To properly terminate the cable at the receiving end, it may be necessary to consider the input impedance of the driven circuit, choosing an additional parallel resistor to make the combination produce the desired termination resistance. Series terminating the cable at the sending end may be preferable in some cases where receiving end terminating is not desirable or possible. When series terminating at the sending end, full signal span, i.e., amplitude, is obtained at the receiving end only when it is essentially unloaded or loaded with an impedance many times that of the cable. This may be accomplished by inserting a series resistor equal to the characteristic impedance of the cable internally in the module between the actual amplifier output on the etched board and the output connector. It must be remembered that this impedance is in series with the input impedance of the load being driven, and in the case where the driven load is 900 ohms, a decrease in the signal span of approximately 10% will occur for a 93-ohm transmission line. A more serious loss occurs when the driven load is 93 ohms and the transmission system is 93 ohms. In this case, a 50% loss will occur. BNC connectors with internal terminators are available from a number of connector manufacturers in nominal values of 50, 100, and 1000 ohms. ORTEC stocks in limited quantity both the 50 and 100 ohm BNC terminators. The BNC terminators are quite convenient to use in conjunction with a BNC tee.

4. OPERATING INSTRUCTIONS

Four controls are present on the 437. Two of these, the RANGE and RANGE MULTIPLIER, determine the upper limitation on the time between start and stop inputs for conversion to take place. For example, with the RANGE switch set to 0.05μsec after a start signal is converted to a pulse amplitude available at both of the outputs. The magnitude of the signal can be controlled by the AMPLITUDE potentiometer. Using the same RANGE and RANGE MULTIPLIER selections as before, the amplitude of the output signal for a 5.0μsec difference between start and stop inputs can be varied from 3V to 10V. The GATING MODE switch determines the control on the start input. In the Coincidence Mode a positive 2-volt or larger signal enables the receipt of a concurrent start signal. In the Anticoincidence Mode, the start input is normally enabled, but may be disabled, by a positive 2-volt concurrent signal. Since the Gate input is also dc-coupled, the converter may be completely controlled by the ADC if so desired. This, however, will rarely be an advantage because most of the ADC's now have reasonably good linear gates and self-gate themselves.

5. CIRCUIT DESCRIPTION (See Drawings 437-0101-S, 437-0101-B, 437-0102-B and Timing Diagrams "A" and "B")

The circuit containing diodes D1 and D2 and resistors R1 through R5 forms a limiter circuit that limits the voltage at the base of Q1 to 700 millivolts for input voltages up to 100 volts. A 250 millivolt or larger negative input signal when amplified by the amplifier composed of Q1 and Q2 causes the tunnel diode D4 to switch from its low voltage state to its high voltage state of about -0.5 volt. The tunnel diode remains in its high voltage state until a reset signal is received from Q25. The -0.5 volt signal at the base of Q3 switches the current of Q4 through Q3. This current is sufficient to reverse the current switch composed of Q5 and Q6 so that the current of Q6 flows through Q5. Current through Q5 turns Q9 off, allowing the constant current from Q35 to start charging the selected timing capacitor C7, C8 and C9, or C10 linearly. The voltage at the base of Q9 is limited to approximately negative 3 volts by the circuitry associated with Q7. Therefore, the voltage on the capacitor is limited to -3.6 volts. The amplifier, composed of transistors Q10 to Q14, furnishes two outputs. One is a positive voltage at the collector of Q14 which is used to control the over-range trigger. The second output is a negative voltage at the gate of Q11, which for a timely stop signal is amplified and shaped by the output amplifiers. The closed-loop voltage gain from Q10-G to Q11-G is unity.

If it is assumed that a stop signal was not obtained within the selected range time, the Schmitt Trigger formed of Q27 and Q28 triggers at about 3.0 volts. Thus, when the signal at the selected timing capacitor reaches -3.0 volts, an over-range is created. The over-range triggers the reset switch composed of transistors Q23 to Q26. The reset switch then causes the start tunnel diode to return to its low state.

If a timely stop signal is received, however, the process is quite different. Diodes D15 and D16 and resistors R81 to R85 form a limiter circuit for the stop input similar to that for the start input. The transistor pair Q29 and Q30 will cause the stop tunnel diode D19 to switch to its high voltage state only if the unit is in the process of conversion, i.e., a start signal arrived previously within the selected range time. The tunnel diode in its high voltage state switches the transistor pair Q32 and Q33. Q32 and Q33 in this state perform two functions. The first is that the current through Q35 is switched to Q34; and therefore, the capacitor C7, C8 and C9, or C10 holds the voltage that it has charged to. The second function is to trigger the read timer composed of transistors Q37 to Q40. The read timer is triggered by Q32 and Q33 after a variable delay time (0.5 — 2.5μsec) provided by R153 and C29.

The read timer also performs two functions. The first is to hold the linear gate open for the read time of about one microsecond. This read time is determined by C37 and R119 plus R120 and can be varied by the potentiometer R120. The second function is to trigger the reset switch at the end of the read time. The reset switch at this time then switches the start tunnel diode D4 to its low state and prevents it from triggering again for a period of approximately 4µsec. This prevents pile-up from occuring. Resetting of D4 forces Q3, Q4, Q5, Q6, and Q31 to switch the stop tunnel diode D19 to its low state.

The signal at the linear gate, composed of Q15 and the associated components, is equal in magnitude to the signal that is being held on the timing capacitor. This signal is therefore proportional to the time between start and stop inputs since the capacitor was charged by a constant current source. With the linear gate open, this signal is fed to the output amplifier. The transistor Q16 is used as an emitter-follower to provide high impedance at the linear gate. Transistors Q17 to Q19 form a feedback amplifier with a gain of minus one to drive the one microsecond delay DL-1. The input and output signals of this amplifier are then added to form the input to the output amplifier. Transistors Q41 to Q45 make up the output amplifier loop. Variable gain from unity to 3.3 is provided by varying the amplitude potentiometer R126. Therefore, for full range time conversions the output may be varied from 3 to 10 volts.

The circuitry not yet described is the logical gating circuitry. The effect the GATE input has on the system is an additional control on the start tunnel diode D4. Diodes D8 and D9 and resistors R55 to R59 form a limiter circuit that limits the voltage at the base of Q20 to 3 volts for input voltages to 100 volts. For the gate control switched to ANTICOINCIDENCE, Q20 is normally "off" and Q22 is "on"; thus the tunnel diode, D4, can accept a start input. If a positive signal greater than 2 volts arrives at the GATE input, Q20 becomes conducting, Q22 turns off and the start tunnel diode can not switch to its high state. When the GATE control is switched to COINCIDENCE, Q21 is normally on and Q22 is off; thus the start tunnel diode will not accept a start input. If a positive signal greater than 2 volts arrives at the gate input, Q21 turns off, Q22 turns on and allows the processing of a start signal during the period of the gating signal.

6. MAINTENANCE INSTRUCTIONS

6.1 Testing Performance

6.1.1 Introduction

The following test descriptions are intended as an aid in the installation and checkout of the 437.

6.1.2 Test Equipment

The following test equipment can be used to perform each of the tests described.

1. Hewlett-Packard 222A Pulse Generator
2. ORTEC 417 Fast Discriminator
3. ORTEC 416 Gate and Delay Generator
4. ORTEC 408 Biased Amplifier
5. ORTEC 260 Time Pickoff Unit
6. ORTEC 403 Time Pickoff Control
7. Monsanto 1000 Counter Timer
8. Tektronix Type 585 Oscilloscope
9. Multichannel Pulse Height Analyzer
10. Fan-In Unit

In each of the tests outlined, reference will be made to this equipment by description and above number. However, an equivalent piece of equipment may be substituted for any of those listed.

6.1.3 Preliminary Procedures

1. Visually check module for possible damage due to shipment.
2. Connect ac power to Nuclear Standard Bin, e.g., ORTEC 401/402.
3. Plug module into Bin and check for proper mechanical alignment.
4. Switch ac power and check the dc power voltages at the test points on the 401 Power Supply control panel.

6.1.4 Conversion Tests

A simple method of testing the 437 for proper operation is to supply a start signal and a stop signal of known time difference and observe the output. A typical test setup is shown in Fig. 1. A delay of about 0.4μsec should be set on the delay unit. The RANGE MULTIPLIER of the 437 should be in the X10 position and the RANGE SELECTOR in the .05μsec position. Check to ensure that the GATING MODE of the 437 is anti-coincidence. With the AMPLITUDE control in its maximum position, a bipolar signal of approximately 8 volts amplitude should be observed on the oscilloscope. Switching the RANGE SELECTOR from the 0.05μs to 0.8μs position should decrease the pulse amplitude one half for each scale change. Return the RANGE SELECTOR to the 0.05µs position. Switching the RANGE MULTIPLIER to the X100 position should decrease the output pulse amplitude to about 0.8 volt. Switching the RANGE MULTIPLIER to the X1 position should eliminate the presence of an output signal. The procedures described basically test the entire operation of the converter.

6.1.5 Resolution Tests

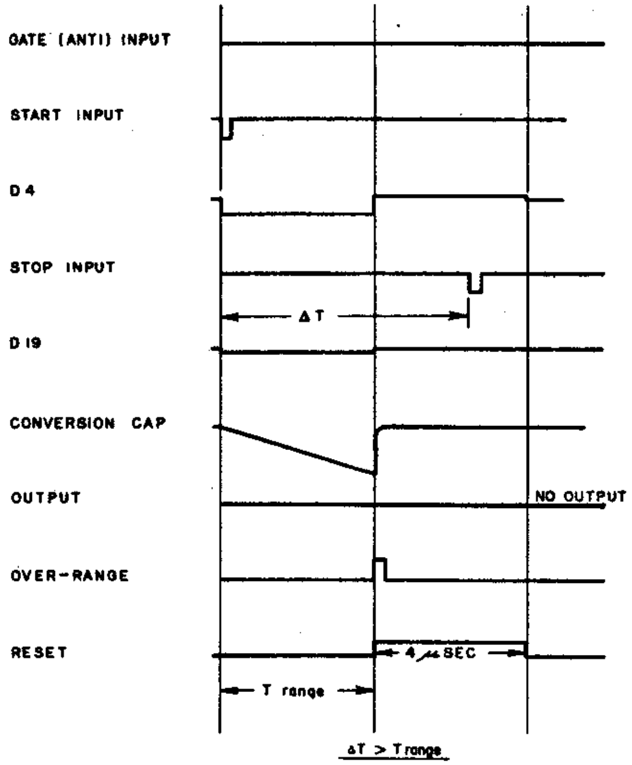
To test the instrumental resolution of the converter, it is necessary to provide start and stop pulses which have fast rise times and are jitter free. A block diagram of a typical test setup is shown in Fig. 2. The minimum time difference the converter can measure is approximately 15 nanoseconds, independent of the width of the start input signal. For this reason, the delay of the stop signal should be greater than 20 nanoseconds. The resolution of any scale can be measured with this setup. The only stipulation is that the stop signal delay be within the linear region of the range setting determined from the Range Selector and Range Multiplier. With this setup, the output signal may be analyzed obtaining a pulser spectrum. Then, a known amount of delay may be inserted into either the start or stop signal line, thus shifting the spectrum a certain number of channels. The converter resolution is then given by the full width at half maximum of either peak, multiplied by the time per channel. The time per channel is obtained by dividing the inserted delay time by the number of channels that the centroid of the time spectrum is shifted.

6.1.6 Count Rate Tests

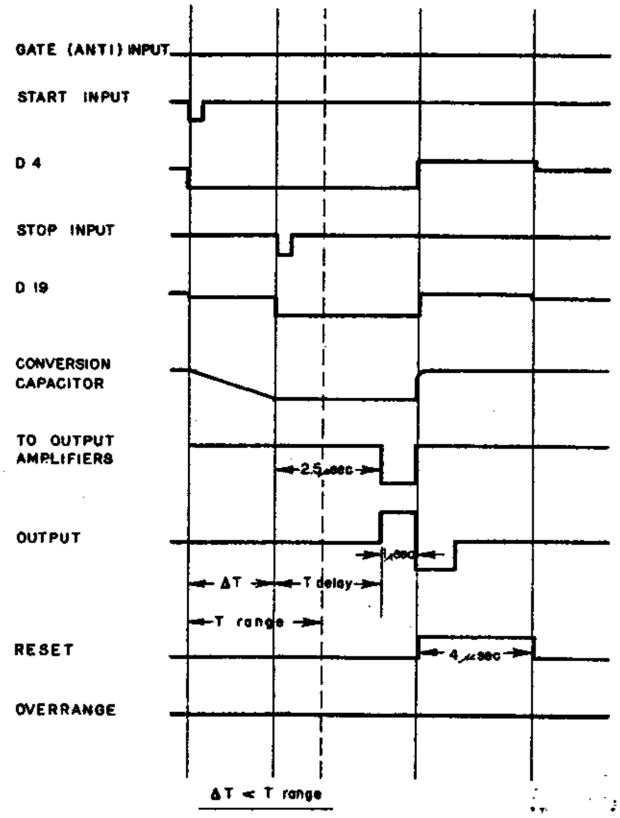
In many applications, it is important for a time to pulse height converter to handle high internal as well as external count rates. A system setup that will test the 437 under high internal count rates is shown in Fig. 3. Normally, the count rate capability is limited by the pile-up or baseline shifting associated with the coupling capacitors; however, in the 437 the conversion circuitry is all direct-coupled, and therefore, count rate is independent of pile-up since no pile-up occurs. Since the start input is pulse width. The limit on internal count rate is imposed by the conversion and reset process. For each accepted start input, the dead time is the selected range time plus 4µsec for events without an associated stop signal, and the measured time plus approximately 7µsec for an event within range time. The internal limit should only impose a system dead-time.

6.1.7 Differential Linearity Measurements

A method of testing the 437 for differential linearity is depicted by the block diagram of Fig. 4. Since the start signal is random in time, the output signal will be random in amplitude. Therefore, for perfect differential linearity and an infinite number of random inputs,



Timing Diagram "A" ($\Delta T > T_{range}$)



Timing Diagram "B" ($\Delta T < T_{range}$)

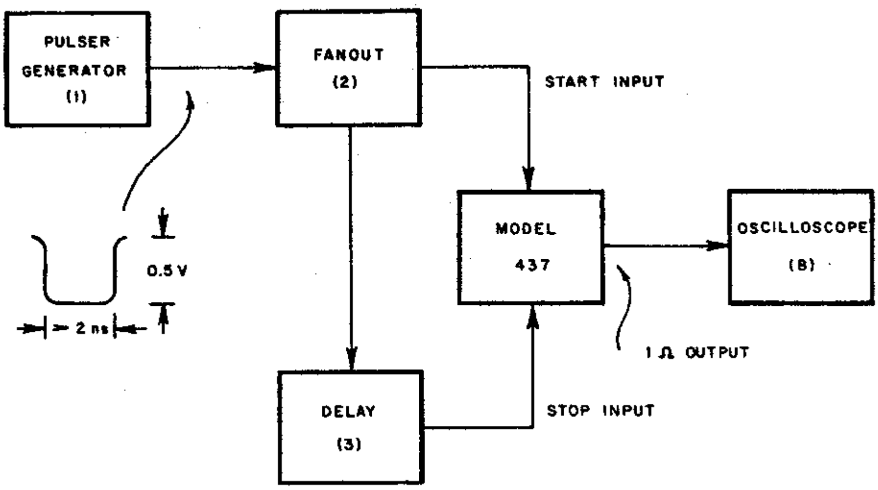


Figure 1. Test System for Checking Conversion

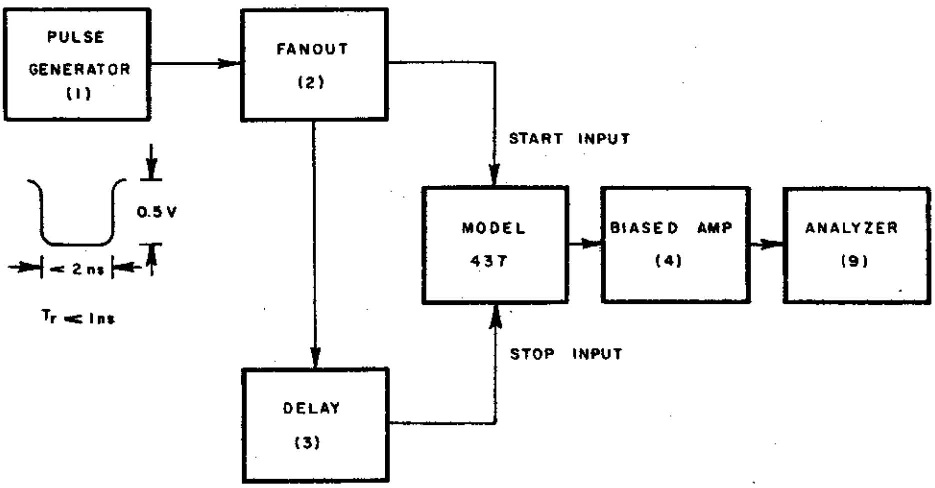


Figure 2. Test System for Checking Converter Resolution

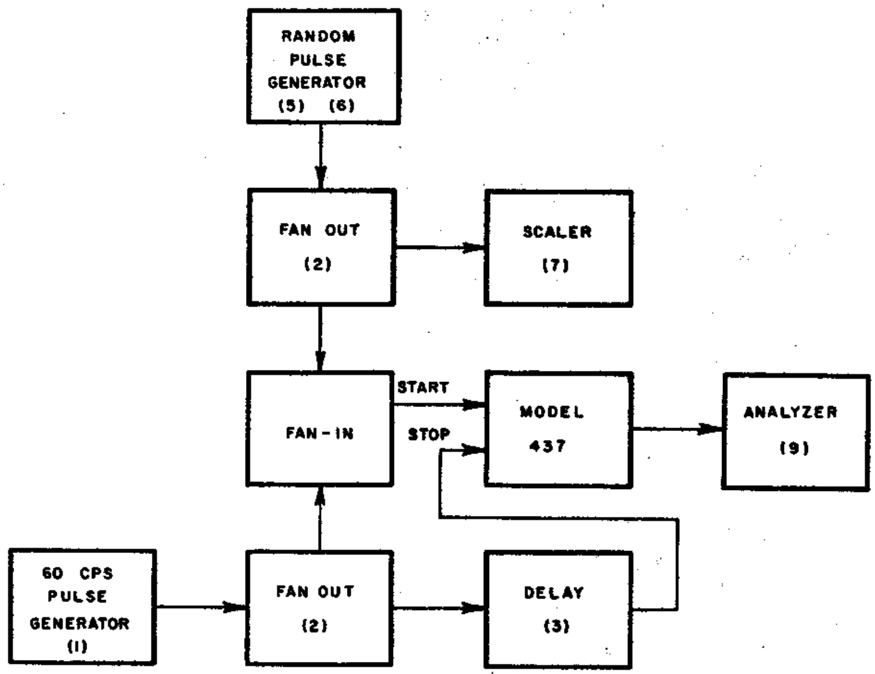


Figure 3. Test System for Checking Count Rate

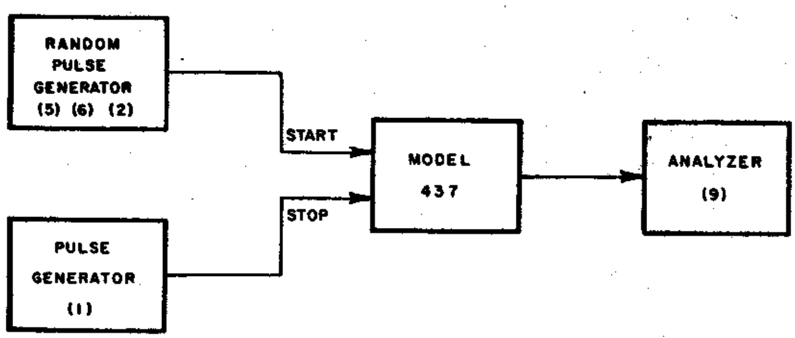
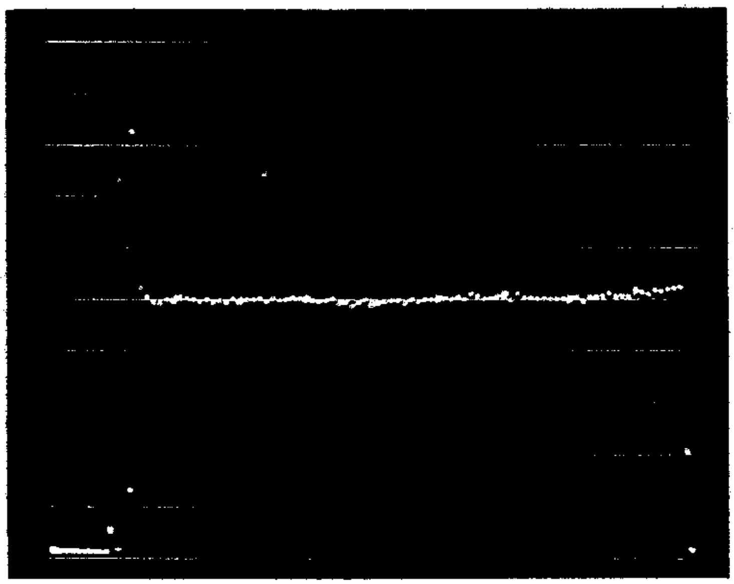
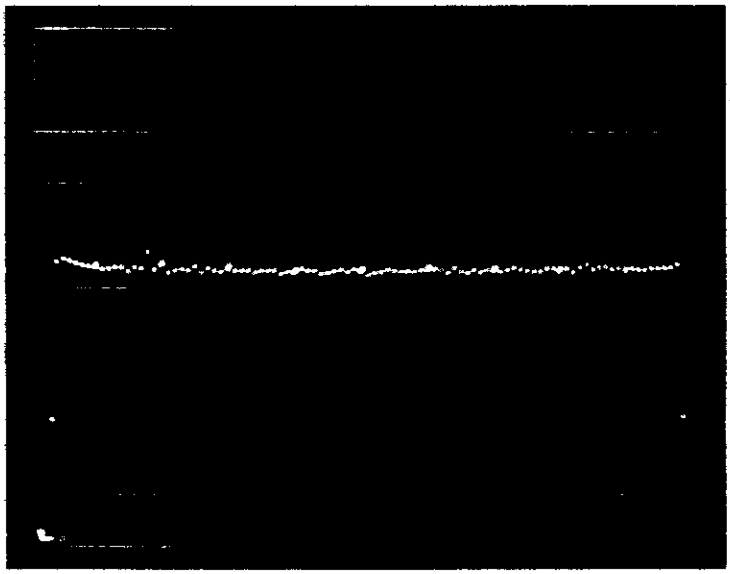


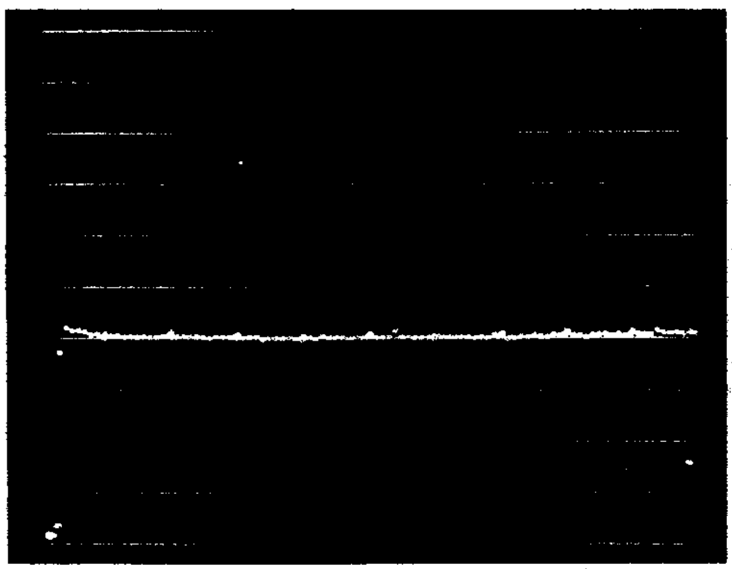
Figure 4. Test System for Checking Differential Linearity



Range = .1 μsec
Multiplier = X1
(Vert): Full Scale = 5 x 10^4 counts
(Horiz): Full Scale = 105% range



Range = .1 μsec
Multiplier = X10
(Vert): Full Scale = 5 x 10^4 counts
(Horiz): Full Scale = 105% range



Range = .1 μsec
Multiplier = X100
(Vert): Full Scale = X10^5 counts
(Horiz): Full Scale = 105% range

Figure 5. Differential Linearity for the Indicated Ranges

the number of counts in each channel of the analyzer would be exactly the same. However, differential nonlinearity does exist and the measure of this is the per cent deviation from the average number of counts per channel. Enough counts must be taken so that this deviation is a measure of the differential nonlinearity and is not caused by the statistical error associated with the number of counts. In this test, the start rate should be quite low; i.e., the analyzer dead time should not be greater than 20%. The stop rate, however, should be rather high to create a high probability for coincidence, i.e., R(stop) >> R(start). This pulse rate should not be allowed to exceed 1 divided by the range time (I/T_R), since otherwise this reduces the range which may be measured.

6.2 Corrective Maintenance

This unit should rarely require more than attention to cleaning to prevent leakage paths from being created by dust collection. If a malfunction is noted, it is important to assure that this is truly within the unit by disconnecting the unit from its position in a system and performing routine diagnostic tests with a pulse generator.

6.2.1 Calibration

The start sensitivity control (R75) and the stop sensitivity control (R98) are merely adjusted to trigger at a level of approximately -250 mV. One must assure, in adjusting R98, that a start signal is present to start a conversion at least 20 nsec prior to the stop signal.

Adjusting of DC and Over-range Zero:

a. Set the Range Selector to 0.8 μsec
b. Monitor TP-1 with a sensitive voltmeter.
c. Adjust R28 until the voltmeter reads ≦±0.002 volt.
d. Monitor TP-2 with the voltmeter.
e. Adjust R31 until the meter reads ≦±0.020 volt.

The adjustment of R28 will affect the reading of TP-2; however, the adjustment of R31 will not affect the voltage at TP-1.

6.2.2 Troubleshooting

Refer to Section 6.1.4 for a simple test to ensure operation of the converter. The typical dc-voltage lists, Table 1, should help to isolate any problem that exists. The voltages given should not be taken as absolute values, but should be taken only as typical values to be used as an aid in troubleshooting.

6.2.3 Factory Repair

The 437, or any ORTEC electronic product, may be returned to the factory for repair service at any time at nominal cost. The standardized procedure requires that each repaired instrument receive the same extensive quality control tests that a new instrument receives.

6.2.4 Tabulated Test Point Voltages on Etched Board

The following voltages are intended to indicate the typical dc voltages measured on the etched board. The voltages given here should not be taken as absolute values, but rather are intended to serve as an aid in troubleshooting.

TABLE 1

TYPICAL DC VOLTAGES

Note: Range = 0.2μsec (X1)
Amp Pot = Min
No signal in

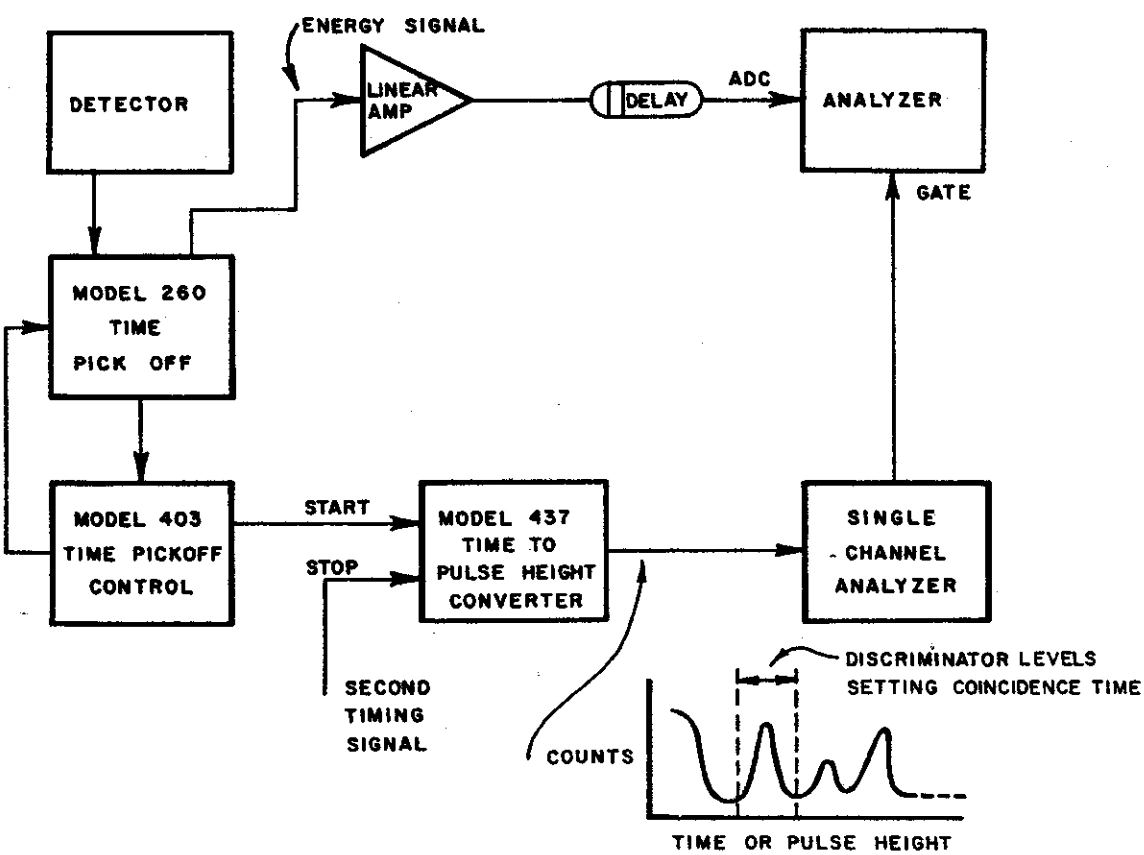
Checkpoint	Typical DC Voltage	Checkpoint	Typical DC Voltage
Q1B	- 0.01	Q23B	+10.36
Q1E	- 0.74	Q23E	+11.0
Q2E	- 0.68	Q24B	+11.61
Q2C	+ 1.07	Q25B	-10.36
Q3B	- 0.06	Q25E	-11.04
Q4B	- 0.20	Q26B	-10.92
Q4E	+ 0.52	Q27B	+ 3.41
Q5B	-12.06	Q27E	+ 2.73
Q6E	-11.69	Q28C	+ 8.14
Q7B	- 2.53	Q29B	- 0.02
Q9B	+ 0.68	Q29E	- 0.76
Q9C	+ 1.42	Q30E	- 0.66
Q9E	0	Q30C	+ 1.07
Q10G	0	Q31B	- 0.63
Q11G	0	Q32B	0
Q12E	+11.66	Q33B	- 0.20
Q12C	+ 5.25	Q34E	-10.88

Checkpoint	Typical DC Voltage	Checkpoint	Typical DC Voltage
Q13B	+ 4.61	Q35B	-10.27
Q14C	- 0.16	D21A	-20.44
Q15B	- 0.70	Q37B	0
Q15E1	0	Q37C	- 5.30
Q16E	+ 0.40	Q39B	- 0.95
Q16B	+ 1.03	Q39C	- 0.13
Q17B	+ 0.06	Q40B	+ 0.74
Q17E	+ 0.66	Q40C	+ 0.10
Q18B	- 9.48	Q41B	-11.40
Q18E	- 8.87	Q41E	-12.01
Q19B	- 0.58	Q42B	-12.68
Q19E	+ 0.06	Q43B	+13.26
Q20B	+ 0.03	Q44C	+15.11
Q21B	+ 1.74	Q44B	+ 1.04
Q 21E	+ 1.04	Q44E	+ 0.42
Q22B (Anticoinc)	+ 0.73	Q45B	- 0.20
Q22B (Coinc)	- 0.51	Q46E	-10.28
		Q46C	0

7. APPLICATION NOTES

7.1 Time to Pulse Height Converter in a Differential Coincidence System

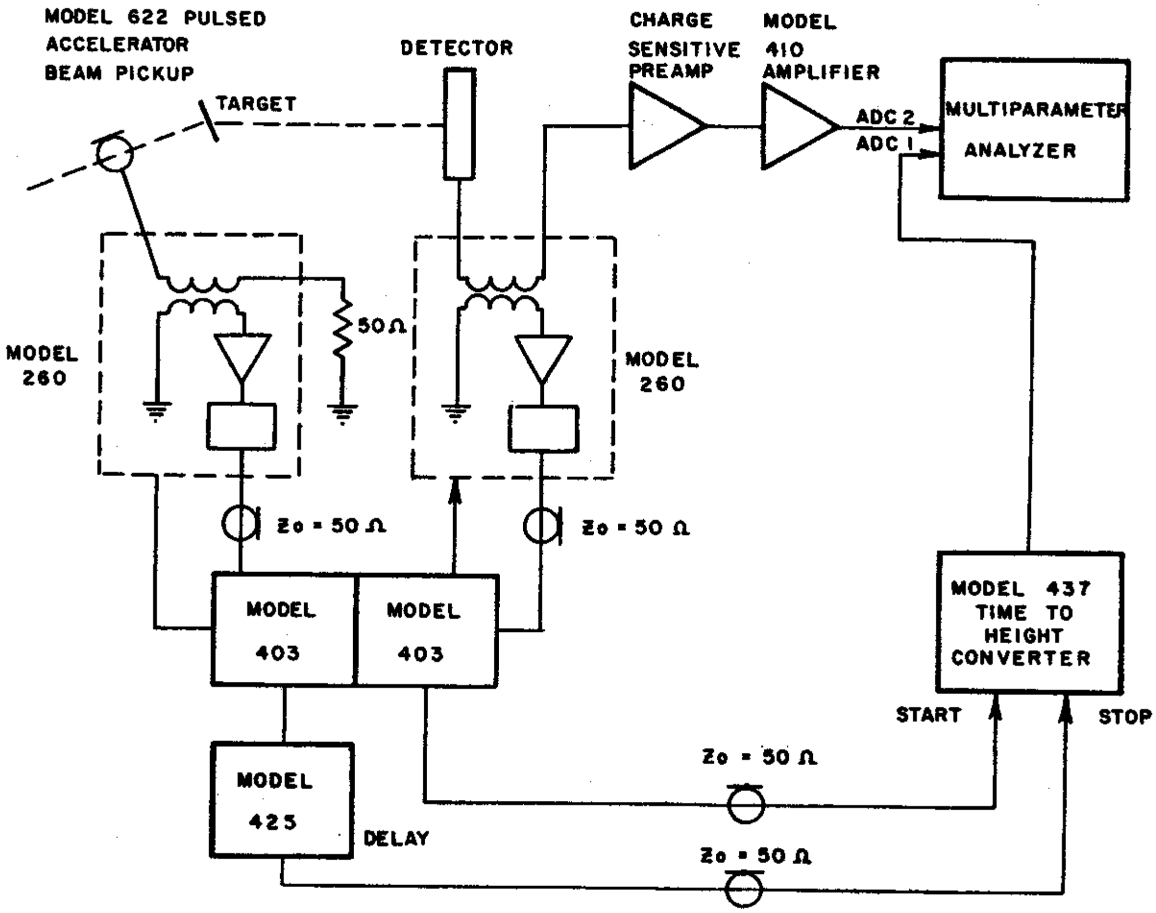
A time to pulse height converter in conjunction with a single-channel analyzer forms a differential coincidence system with variable coincidence time. This coincidence time may be selected by simple variation of the single-channel window position and width. The resolution is limited only by the detector and/or time converter resolution. The advantage is that the fast coincidence is performed by slow linear circuitry. One side of a fast coincidence system of this type is shown in block diagram form below.



Block Diagram of Differential Coincidence System

7.2 Correlated Time-Energy Measurements

Much use of multiparameter analyzers in the recent past has been in connection with correlated time-energy studies.[1,2] The advent of the ORTEC 260 Time Pickoff, in conjunction with the ORTEC 437 Time to Pulse Height Converter and multiparameter analyzers, opens up a new realm of exploration in charged particle spectroscopy by allowing simultaneous high-resolution energy analysis versus subnanosecond time resolution of charged particles. By this method, particle breakup and mass-energy relationships may be studied in detail. A system for identifying charged particles from a pulsed accelerator is shown in the block diagram below.



Block Diagram for Correlated Time-Energy Measurements

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[1] C. W. Williams, W. E. Kiker, and H. W. Schmitt, Rev. Sci. Instr. 35:116 (Sept. 1964)

[2] D. S. Gemmell, IEEE Trans. Nucl. Sci. NS-11(3):409 (June 1964)

7.3 Pulse Shape Discrimination

The extraction of important information contained in a pulse is quite often difficult, but in many cases the additional information is worth the trouble required for its extraction. In the case of pulse shape discrimination, the information may be associated with the sum of multiple pulses, or the sum of differing time components of a single pulse. There are many applications of this principle. Some of these applications are:

A. Scintillation counter pulse shape discrimination

(1) neutron-gamma identification, etc.
(2) photomultiplier noise background reduction

B. Charged particle identification in semiconductors

C. Inspection for pileup reduction

In all of the applications that follow, the basic method of pulse shape discrimination is that of detecting the time variation between the leading edge of the pulse and the crossover point of the pulse. (Double delay line pulse shaping is presumed). The leading edge is identified by a 260 Time Pickoff installed at the detector, and the crossover point is identified by a crossover pickoff circuit following the double line amplifier. These two events actuate the start and stop inputs of the 437 Time to Pulse Height Converter, with the resultant generation of output pulses whose height identifies the shape characteristic of the original detector pulse. Single or multichannel pulse height analysis of the converter output pulses is then utilized to effect the desired analysis of the chosen detector events.

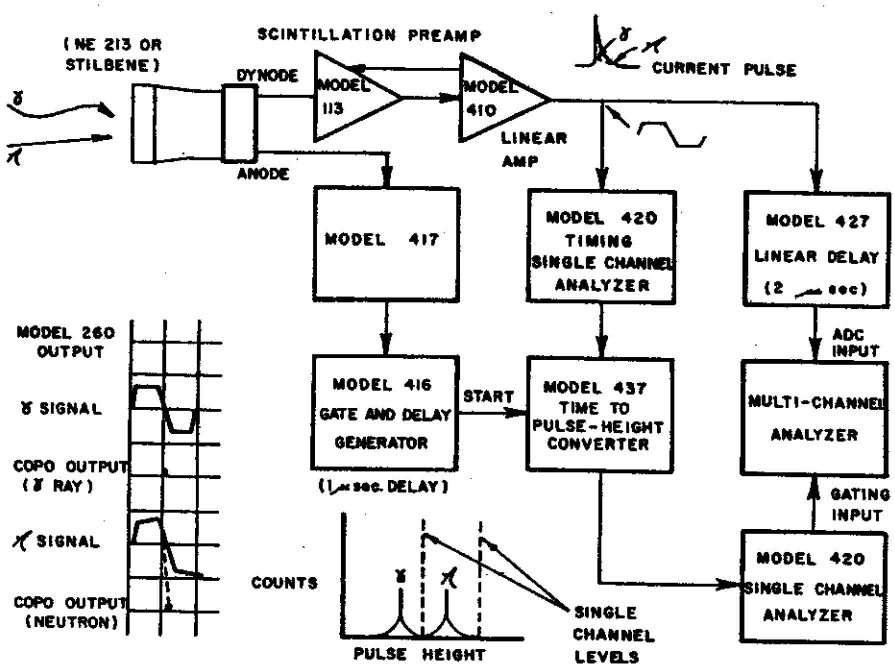
A. Scintillation counter pulse shape discrimination[1,2]

In this type of pulse shape discrimination, the pulse is formed of a component with a short decay time plus a component with a long decay time. In case of the neutron-gamma identification, the energy contained in the long-term decay component from the phosphor is quite different for the same incident energy. When this is integrated and differentiated by two differentiating networks, i.e., double delay line clipping, etc., the crossover point is different for the neutron and the gamma ray.

These same conditions exist in the case of photomultiplier noise and scintillations. The decay of a signal created by photoelectrons which are not a result of scintillation in a phosphor will have only one decay time component, whereas the decay of light from a phosphor adds a second component to all scintillation signals.

A block diagram showing a typical experimental setup for neutron-gamma discrimination is shown below. The same method may be directly applied to PM noise reduction. Some of the advantages of this method are:

(1) high count rate capability ($\geqq 2 \times 10^4$ cps)
(2) wide dynamic range (E_n min >20:1)
(3) low neutron threshold (E_n <300 keV)
(4) simple to set up and monitor
(5) may be performed with a 10-stage photomultiplier



Pulse Shape Discrimination by Crossover Timing

B. Charged particle identification in semiconductors

The method of pulse shape discrimination described above may be applied to the identification of charged particles when used with a semiconductor detector. Essentially, the block diagram is the same as that shown, with only the detector changed. In the identification of particles of the same energy but of differing range (e.g., alphas in the presence of protons), the depletion depth may be adjusted to stop the alphas but not the protons. Proton pulses will then consist of a fast portion, corresponding to collection of signal deposited in the depletion zone, and a slow portion, corresponding to signal collected by diffusion from the field-free undepleted region. The alpha pulses will have only a fast portion associated with them. Identification of the particles can be performed by this means.

C. Inspection for pileup reduction

A different type of pulse shape is of interest here, but the method of identification is again essentially the same. When two pulses are summed in the linear amplifier because they arrive within the resolving time of the amplifier, the crossover time is shifted as before, though not by the same process. This shift of crossover time for a double delay line shaping amplifier will be equal to or greater than

T_r = Rise time
E_1 and E_2 are the two pulses summed.

Here T_r is the amplifier rise time, and E_2 is the amplitude of the pulse that is piled upon E_1 .

The pileup event is distorted, of course, and since its time of zero crossing is shifted, it may be inhibited before analysis. Approximate limits on the use of this method of inspection may be determined from the available resolution of the crossover pickoff used, since an accurate leading edge trigger is now available.

When semiconductor detectors are in use, or when the dynamic range of energies is large (20:1), a more suitable method of pileup rejection may be had by using the 260 Time Pickoff merely to identify the leading edges of all detector events, and then, by means of a suitable circuit, rejecting from analysis all pulse pairs that fall within the resolving time of the amplifier system. Such an inspector system is available as the ORTEC 404 Inspector.

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[1] R. W. Peele and T. A. Love, Instrumentation Techniques in Nuclear Pulse Analysis, National Academy of Sciences — National Research Council Pub. 1184:146 (1964)

[2] D. Landis and F. S. Goulding, Instrumentation Techniques in Nuclear Pulse Analysis, National Academy of Sciences — National Research Council Pub. 1184:143 (1964)

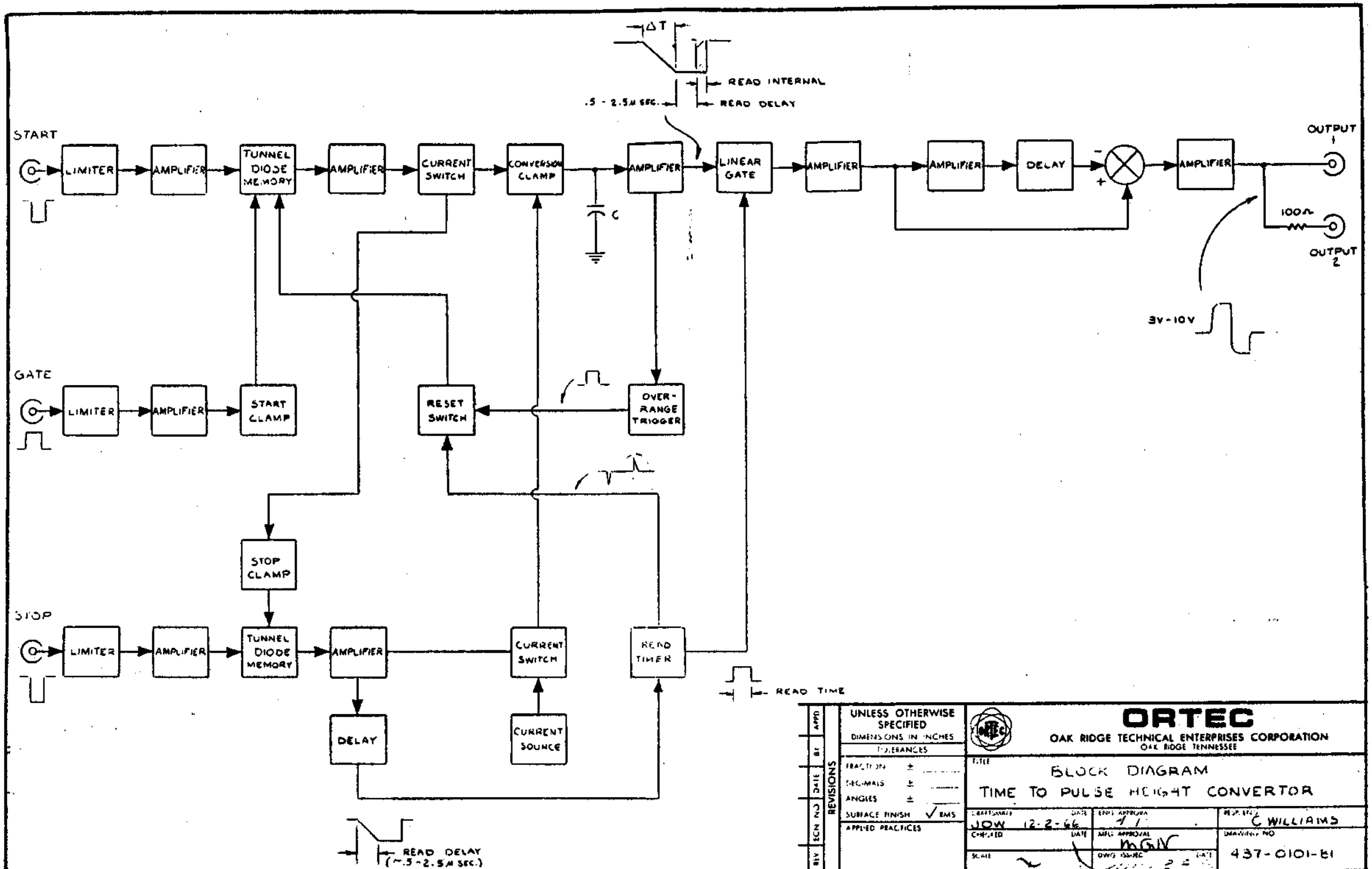
[3] C. W. Williams, H. W. Schmitt, F. J. Walter, and J. H. Neiler, Nucl. Instr. Meth. 29:205-12 (1964)

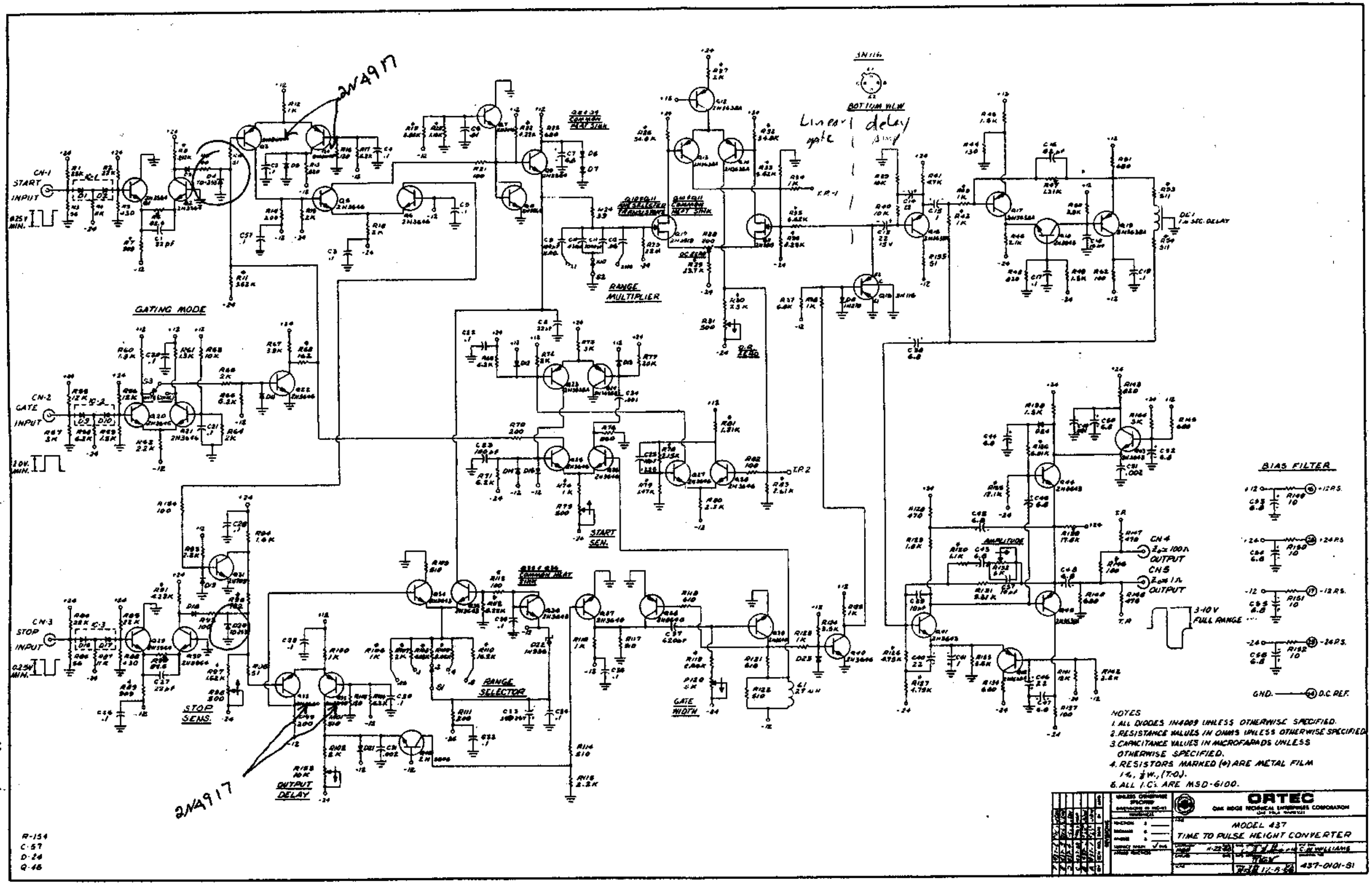
BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893

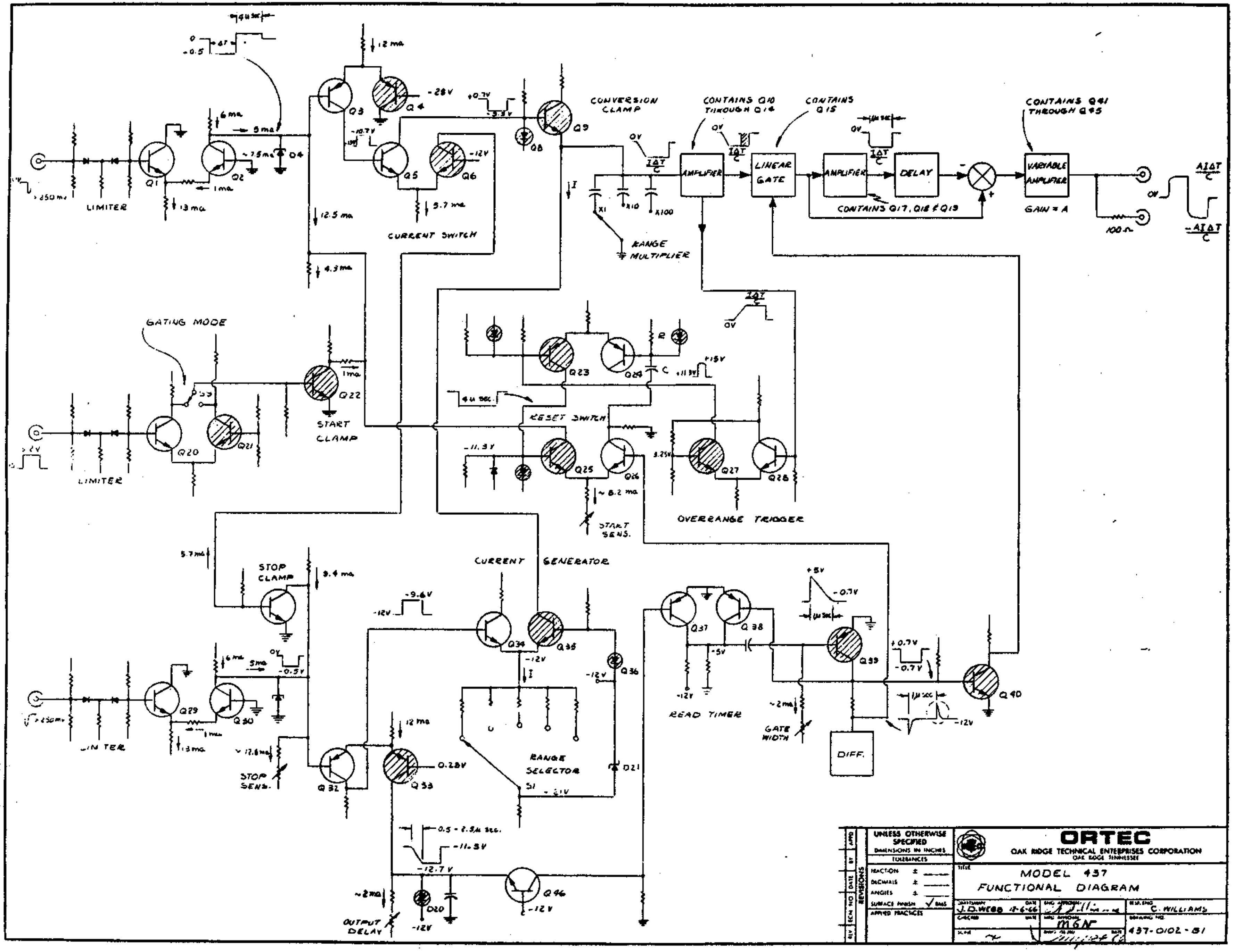
Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	−3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	−24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Carry No. 2
*10	+6 volts	32	Spare
*11	−6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground,
13	Carry No. 1	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	−12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

These pins are installed and wired in parallel in the ORTEC Model 401 Modular System Bin.

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.


START
GATE
STOP
LIMITER
AMPLIFIER
TUNNEL DIODE MEMORY
START CLAMP
STOP CLAMP
CURRENT SWITCH
CONVERSION CLAMP
RESET SWITCH
OVER-RANGE TRIGGER
LINEAR GATE
DELAY
CURRENT SOURCE
READ TIMER
C
ΔT
READ INTERNAL
READ DELAY
.5 - 2.5μ SEC.
READ TIME
READ DELAY (~.5 - 2.5μ SEC.)
3V-10V
100Ω
OUTPUT 1
OUTPUT 2
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTION ±
DECIMALS ±
ANGLES ±
SURFACE FINISH √ RMS
APPLIED PRACTICES
REVISIONS
ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE
BLOCK DIAGRAM
TIME TO PULSE HEIGHT CONVERTOR
JOW 12-2-66
C WILLIAMS
437-0101-B1


CH-1 START INPUT
.25V MIN.
CH-2 GATE INPUT
2.0V MIN.
CH-3 STOP INPUT
0.25V MIN.
GATING MODE
RANGE MULTIPLIER
START SEN.
STOP SENS.
RANGE SELECTOR
OUTPUT DELAY
GATE WIDTH
AMPLITUDE
T.P.1
T.P.2
O.S. ZERO
DL1 1 μ SEC. DELAY
BOTTOM VIEW
CH4 Zo= 100 Ω OUTPUT
CH5 Zo= 1 Ω OUTPUT
3-10V FULL RANGE
BIAS FILTER
+12 R149 10 +12 P.S.
+24 R150 10 +24 P.S.
-12 R151 10 -12 P.S.
-24 R152 10 -24 P.S.
GND. D.C. REF.
NOTES
1. ALL DIODES 1N4009 UNLESS OTHERWISE SPECIFIED.
2. RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.
3. CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4. RESISTORS MARKED (*) ARE METAL FILM 1%, 1/4 W., (T-O).
5. ALL I.C.s ARE MSD-6100.
R-154
C-57
D-24
Q-46
ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
MODEL 437
TIME TO PULSE HEIGHT CONVERTER
C. WILLIAMS
437-0101-S1
2N4917
2N4917
Linear delay gate



UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTION ±
DECIMALS ±
ANGLES ±
SURFACE FINISH √ RMS
APPLIED PRACTICES

REVISIONS

ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE

MODEL 437
FUNCTIONAL DIAGRAM

DRAFTSMAN J.D. WEBB DATE 12-6-66
RES. ENG. C. WILLIAMS
DRAWING NO. 437-0102-B1