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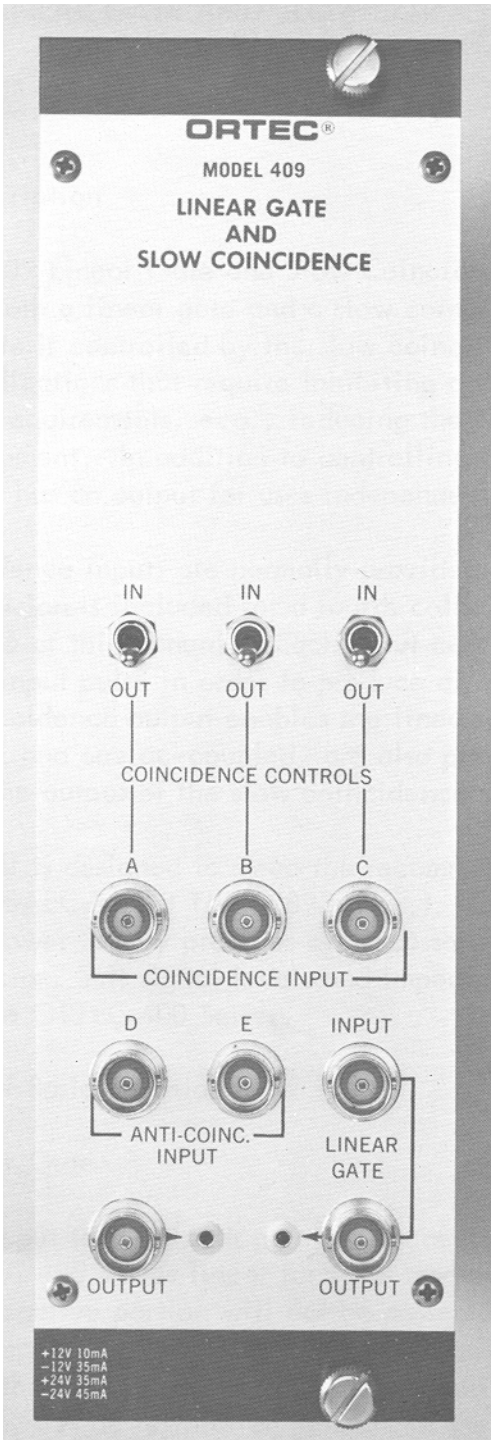
INSTRUCTION MANUAL

409 LINEAR GATE AND SLOW COINCIDENCE

TABLE OF CONTENTS


ORTEC®
MODEL 409
LINEAR GATE
AND
SLOW COINCIDENCE
IN
IN
IN
OUT
OUT
OUT
COINCIDENCE CONTROLS
A
B
C
COINCIDENCE INPUT
D
E
INPUT
ANTI-COINC.
INPUT
LINEAR
GATE
OUTPUT
OUTPUT
+12V 10mA
−12V 35mA
+24V 35mA
−24V 45mA

ORTEC 409
LINEAR GATE AND SLOW COINCIDENCE

1. DESCRIPTION

1.1 General Description

The ORTEC 409 Linear Gate and Slow Coincidence is a dual-purpose module incorporating both a linear gate and a slow coincidence circuit. The operation of the linear gate is controlled by the slow coincidence circuit. The linear gate is useful in applications that require inhibiting a linear signal according to chosen coincidence requirements, e.g., reducing the counting rate in subsequent linear analysis equipment. In addition to controlling the linear gate, the slow coincidence circuit has an output for uses independent of the linear gate.

Three coincidence inputs are normally provided, each with an IN/OUT control switch. Provision is included for a fourth coincidence input if desired. (Refer to Section 6.5 of this manual.) Each input control switch set to IN must have a coincidence input pulse in order to produce an output from the slow coincidence. The slow coincidence output enables the linear gate. Two anticoincidence inputs, one dc- and one ac-coupled, are also provided. An input to either one will inhibit the output of the slow coincidence and the linear gate.

The instrument is designed to meed the recommended interchangeability standards outlined in USAEC Report TID-20893 (Rev.). ORTEC 401A/402A Nuclear Standard Bin and Power Supply provides all necessary power through the rear module power connector. All signal levels and impedances are compatible with other modules in the ORTEC 400 Series.

1.2 Description of Basic Function

1.2.1 Linear Gate

The input to the linear gate will accept all pulse shapes existing in the ORTEC 400 Series linear function modules. If the input signal is bipolar, the negative portion will not be passed through the linear gate. The input impedance is greater than 5000 ohms, ac-coupled as normally sent from the factory, but can be dc coupled if desired. (Refer to Section 4.4.1.) A dc restoration network at the input reduces baseline shift at high counting rates. The restoration network works on both unipolar and bipolar input pulse shapes. The linear gate proper, a series-parallel saturated transistor switch, incorporates an adjustment that allows the

2. SPECIFICATIONS

2.1 General

The 409 is housed in a Nuclear Standard Module; it is two modules wide and weighs 5.3 pounds. It contains no internal power supply and therefore obtains necessary operating power from the Nuclear Standard Bin and Power Supply, ORTEC 401A/402A. All signals in and out of the module are on front panel BNC connectors, and input power is via the standard connector on the rear panel.

2.2 Linear Gate

Input — Unipolar or bipolar, with positive portion leading. Rated range is 0.2V to 10V, 12V maximum
Input Impedance — Greater than 5000 ohms
Gain — Unity
Linearity — Integral nonlinearity less than 0.2% from 0.2V to 8V, 0.3% to 10V
Gate Width — Continuously variable from 0.5 to 3 μsec
Pulse Feedthrough — Less than 10 mV with an 8-volt input pulse
Output Pedestal — Output pedestal adjustable to less than 1 mV
Output — 0.2V to 10V positive rated output range, 12V maximum
Output Impedance — Less than 10 ohms, short-circuit protected
Temperature Stability — Gain shift less than 0.02% per °C
Operating Temperature Range — 0 to 50°C

2.3 Slow Coincidence

Input — Coincidence inputs: Positive 1V minimum, 30V maximum
Anticoincidence inputs: Positive 2V minimum, 15V maximum
Coincidence and anticoincidence input pulses both should be greater than 50 nsec wide.
Input Impedance — 1000 ohms
Resolving Time — The resolving time between two input pulses is equal to the sum of the two input pulse widths. The slow coincidence unit does not regenerate the input signals.
Output — Positive 6V with fwhm adjustable from 0.5 to 3 μsec
Output Impedance — Less than 10 ohms
Power Requirements —

+24V	34 mA
+12V	6 mA
-12V	33 mA
-24V	40 mA

Mechanical — Two modules wide and designed to meet recommended interchangeability standards set out in AEC Report TID-20893 (Rev.); 2.7 inches wide, 8.75 inches high, and 9.75 inches long

3. INSTALLATION

3.1 General Installation Considerations

The 409, used in conjunction with an ORTEC 401A/402A Bin and Power Supply, is intended for rack mounting and therefore it is necessary to ensure that vacuum tube equipment operating in the same rack have sufficient cooling air circulating to prevent any localized heating of the all-transistor circuitry used throughout the 409. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are taken. The 409 should not be subjected to temperatures in excess of 120°C (50°C).

3.2 Connection to Power — Nuclear Standard Bin, ORTEC 401A/402A

The 409 contains no internal power supply and therefore must obtain operating power from the Nuclear Standard Bin and Power Supply (ORTEC 401A/402A). It is recommended that the bin power supply be turned off when inserting or removing modules. The ORTEC 400 Series is designed so that it is not possible to overload the bin power supply with a full complement of modules in the Bin; however, this may not be true when the Bin contains modules other than those of ORTEC design, and in such instances power supply voltages should be checked after the insertion of modules. The 401A/402A has test points on the power supply control panel to monitor the dc voltages.

When using the 409 outside the ORTEC 401A/402A Bin and Power Supply, be sure that the jumper cable used properly accounts for the power supply grounding circuits provided as per the recommended AEC standards of TID-20893 (Rev.). Both high quality and power return ground connections are provided to ensure proper reference voltage feedback into the power supply, and these must be preserved in remote cable installations. Care must also be exercised to avoid ground loops when the module is not physically in the Bin.

3.3 Input Signal Connection to Linear Gate

The input to the linear gate section of the 409 is on the front panel BNC connector; it is directly compatible with the output of all linear amplifiers, biased amplifiers, pulse stretchers, delay amplifiers, and all linear circuitry found in the ORTEC 400 Series. The linear gate passes only positive unipolar signals and/or the positive portion of bipolar signals. This must be kept in mind when putting in linear signals from units other than those of ORTEC design. The input to the 409 linear gate is ac coupled as normally supplied but may be dc-coupled if desired.

If the 409 linear gate is driven from a low impedance source such as the ORTEC 410 output, the input should be terminated in the characteristic impedance of the connecting coaxial cable.

3.4 Logic Inputs to the Slow Coincidence

The input pulses to the slow coincidence may come from any source of logic pulses. The input impedance of the slow coincidence inputs is 1000 ohms, and some care must be given to ensure that reflections do not occur in the driving transmission cable. This probably can best be avoided by terminating the driving cable at the slow coincidence inputs with the characteristic impedance of the driving cable. The amplitude and width of the input signals are specified in Section 2.3.

3.5 Linear Output Signal Connections and Terminating Impedance Considerations

The source impedance of the 0-10 volt standard linear outputs of most 400 Series modules is approximately 1 ohm. Interconnection of linear signals is, thus, non-critical since the input impedance of circuits to be driven is not important in determining the actual signal span, e.g., 0-10 volts, delivered to the following circuit. Paralleling several loads on a single output is therefore permissible while preserving the 0-10 volt signal span. Short lengths of interconnecting coaxial cable (up to approximately 4 feet) need not be terminated. However, if a cable longer than approximately 4 feet is necessary on a linear output, it should be terminated in a resistive load equal to the cable impedance. Since the output impedance is not purely resistive, and is slightly different for each individual module, when a certain given length of coaxial cable is connected and is not terminated in the characteristic impedance of the cable, oscillations will generally be observed. These oscillations can be suppressed for any length of cable by properly terminating the cable either in series at the sending end or in shunt at the receiving end of the line. To properly terminate the cable at the receiving end, it may be necessary to consider the input impedance of the driven circuit, choosing an additional parallel resistor to make the combination produce the desired termination resistance. Series terminating the cable at the sending end may be preferable in some case where receiving end terminating is not desirable or possible. When series terminating at the sending end, full signal span, i.e., amplitude, is obtained at the receiving end only when it is essentially unloaded or loaded with an impedance many times that of the cable. This may be accomplished by inserting a series resistor equal to the characteristic impedance of the cable internally in the module between the actual amplifier output on the etched board and the output connector. It must be remembered that this impedance is in series with the input impedance of the load being driven, and in the case where the driven load is 900 ohms, a decrease in the signal span of approximately 10% will occur for a 93-ohm transmission line. A more serious loss occurs when the

driven load is 93 ohms and the transmission system is 93 ohms. In this case, a 50% loss will occur. BNC connectors with internal terminators are available from a number of connector manufacturers in nominal values of 50, 100 and 1000 ohms. ORTEC stocks in limited quantity both the 50 and 100 ohm BNC terminators. The BNC terminators are quite convenient to use in conjunction with a BNC tee.

4. OPERATING INSTRUCTIONS

4.1 Front Panel Controls

IN/OUT (COINCIDENCE INPUT Control Switches A, B, and C)
These three switches allow the input signals to the coincidence circuit to be disabled without the necessity of actually removing the input coaxial cables. They effectively cause the coincidence circuit to be either one-fold, two-fold, or three-fold, as may be desired, by operating the front panel switches.

4.2 Initial Testing and Observation of Pulse Waveforms

Refer to Sections 6.1 and 6.2 for information on testing performance and observing waveforms.

4.3 Connector Data

PG1 — LINEAR GATE INPUT (BNC)
PG1 is the ac-coupled linear gate input. It has input impedance of greater than 5000 ohms. The rated input voltage range is 0.2 to 10 volts, and maximum input 12 volts. To minimize reflections when driving from low impedance sources into this connector, a terminator equal to the characteristic impedance of the driving cable should be shunted from this connector to ground.

PG2 — COINCIDENCE INPUT A (BNC)
PG2 is the dc-coupled coincidence input. It has input impedance of 1000 ohms, and requires a positive input signal greater than 1 volt.

PG3 — COINCIDENCE INPUT B (BNC)
The characteristics for PG3 are the same as those for PG2.

PG4 — COINCIDENCE INPUT C (BNC)
The characteristics for PG4 are the same as those for PG2.

PG5 — ANTI-COINC. INPUT D (BNC)
PG5 is the dc-coupled anticoincidence input. It has input impedance of 1000 ohms, and requires a positive input signal greater than 2 volts.

PG6 — ANTI-COINC. INPUT E (BNC)
PG6 is the ac-coupled anticoincidence input. It has input impedance of 1000 ohms, and requires a positive input signal greater than 2 volts.

PG7 — OUTPUT (BNC)
PG7 is the dc-coupled coincidence output. It provides a positive 6-volt output signal whose width is continuously adjustable from 0.5 to 3 microseconds. Output impedance is less than 10 ohms.

PG8 — LINEAR GATE OUTPUT (BNC)
PG8 is the ac-coupled Linear Gate output. Output impedance is less than 10 ohms. It provides positive output signals only, with a rated range of 0.2 to 10 volts, and a maximum output of 12 volts.

TP1 — Coincidence Output Test Point
TP1 is the oscilloscope test point for monitoring a signal on the coincidence output BNC connector, PG7. This test point has a 470-ohm series resistor connecting it to PG7.

TP2 — Linear Gate Output Test Point
TP2 is the oscilloscope test point for monitoring a signal on the linear gate output BNC connector, PG8. This test point also has a 470-ohm series resistor connecting it to PG8.
Power Connector
A Nuclear Standard Module Power Connector is provided.

4.4 Typical Operating Considerations

4.4.1 Linear Gate

The Linear Gate is enabled by the output pulse of the slow coincidence section of the 409. Normally, the width of this pulse is continuously variable from 0.5 to 3 microseconds; for other pulse widths refer to Section 6.2 of this manual.

Figure 4.1 illustrates the gating action of the Linear Gate. Notice that only the positive portion of the input signal is passed through the Linear Gate.

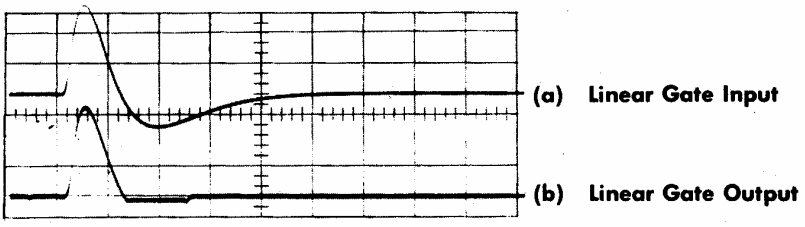


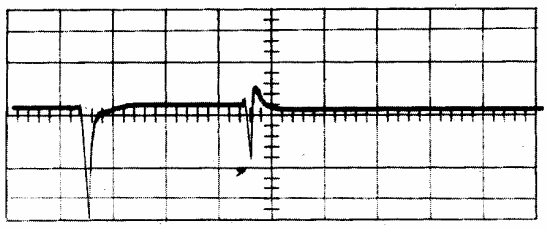
Figure 4.1

The Linear Gate has an internal pedestal adjustment that allows the pedestal to be reduced to a negligible value. (Refer to Section 6.2 for adjustment procedure.) Figure 4.2 shows the output of the Linear Gate with the pedestal a) properly adjusted and b) improperly adjusted. If it is desired to have the input dc coupled, a short jumper wire can be connected from pin 2 to pin 4 on the etched board connector.

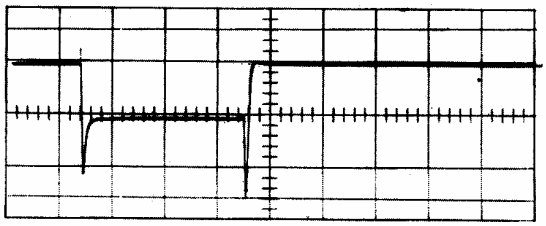
4.4.2 Slow Coincidence

The Slow Coincidence circuit is of the "overlap" type in that there is no regeneration of the input signals within the coincidence recognition circuit. This circuit can also be described as an AND circuit. After coincidence has been recognized, regeneration of the coincidence recognition output occurs, and this regenerated signal constitutes the Linear Gate enable input and the Slow Coincidence output.

Since there is no reshaping of the input pulses, the 2τ resolving time of two input signals is controlled directly by the pulse width of the input signals. Figure 4.3 presents some timing diagrams illustrating input and output waveforms from the 409 coincidence section.



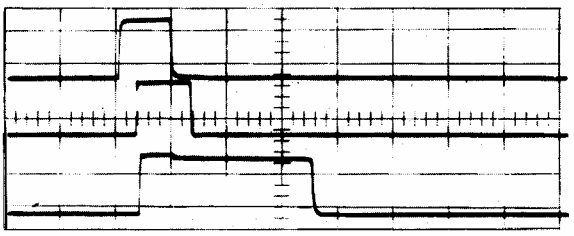
(a) Linear Gate Output showing pedestal properly adjusted.
Scale: 100 mV/cm
500 nsec/cm



(b) Linear Gate Output showing pedestal improperly adjusted.
Scale: 100 mV/cm
500 nsec/cm

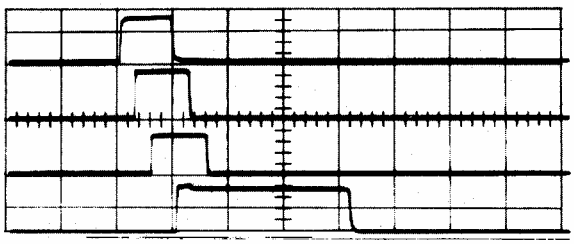
Figure 4.2

If the input pulse that causes coincidence is longer than the pulse width normally generated by the Slow Coincidence circuit, the Slow Coincidence output pulse will be as long as the duration of the input pulse. This is normally not a problem since the inputs to the Slow Coincidence unit have been reshaped by a preceding logic function.



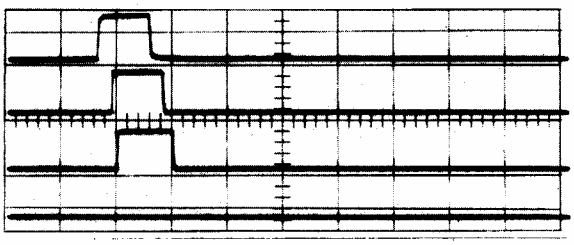
(a) Coincidence Input A
(b) Coincidence Input B
(c) Coincidence Output

I



(a) Anticoincidence Input D
(b) Coincidence Input A
(c) Coincidence Input B
(d) Coincidence Output

II



(a) Coincidence Input A
(b) Anticoincidence Input D
(c) Coincidence Input B
(d) Coincidence Output

III

Figure 4.3

5. CIRCUIT DESCRIPTION, Linear Gate and Slow Coincidence (Etched Board 409-0201)

5.1 Linear Gate

The input to the Linear Gate can be either ac or dc coupled. (See Drawings 409-0201-S1, 409-0201-B1, and 409-0101-S.) The ac-coupled signal is fed in on pin 2 of the etched board and then into the baseline recovery network consisting of diodes D1 through D4 and resistors R1 and R2. The dc restoration network works as follows: With the application of a positive input signal at pin 2, it is coupled through capacitor C1 to the junction of D4 and R2. As the junction of D4-R2 increases in the positive direction, the current through D1 increases due to the current flow out of capacitor C1 through R2. The current flow out of C1 and through R2 is that current necessary to maintain the amplitude of the input voltage at the junction of D4 and R2. With the removal of the input pulse, the quiescent current flow through D1 is available to recharge capacitor C1 back to its steady-state value, since the current through D1 can be reduced to zero and the current through D4 can increase in magnitude to a value of 21. Therefore, the potential at the junction of D4 and R2 will be restored to its steady-state value in a period of time approximately equal to the pulse width of the incoming pulse. The Linear Gate will gate through positive signals or the positive part of bipolar signals. The input signals are coupled through emitter-follower Q1 to the collector of Q2, the series section of a series-shunt Linear Gate. The positive part of the input signal back-biases diode D6, while the negative parts of bipolar signals are blocked by D5. In the steady-state condition Q2 is normally off, since the current switch, Q3 and Q5, is requiring a current through R9 of approximately 4 milliamperes. Q3 of the current switch is normally on, and the current required in the emitter circuit of the current switch is drawn from diode D7 and resistor R8. With the heavy conduction of Q3, the base current for Q2 is zero; therefore, the series resistance of the collector to the emitter of Q2 is very high. Conversely, transistor Q4 has a constant-current base drive through R13 of approximately 1 milliampere, and diode D8 is back biased, causing shunt transistor Q4 to be heavily saturated.

With the application of a positive signal to the collector of Q2, and with the absence of a signal to the current switch, transistors Q3 and Q5, the series-shunt gate is closed for input signals to pin 2 or 4. The Linear Gate is opened by the application of a positive signal to the base of Q5, which causes the current switch to switch its emitter current from Q3 to Q5. When Q5 conducts the emitter current of the current switch, the base drive to Q2 is available via R8, and concurrently, base current for Q4 becomes negligible, since the collector of Q5 requires approximately 4 milliamperes. With the current switch conducting current in Q5, it is seen that Q2, the series element, is in heavy saturation, with the base drive current supplied from R8 flowing into the base through the emitter and back through diode D9 to the emitter follower, Q1. Also, Q4, the shunt element in

the Linear Gate, is now back biased and presents a high shunt impedance to signals flowing through the series element, Q2. With the series-shunt Linear Gate in the open position, i.e., Q2 saturated and Q4 back biased, the output signals of emitter-follower Q1 are presented to emitter-follower Q6 and then to the cascode emitter follower consisting of Q7 and Q8. The output of the cascode emitter follower is taken from the emitter of Q7 to pin 22, the output of the Linear Gate.

Notice that with the Slow Coincidence front panel controls all switched to the OUT position, the current available through the common emitter resistor, R48, will flow through Q15, causing the current switch to conduct current through transistor Q5. With Q5 conducting current in the steady-state condition, the Linear Gate will normally open. With the Linear Gate operating in the normally open mode, the application of an anticoincidence signal to either Q13 or Q14 will result in the closing of the Linear Gate for the duration of the anticoincidence signal, since the current through Q15 will be transferred to Q16 and will enable the current switch, Q3 and Q5, to switch states.

5.2 Slow Coincidence

The Slow Coincidence circuit has provisions for three coincidence input signals and two anticoincidence input signals. The three coincidence signals are dc coupled and come from inputs A, B, and C. The anticoincidence inputs are fed in on inputs D and E, and may be either dc or ac coupled. All inputs are fed in via the front panel BNC connectors. The three coincidence inputs may be switched IN and OUT; i.e., the control of the input pulses may be disabled by operation of the front panel switches.

The Slow Coincidence circuit consists of a three-transistor AND circuit with an inhibit circuit controlling the output of the AND circuit. The output of the AND circuit triggers an output pulse shaper which feeds an output emitter follower. The coincidence AND circuit consists of transistors Q9, Q10, and Q11. These transistors have their common collectors connected in parallel to a coincidence line which feeds into the output shaper, trigger pair Q15, Q16, and Q17. Transistors Q9, Q10, and Q11 operate in the switching mode and are either switched off or are in hard saturation. Operation of the front panel coincidence control switches determines the mode of these transistors. When the control switches are placed to IN, base current is drawn through the 20K-ohm base resistor, saturating the transistor; e.g., Q9 will be saturated due to the base current flowing through R28. If the control switch associated with COINCIDENCE INPUT A is placed to OUT, a 10K-ohm resistor, R25, is connected from the base of Q9 to the +24V supply. This back-biases Q9 and disables coincidence input A. A similar operation occurs for coincidence inputs B and C.

The anticoincidence function, i.e., inhibit, is performed with transistors Q12, Q13, and Q14. The collector of Q12 is connected in parallel with the collectors of input transistors Q9, Q10, and Q11. Transistor Q12 functions as a switch and is normally off, back-biased by approximately 0.3 volts by resistors R41, R44, and R46. Q12 is switched from its OFF state to its ON state by saturation of either Q13 or Q14. Both Q13 and Q14 are normally off and are pulled into saturation with the application of an anticoincidence input pulse to the base of Q13 via R39, or Q14 via R42.

An output pulse from the Slow Coincidence unit is generated when the three coincidence input transistors Q9, Q10, and Q11, and the anticoincidence control transistor, Q12, are turned off, either by application of input pulses or by operation of the coincidence control switches. When these transistors are all turned off, the coincidence line connected to the base of Q15 moves from its steady-state value towards — 1.3V. This negative-going waveshape causes the current through R48 to be switched from Q16, which is normally on, to Q15, resulting in regeneration of the input pulse. Trigger-pair Q15 and Q16 generate a pulse whose width is controlled by C16, R53, and R54. Emitter-follower Q17 provides a low impedance discharge path for capacitor C16, which reduces the trigger pair dead time. Emitter-follower Q18 provides a low impedance output driver for the Slow Coincidence output pulse.