PRECISION

INSTRUMENTATION

FOR RESEARCH

Oak Ridge Technical Enterprises Corporation

OAK RIDGE, TENNESSEE

ORTEC

INSTRUCTION MANUAL

MODEL 408

BIASED AMPLIFIER

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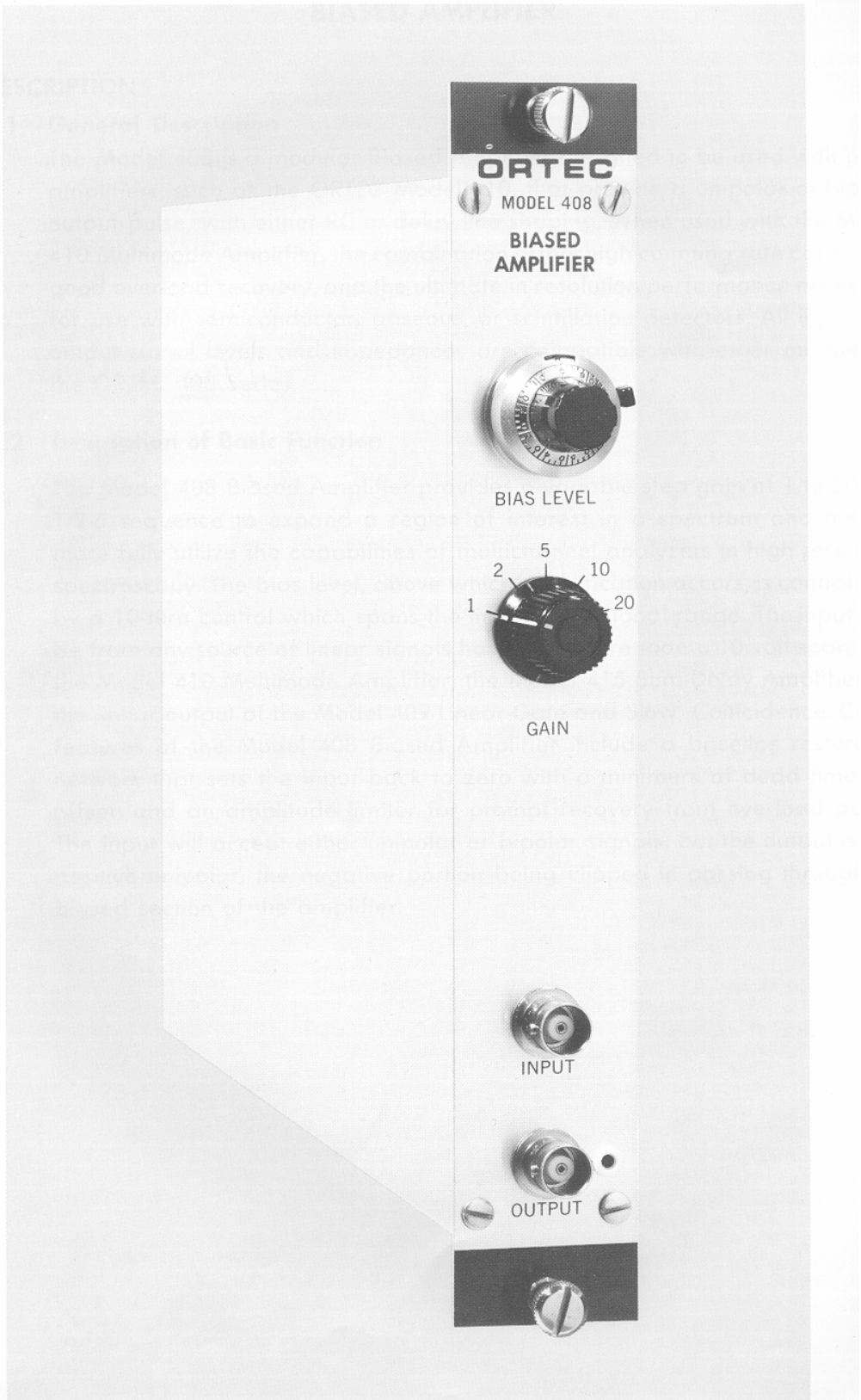

MODEL 408 BIASED AMPLIFIER

2. SPECIFICATIONS

2.1 General Specifications

The Model 408 is housed in a Nuclear Standard Module; it is one standard module wide and weighs 2.4 pounds. The module contains no internal power supply and therefore must obtain the necessary operating power from a Nuclear Standard Bin and Power Supply such as the ORTEC Model 401/402. All signals in and out of the module are on front panel BNC connectors, and the input power is via the standard connector on the rear panel.

2.2 Biased Amplifier Specifications

Input	Unipolar or bipolar (with the positive portion leading); 0.2V to 10V rated range, 12 volts maximum
Input Impedance	125 ohms
Gain	1 to 20 in steps of 1-2-5-10-20
Bias Range	0 to 90% of rated span
Output	0 to 10V rated span, 12V maximum; positive pulse only
Output Impedance	Approximately 1 ohm, short-circuit protected
Linearity	Integral nonlinearity less than 0.2% from 0.2V to 8V, 0.3% to 10V, taken with 1-μsec RC shaped pulse and minimum bias level
Temperature Stability	Gain shift less than 0.01% per °C per gain factor
Operating Temperature Range	0 to 50°C
Power Required	+24V, 59 mA +12V, 3 mA −12V, 13 mA −24V, 53 mA
Mechanical	One module wide and designed to meet the recommended interchangeability standards set out in AEC Report TID-20893; 1.35 inches wide, 8.75 inches high, and 9.75 inches long.

3. INSTALLATION

3.1 General Installation Considerations

The Model 408 Biased Amplifier, used in conjunction with a Model 401/402 Bin and Power Supply, is intended for rack mounting and therefore it is necessary to ensure that vacuum tube equipment operating in the same rack with the Model 408 have sufficient cooling air circulating to prevent any localized heating of the all-transistor circuitry used throughout the Model 408. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are taken; the Model 408 should not be subjected to temperatures in excess of 120°F (50°C).

3.2 Connection to Power—Nuclear Standard Bin, ORTEC Model 402/402

The Model 408 contains no internal power supply and therefore must obtain power from a Nuclear Standard Bin and Power Supply such as the ORTEC Model 401/402. It is recommended that the bin power supply be turned off when inserting or removing modules. The ORTEC 400 Series is designed so that it is not possible to overload the bin power supply with a full complement of modules in the Bin; however, this may not be true when the Bin contains modules other than those of ORTEC design. In such instances, the power supply voltages should be checked after the insertion of modules. The ORTEC Model 401/402 has test points on the power supply control panel to monitor the dc voltages.

When using the Model 408 outside the Model 401/402 Bin and Power Supply, be sure that the jumper cable used properly accounts for the power supply grounding circuits provided in the recommended AEC standards of TID-20893. Both clean and dirty ground connections are provided to ensure proper reference voltage feedback into the power supply, and these must be preserved in remote cable installations. Care must also be exercised to avoid ground loops when the module is not physically in the bin.

3.3 Connection to Linear Amplifier

The input to the Model 408 is on the front panel INPUT BNC connector, and is compatible with all linear unipolar or bipolar signals from the outputs of linear amplifiers, linear gates, delay amplifiers, etc. The input impedance is 125 ohms, ac coupled, and the input operating range is from threshold, typically 100 millivolts, to 10 volts. It is important that no external terminators be added to the INPUT BNC on the Biased Amplifier unless it is determined beforehand that the driving source can drive the combination load of the Model 408 125-ohm input impedance and the external terminator in parallel.

4. OPERATING INSTRUCTIONS

4.1 Front Panel Controls

GAIN

The voltage gain of the Model 408 Biased Amplifier is controlled by the GAIN switch. The gain is applied to the input signal that exceeds the dc BIAS LEVEL. The gain covers the range of 1 to 20 in a 1-2-5-10-20 sequence.

BIAS LEVEL

A continuously adjustable dc bias voltage ranging from 0 to 9V is provided to bias out a fixed level of all input pulses to the Biased Amplifier. The resultant signal, i.e., the portion of the input signal above the bias level, is then amplified by an amount determined by the setting of the Biased Amplifier GAIN switch.

4.2 Initial Testing and Observation of Pulse Waveforms

Refer to Section 6.1 of this Manual for information concerning data obtained during initial testing.

4.3 Connector Data

PG1 — INPUT BNC Connector

Input impedance is 125 ohms, ac coupled. The input voltage rated range is 0 to 10V, with a maximum of 12V. The input may be shunted from its 125-ohm input impedance if necessary to terminate transmission lines that have impedances other than 125 ohms. In shunting the input impedance, care must be taken to ensure that the driving source can drive the resultant low input impedance.

PG2 — OUTPUT BNC Connector

Output driving impedance is approximately 1 ohm and is short-circuit protected.

OUTPUT Test Point

An oscilloscope test point is available for monitoring the signal on the OUTPUT BNC connector. This test point has a 470-ohm series resistor connecting it to to the OUTPUT BNC connector.

Power Connector

The Nuclear Standard Module power connector is an AMP 202515-3.

4.4 Typical Operating Considerations

The output signal of the Model 408 must be closely monitored when using RC shaped input pulses. This is also true if a large amount of integration is used with delay line shaped pulses. The reasoning behind this can be pointed out by examining the resultant pulse shape illustrated in Figure 4-1. With the BIAS LEVEL set at level A, it can be noted that the output pulse width of the Model 408 at the baseline will be from A to A′; i.e., the baseline width is equal to the time the input signal E_{in} is above the BIAS LEVEL. For the BIAS LEVEL A in Figure 4-1, the output pulse of the Model 408 will be satisfactorily shaped to be used as an input to most multichannel analyzers. However, the resultant

Model 408 output pulse for BIAS LEVEL B will have a pulse width at the baseline equal to the time from B to B′ in Figure 4-1. With the Biased Amplifier gain applied to the portion of the input signal E_{in} that is above the BIAS LEVEL B, it is seen that the resultant Model 408 output pulse is much too narrow to be satisfactorily used as an input signal to the majority of available multichannel analyzers. For double RC shaped signals with 0.5-microsecond integration and differentiation time constants, the time between B and B′ can easily be as short as 0.5 microsecond. For the above reasons, an ORTEC Model 411 Pulse Stretcher is recommended for applications involving the Model 408 Biased Amplifier. The Pulse Stretcher will stretch the *peak* amplitude of the output signal from the Model 408 for a minimum of 1.5 microseconds, thereby improving the system linearity by reducing the bandwidth requirements of the multichannel analyzer analog-to-digital converter (ADC).

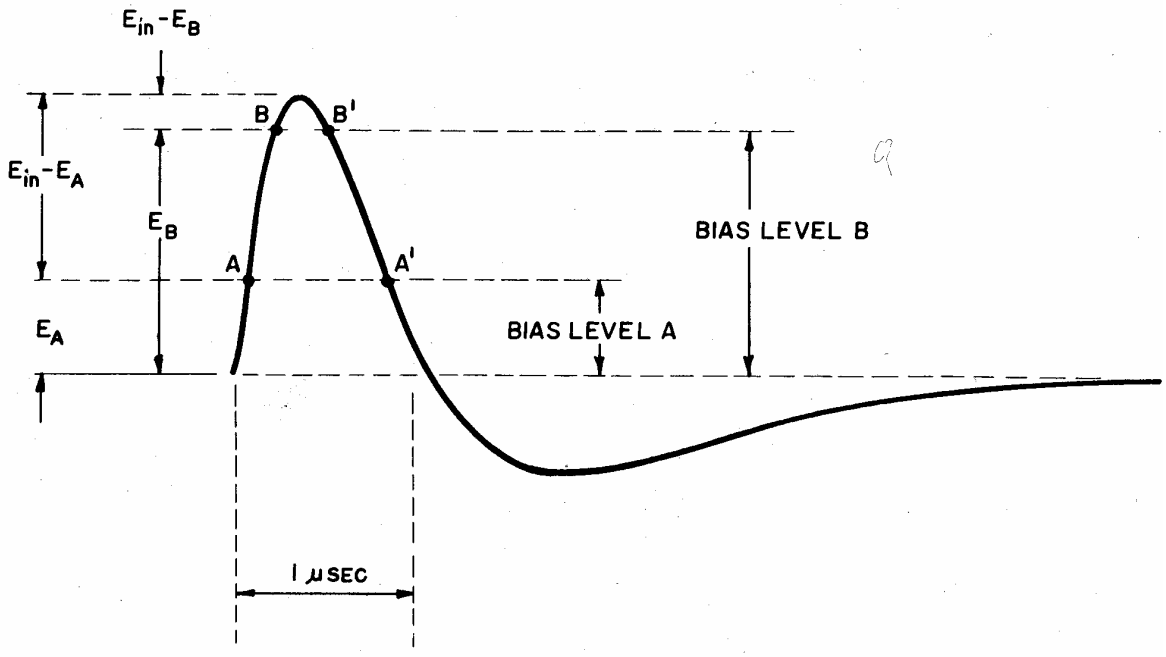

Figure 4-1. Bipolar RC Shaped Input Pulse

5. CIRCUIT DESCRIPTION, BIASED AMPLIFIER (Etched Board 408-0148)

5.1 From Drawings 408-0148-B1 and 408-0148-S1, the following functions can be recognized in the Biased Amplifier: a baseline recovery network consisting of Q1, D2, D3, D4, and Q3 (also called the dc restoration network). Q2 constitutes a dc emitter follower that establishes the bias level at the input to the Biased Amplifier. Q4 is an emitter follower that drives the linear gate section of the Biased Amplifier (Q5 and Q7), and also drives the Schmitt trigger circuit (Q11 and Q12) via the 0.70 limiter (D12, D13, and D14). The linear gate is opened by the application of a positive signal through C4 to the base of Q8, which causes the current switch to transfer its emitter current flowing through R8 from Q6 to Q8. When Q8 conducts the emitter current of the current switch, the base drive current to Q5 is available via R6, and concurrently, base current for Q7 becomes negligible, since the collector of Q8 requires approximately 4 milliamperes. With the current switch conducting current in Q8, it can be seen that Q5, the series element, is in heavy saturation, with the base drive current supplied from R6 flowing into the base through the emitter and back to the emitter of Q4, a low impedance voltage source. Also, Q7, the shunt element in the linear gate, is now back biased and presents a high shunt impedance to signals flowing through the saturated series element, Q5. The output of the linear gate is taken from the collectors of Q5 and Q7. The output of the linear gate is followed by a cascode emitter follower, Q9 and Q10. The output of emitter-follower Q9 and Q10 is fed through a gain control switch and then through two amplifying loops similar to the loops shown in Figure 5-1.

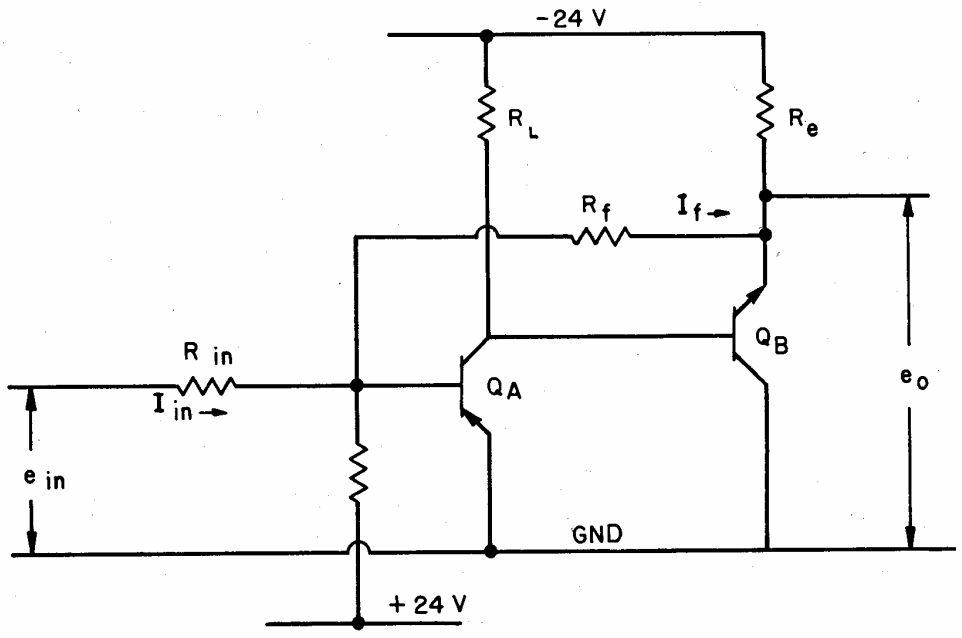

Figure 5-1. Basic Feedback Amplifier Loop

The bias level is set by the 1K helipot; then, the dc bias level is fed through the baseline recovery network in such a way that the bias level is approximately equal to the dc potential on the base of Q4. Diode D6 prevents the emitter potential of emitter-follower Q4 from going more negative than approximately 0.6 volts due to the BIAS LEVEL control.

With the application of a positive input signal, on pin 2 of the Biased Amplifier board, that is equal to or exceeds the bias level dc potential, emitter-follower Q4 will be forward biased and its emitter potential will be equal to the potential of the input pulse minus the dc bias level voltage. The positive pulse generated at the emitter of Q4 is fed in parallel to two circuits—to the emitter of Q5 and to the cathode of D12. The combination of series transistor Q5 and shunt transistor Q7 forms a linear gate. The switching of the linear gate from its normally closed position, i.e., Q5 back-biased and Q7 saturated, to the open position is controlled by the current switch, Q6 and Q8. The current switch is activated by the application of a positive pulse at the base of Q8.

The positive pulse necessary to trigger the current switch is generated at the collector of Q12. Transistors Q11 and Q12 constitute a Schmitt trigger discriminator circuit that is triggered when the pulse amplitude of the input signal on pin 2 exceeds the bias level by 100 millivolts. The appearance of a 100-millivolt positive pulse at the emitter of Q4 is coupled to the trigger circuit, Q11 and Q12, through the diode network, D12 and D13. The positive pulse applied to the cathode of D12 back-biases D12, thereby shunting the ½-milliampere current normally flowing through D12, through diode D13, and then through the parallel combination of D14 and R45. Since R46 constitutes a constant current generator of approximately 1 milliampere, and R45 constitutes a constant current sink of approximately 0.5 milliampere, turning off diode D12 will force the additional ½ milliampere to flow in the combination D13, D14, and R45.

When the additional ½ milliampere is transferred from D12, transistor Q11 will be forward biased, causing the Schmitt trigger circuit, Q11 and Q12, to trigger and remain triggered for the duration of the input pulse that exceeds the bias level by 100 millivolts. Since Q12 is normally conducting, the trigger action will transfer the current from Q12 to Q11, thereby generating a positive pulse at the collector of Q12; this pulse is then coupled to the base of Q8 and activates the current switch, Q6 and Q8.

Transistor Q6 in the current switch is normally conducting, but the application of a positive signal to the base of Q8 causes Q6 to cease conduction and Q8 to conduct heavily. When Q6 ceases conduction, the current flow flowing through R6 is switched from the collector of Q6 into the base of Q5, thereby causing Q5 to go into heavy saturation. In a similar manner, the heavy conduction of transistor Q8 removes the available base current for Q7, causing Q7 to be turned off. With Q5 in heavy saturation and Q7 turned off, the action of the linear gate is evident; i.e., the series path from the emitter of emitter-follower Q4 to the base of transistor Q9 is seen to have a very low impedance. Since transistors Q9 and Q10 form a cascode emitter follower, the signal input at

pin 2 that exceeds the bias level will now appear at the collector of Q10, the output of the cascode emitter follower.

The emitter of Q7 is connected to the wiper of the trimpot, R29, labeled PEDESTAL. The pedestal is normally adjusted for a value of −100 millivolts, i.e., to a negative voltage level that is equal in magnitude and opposite in polarity to the discriminator threshold of the Schmitt trigger circuit, Q11 and Q12. It is important to note that the input signal to the biased amplifier must exceed the bias level (V_B) by approximately 100 millivolts before the linear gate, Q5 and Q7, will be switched open. Since the linear gate is either open (Q5 saturated) or closed (Q5 back-biased), there is negligible nonlinearity for signals just exceeding the bias level. The adjustment of the pedestal trimpot is considered further in Section 6.2.

5.2 The Biased Amplifier GAIN is of the resistor shunt type on the output of the cascode emitter follower, Q9 and Q10. As the amplifier following the cascode emitter follower is of the current type, a shunt resistor to ground from pin 12 will reduce the amount of current flowing into the base of transistor Q13 for a given output voltage from the cascode emitter follower.

The amplifier loop, Q13-Q14, and the output cable driver loop Q15-Q16 Q17, and Q18, are of the basic type shown in Figure 5-1, with the exception of the diode limiter in the loop Q13-Q14. Notice that the diode limiter in the loop is necessary because the output of Q9 and Q10, the cascode emitter follower, can be equal to 10 volts under the conditions of a 10-volt input signal and a bias level of 000.

The output driver loop consists of Q15 through Q18. Q15 and Q17 constitute the typical npn-pnp loop, and they drive quite well in the negative direction but not in the positive direction. The addition of emitter-follower Q16 in this loop allows the overall loop to handle both positive and negative signals quite easily to plus or minus 12 volts into 100 ohms, but an accidental short circuit of the output will cause Q16 to be destroyed. For this reason, Q18 was added to protect Q16. The function of Q18 is to provide a method of limiting the average current through Q16 to a value less than that required to destroy Q16. Q18 can supply large peak currents from the collector-capacitor C24, and these currents can flow directly through Q18 and Q16 and thence into the load. In the event of a short circuit on the output, the absolute magnitude of current that can be supplied through Q18 and Q16 from C24 is less than that required to destroy either Q18 or Q16. Capacitor C24 charges back to the B+ voltage through R47 in the absence of any input pulse.