Model 9633
ADC

9231461A 4/99

User's Manual

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Table of Contents

1. Introduction

The Canberra Model 9633 Analog-to-Digital Converter is a single-width NIM family member of the ICB line of programmable front end electronics and has been designed for use in high resolution and moderate to high count rate applications.

The 9633 boasts differential and integral linearity performance that until now was only possible with Wilkinson ADCs. Its exceptional linearity improves peak shape and resolution, thereby improving the overall performance of the spectroscopy system.

Programmable Gain, Range and Digital Offset allow the user to maximize the use of limited MCA memory by selecting only the specific energy range of interest. This can be particularly useful for multi-input applications such as alpha spectroscopy, thus eliminating the need for older biased amplifiers. These digital controls accomplish the same end more accurately and repeatably.

Conversion for the Pulse Height Analysis (PHA) mode can be programmed for Automatic or Delayed operation. Automatic operation uses an internal constant-fraction peak detector operating on the trailing edge of the input pulse to initiate a conversion. Delayed operation waits up to 100 μs after the leading edge of the input pulse passes the LLD before initiating a conversion. This delay time is ADJustable on the front panel with help from the adjacent Linear Gate signal INSPection test point. Conversions may be enabled/disabled by a Gate input applied at any time during the Linear Gate Interval. Coincidence or Anticoincidence operation is programmable.

Conversion for the Sample Voltage Analysis (SVA) mode is initiated by the falling edge of a Gate pulse applied in the Coincidence mode. The same LLD and ULD limits are used for acceptance of the peak input during the positive gate time.

The 9633 provides the connections required for use with current Canberra amplifiers that perform pileup rejection and live time correction (PUR/LTC). These ADC/amplifier interfaces are also required to use the Westphal Loss Free Counting or Precision Live Time techniques.[1]

The 9633 accepts programming information over an 8-bit wide Canberra bus standard called the Instrument Control Bus (ICB). ICB NIMs connect to this bus via a host module such as the Model 556 Acquisition Interface Module (AIM) as part of a hierarchy of networked acquisition and control managed by a Genie family computing platform.

Adjustments are made via the Graphical User Interface of the Genie software environments. Equivalent batch procedure commands are also available in the environments. All ICB NIM parameters are stored in the single data file structure of the Genie family, allowing verification of correct setup from one experiment to the next.

All ICB NIMs feature a characteristic two-color READY LED to indicate operational status.

The 9633 ADC is fully compatible with Canberra's Model 8233 Digital Stabilizer and Models 8223 and 8224 Analog Multiplexers.

1. G. P. Westphal, Nuclear Instruments and Methods, 163 (1979) 189-196.

2. Controls and Connectors

2.1 Front Panel Controls

This is a brief description of the front panel and connectors. For more detailed information, refer to Appendix A, Specifications.

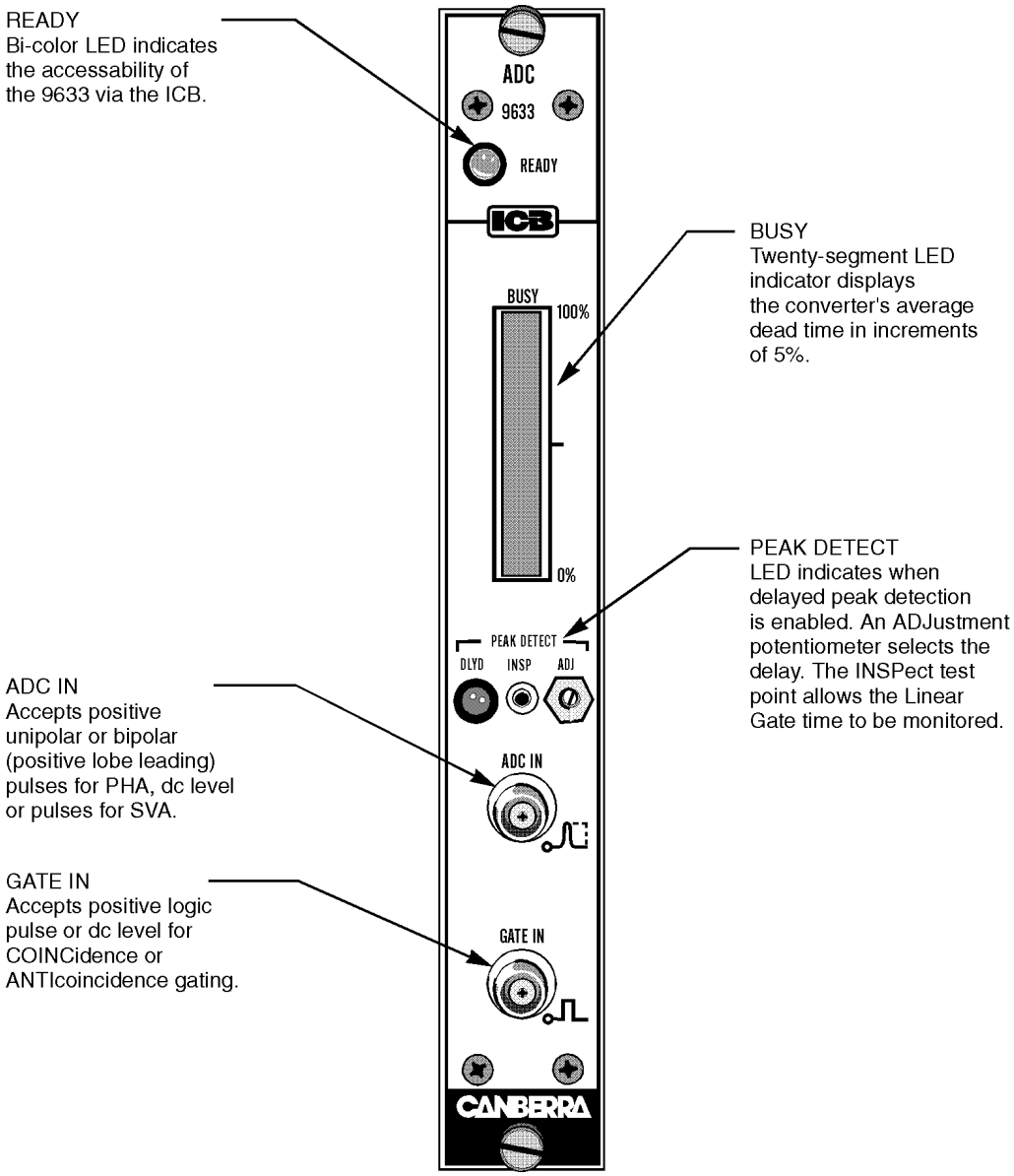

Figure 2.1 Front Panel Controls

2.2 Rear Panel Controls

This is a brief description of the rear panel controls and connectors. For more detailed information, refer to Appendix A, Specifications.

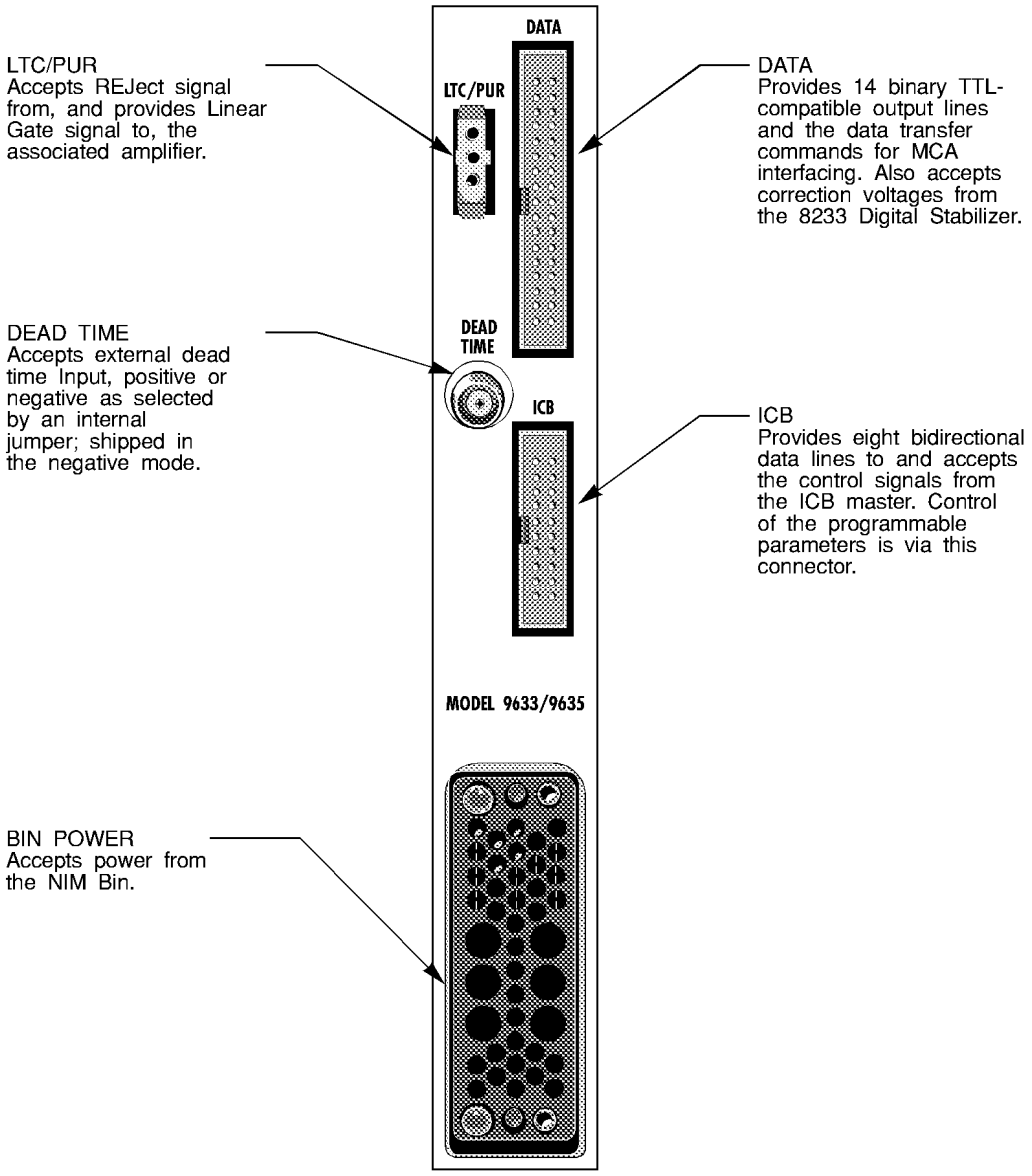

Figure 2.2 Rear Panel Controls

2.3 Internal Controls

This is a brief description of the internal jumpers. For more detailed information, refer to Appendix A, Specifications.

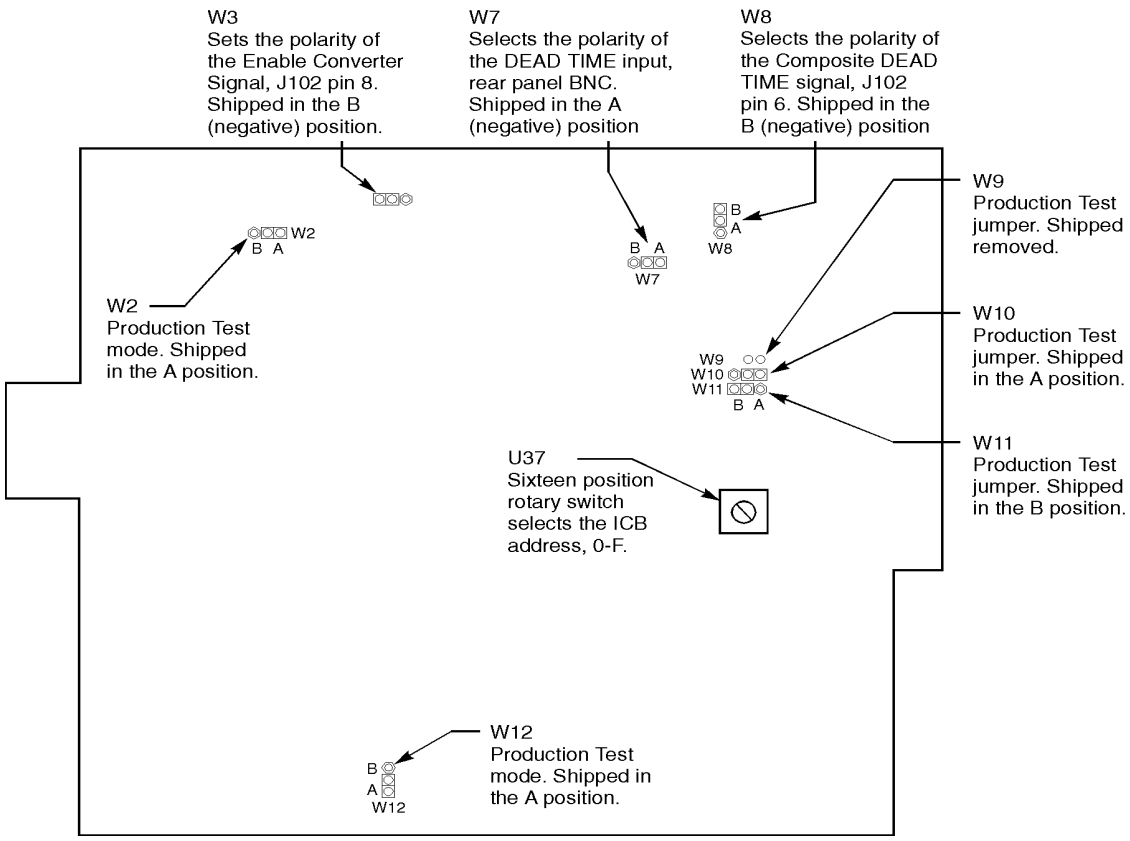

Figure 2.3 Internal Controls

3. Operation

This section discusses the use of the 9633's controls and functions. The controls are programmable unless otherwise noted. For proper operation, an ICB master, such as a Model 556 AIM module, and appropriate software, such as Genie-PC, are required. For details on programming the 9633's controls, please refer to the software manual.

3.1 Busy

The BUSY indicator is 20-segment LED display which shows the average dead time in increments of five percent. Dead time is the time that the ADC is busy converting an input and increases proportionately with increases in conversions per unit time.

3.2 Ready

The READY indicator is a two-color LED which shows the operational status of the unit. An ON-LINE status is indicated by green; a fault or error condition, such as a bus disconnection, is indicated by yellow.

3.3 Gain

The GAIN is a programmable function which controls the ADC's resolution; that is, the number of parts into which the full-scale (10 V) inputs can be divided. The larger the selected gain, the finer the divisions and the greater the resolution.

3.4 Range

The RANGE is a programmable function which is commonly set to equal the size of the MCA memory group assigned to the ADC. For instance a memory assignment of 4096 channels would require a RANGE of 4096.

Inputs which exceed the selected RANGE will not be stored in the MCA's memory. Since the range check is made after the input has been converted, these conversions will add to the ADC's dead time.

3.5 Offset

The OFFSET is a programmable function and is used to precisely shift the memory assignment of the ADC's conversions. With no OFFSET, the ADC's channel numbers are the same as the memory's channel numbers.

For example, if the GAIN is programmed to 8192 and the memory assignment is only 4096, an OFFSET of zero will allow only the lower half of the full-scale conversions to be stored. That is, pulses up to five volts will be stored, pulses greater than five volts will not be stored.

If, in this example, the OFFSET were programmed to 4096, channel 4096 of the ADC would be shifted down to correspond to channel zero of the memory. This offset would allow the upper half of the full-scale conversions, those above five volts, to be stored in the assigned MCA memory.

3.6 LLD and ULD

The Lower Level Discriminator (LLD) and the Upper Level Discriminator (ULD) controls set the limits for the input signals to be accepted by the ADC for conversion. Both of these controls are programmable. If an input pulse falls within the selected window (higher than the LLD setting but lower than the ULD setting) the input will be converted. If the input does not fall within the window, the input will not be converted. The window check is made at the conclusion of the linear gate time. An input pulse oonlide of the window will add to the ADC's dead time, since no pulses may be accepted for processing by the ADC while the linear gate is open.

3.7 Zero

The ZERO control varies the zero intercept of the ADC conversion so that zero energy is stored in the memory's channel zero. The ZERO is a programmable control. A slight adjustment of the control may be necessary for precise energy calibration.

For accurate setting of the ZERO control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. Connect the Pulser's SIGNAL OUT to the ADC Input.
2. Set the Pulser to HI, 0°, +, and 0.5 µs Rise Time.
3. Set the ADC's GAIN control as desired.
4. Set all binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY on, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.
5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be programmed into the ADC. For instance, if the memory is 4096 channels and the GAIN is programmed for 8192, an OFFSET of 4096 must be added so that conversion can take place in the highest channel of the memory.
6. Turn all binary switches on the Model 8210 OFF, except the 1/64 switch, which should be left ON.
7. Program the ADC for an OFFSET of zero.
8. Adjust the ZERO control so that counts are being collected in the proper channel, as follows:

Gain	Channel
16 384	256
8192	128
4096	64
2048	32
1024	16
512	8
256	4

9. Repeat steps 4 through 8 until no further adjustments are necessary.

3.8 Peak Detect

The linear gate, which allows a valid input to be acquired, is normally open. In the AUTO mode, the linear gate closes when the peak amplitude of the input pulse has been detected. Wide input pulses may make the AUTOmatic detection of the peak amplitude uncertain. To overcome this uncertainty, the DELAYED peak detect mode may be used. In the DELAYED mode, the linear gate closes at the end of a selectable time delay. This time delay can be set with the ADJ control while monitoring the INSP test point adjacent to the ADJ control. The adjustment range is from 2 to 100 µs. The selection of AUTO or DELAYED is a programmable function. When DELAYED is selected the Front Panel DLYD (delayed) LED will be illuminated.

The INSP test point provides a positive logic pulse which starts when the input crosses the threshold and ends when the linear gate closes. The threshold voltage follows the LLD setting up to 500 mV maximum. Note that the signal must return below the threshold to allow the ADC to accept a second input. Therefore, the input signal's baseline must be below 500 mV for proper ADC operation.

3.9 Gate

Input pulse conversions may be enabled or disabled by using the GATE function. This function is not the same as the linear gate, which is an internal circuit.

With the ADC programmed for the COINC mode, a positive logic pulse at least 250 ns wide or a positive dc level must be present at the GATE connector during the linear gate time. The linear gate time is defined as the time the input crosses the threshold to the closing of the linear gate and can be monitored at the INSP test point.

If the GATE input is low during the linear gate time, conversion will not take place.

The GATE pulse must be present sometime during the linear gate time to be effective. Since a common gating signal is the output of an independent SCA module, this late-arriving pulse can be accommodated by using the DELAYED peak detect mode and adjusting the linear gate time, as seen at the INSP test point, so that the linear gate closes after the SCA's output arrives. Thus the need for delaying the ADC INput signal can be eliminated.

When the ADC is programmed for the ANTIcoincidence mode, the logic sense of the GATE signal is inverted. That is, a logic low will enable the linear gate and a logic high will disable it.

In any gating mode, an open GATE (nothing connected to the GATE connector) acts as if an enabling level were present.

3.10 Sampled Voltage Analysis

The ADC is usually used in the Pulse Height Analysis (PHA) mode, but by programming the ADC for the SVA mode, analog voltages can be sampled by the ADC. The result will be an amplitude distribution curve of the input signal. The input signal must be between 0 V and 10 V in amplitude to be sampled. If desired, an amplitude window may be set with the LLD and ULD controls.

The GATE input supplies the sampling signal, which must be equal to or greater than 1 µs in width. However, for pulse inputs (rather than dc levels or slowly changing ac signals), the GATE input signal must be narrower than the input pulse width.

In SVA, the GATE input can also be used to trigger the Delay Timer by programming the ADC for Delayed operation. This mode allows the use of Gate Inputs which are narrower than 1 µs. In this configuration, the COINC/ANTI selection is used to select the triggering edge, rising or falling. COINC selects rising and ANTI selects falling. As in the PHA mode, the ADJ control is used to set the delay time.

The sampling rate should be at least twice the frequency of the input signal for accurate sampling.

3.11 Rear Panel Connectors

J107 DEAD TIME – A BNC connector which is used as an external dead time input from Canberra Amplifiers equipped with PUR/LTC. This input is ORed with the ADC Dead Time. Accepts a negative or positive logic signal jumper, selectable via W7; shipped in the A (negative) position.

J102 DATA – Used to connect the ADC to an MCA, an AMX, a Digital Stabilizer, or an LFC module. The proper cable is supplied with the MCA.

J103 ICB - Provides bidirectional data to, and accepts control signals from, the ICB master. Control of the ADC is via this port.

J106 LTC/PUR – Accepts the REJect signal from, and provides the Linear Gate (LG) signal to, Canberra Amplifiers equipped with PUR/LTC.

Further information and signal specifications for these connectors can be found in Appendix A, Specifications.

3.12 ADC Interfacing

This ADC improves its throughput by using a data buffer, or overlap mode, which allows the ADC to accept another analog input and start converting it while the previous conversion is being transferred from the buffer to the memory unit. In the unlikely event that the conversion finishes before the previous data has been transferred from the buffer, the new data is held in the counter and no new conversion can start until the DATA ACCEPTED signal is received. No valid conversion data is discarded by the ADC.

The result of the ADC's conversion is a 14-bit binary-coded number. At the end of the conversion, this number is transferred into the data buffer and signal DATA READY is set true. The address data can now be used by the MCA and the ADC is free to begin another conversion.

The DATA lines are driven by tri-state drivers that are controlled by the ENABLE DATA input. The DATA ACCEPTED input signals the ADC that the current output data has been transferred and the result of the next conversion can be loaded into the buffer.

In a synchronous application, such as Multiparameter Acquisition, it is necessary to operate the ADC in a non-overlap mode, which disables the internal buffer. In this mode, the ADC cannot accept a second input for conversion until the first conversion has been accepted by the MCA.

The overlap/non-overlap mode is a programmable function of the ADC. The ADC is also automatically placed in the non-overlap mode when used in SVA. This is required by the 8223 and 8224 AMX modules.

Invalid inputs are not normally stored by the MCA. In the overlap mode, invalid inputs are converted but are not stored in the buffer and the DATA READY signal is not generated. In the SVA and non-overlap modes, invalid events are converted and the ADC generates the DATA READY and INHIBIT output signals. This causes the MCA to service the ADC; that is, the DATA ACCEPT and ENABLE DATA signals will be generated, but the data will not be stored by the MCA because of the INHIBIT signal. Invalid inputs are defined in "Invalid Flag Conditions" on page 9.

It may sometimes be necessary to record all inputs whether valid or not. This is true for Multiparameter or other synchronous applications. For this case, the ADC must be configured in the non-overlap mode. In this configuration the INHIBIT signal is now considered an INVALID signal, flagging an invalid input but not inhibiting storage. The multiparameter MCA would use this INVALID indication as an input to record these types of events.

The ENABLE CONVERTER input (J102, pin 8) or the front panel GATE input can be used to inhibit a later conversion and thus synchronize multiple ADCs.

The COMPOSITE DEAD TIME output is the sum of the conversion time and the time that the input is above the threshold. The output signal begins when the input signal exceeds the input threshold and ends when the conversion is complete or the input signal goes back below the input threshold, whichever time is longer.

If an external Live Time Corrector (for example, the Model 2024 or 2025 Amplifier) is used, its BUSY signal is summed with the ADC DEAD TIME. The ENABLE CONVERTER signal and gate signal make no contribution to the dead time, although when false, they do inhibit conversion.

3.13 Invalid Flag Conditions

For a conversion to be accepted, it must meet all of the following criteria. When violated, the INVALID flag (J102, pin 12) will be set if the ADC is configured for this mode.

SCA Window

Pulses not in the SCA's analog window will be rejected, initiating a dump cycle. An LLD or a ULD violation will generate the INVALID flag. Both states are interrogated at the peak detection time.

Digital Underflow

Input pulses resulting in a numeric conversion less than the ADC ZERO baseline or less than the digital offset, or both, will be rejected by inhibiting ADC READY. The INVALID flag will be set at the end of LOAD (transfer of data from converter).

Digital Overflow

Input pulses resulting in a numeric conversion greater than the ADC RANGE will be rejected by inhibiting ADC READY. The INVALID flag will be set at the end of LOAD (transfer of data from converter).

Coincidence/Anticoincidence

The GATE pulse width must be at least 250 ns wide and be true (high for coincidence, low for anticoincidence) for at least 100 ns before the peak detection point or the end of Linear Gate. Otherwise the conversion is aborted by initiating a dump cycle. The INVALID flag will be set at the peak detection point.

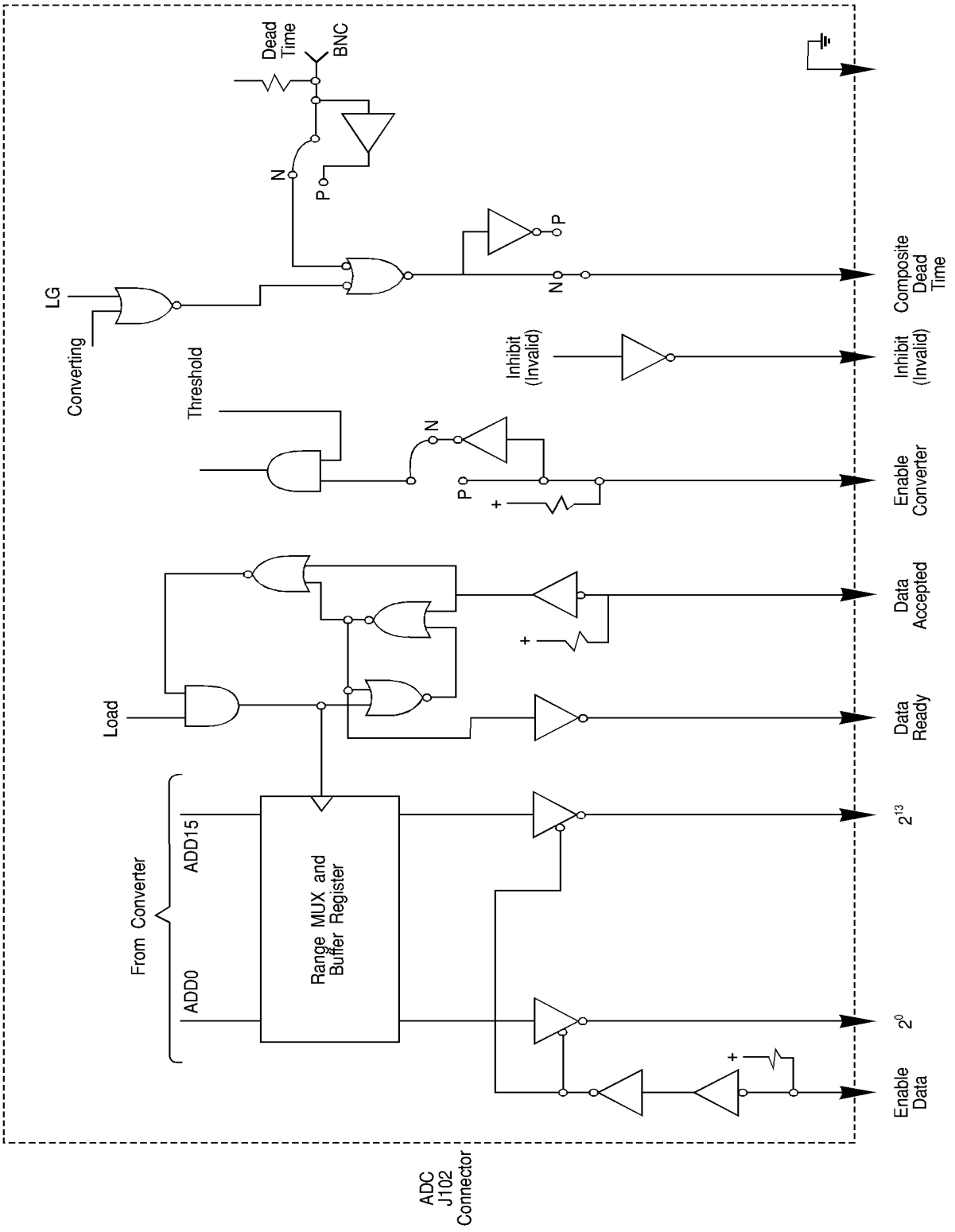

Figure 3.1 Interfacing Logic Block Diagram
(Refer to Schematic B-27205)

4. Theory of Operation

In this chapter, all negative true signals are shown with a trailing asterisk (DUMP*); all other signals are positive true. Each section of the Theory of Operation includes the relevant schematic sheet number after the section title. Two timing diagrams have been included, one for overlap mode and one for non-overlap mode.

4.1 **Peak Detector** (Sheet 1)

The peak detector circuit is designed to track the input signal to its peak amplitude, detect that the peak has been reached, store the peak amplitude and inform the control logic that an input event has been captured. The input is buffered by U53 and presented to the positive input of U54 if the linear gate is open, LGC* high. During the positive transition of the input, U54 supplies current through CR3 pin 3 to charge the storage capacitor, C16. When the peak of the input pulse has been reached, CR3 stops conducting current and charging C16; C16 now holds the peak value of the input pulse.

U41 is a unity gain buffer which provides current isolation between the storage capacitor and the circuit output connections. One of these connections is the peak detector comparator U32. U32 compares the voltage stored on the holding capacitor with the buffered input pulse. When the input pulse is lower in amplitude than the stored voltage the output of U32, PHD*, switches low.

PHD*, Peak Detect, informs the control logic that an input has been captured. The control logic now closes the linear gate by switching LGC* low.

After the converter has digitized the stored voltage, the storage capacitor is rapidly discharged when the control logic sets the DUMP* signal low. The linear gate is reopened immediately following the DUMP* pulse.

4.2 **SCA** (Sheet 1)

The input signal is compared to three separate reference voltages prior to the conversion cycle. These are the LLD, ULD and threshold settings. The threshold tracks the LLD setting up to 500 mV. The output of U53 is compared to the threshold voltage by U45. When an input crosses the threshold, THD* will switch low. The output of the peak detector circuit, VC, is compared to the LLD and ULD setting by U30 and U31 respectively. If the stored voltage is higher than the LLD and lower than the ULD then ULD* will be high and the input will be considered valid for conversion.

4.3 **Sliding Scale** (Sheet 2)

The sliding scale circuit is used to improve the differential non-linearity of the ADC. The sliding scale circuit averages variations in the channel width over 256 channels.

U33 and U48 make up a random number generator. The output of this generator is presented to a DAC, U20. The output of the DAC modifies the amplitude of the signal presented to the converter for processing by subtracting small analog values. In this way, the same input amplitude will produce different results from the converter. This variation is corrected for by adding the random number to the result of the converter. This is done by U22, U35, U42 and U50 on Sheet 3.

4.4 Analog to Digital Converter (Sheet 2)

U19 is the Analog to Digital Converter. It is controlled by inputs TRIG*, LOAD* and Gain Control. The TRIG* signal starts the conversion process. When the conversion is complete, EOC*, (End of Conversion) is set low by U19. The control logic recognizes the EOC*, and, if there are no previous conversions waiting for MCA service, sets the LOAD* signal low to enable the output of U19. The Gain Control input is controlled by the VGAIN input on J102 pin 30 which is generated by the 8233 Digital Stabilizer. The Gain Control input will change the gain of the ADC by ±3% for a ±5 volt input on VGAIN.

4.5 Conversion Gain Control (Sheet 3)

The Conversion Gain setting is a 3-bit code (CCG0-2*) programmed via the ICB and stored in a register in U11, on sheet 5. This 3-bit code is presented to the Conversion Gain Mux PALs U21, U34 and U49. The Conversion Gain Muxes latch the data from the ADC after the random number has been subtracted and perform a shift right of that data. The magnitude of the shift is determined by the Conversion Gain setting. Because the ADC has a fixed conversion time, it is always allowed to convert to its full range regardless of the Conversion Gain setting. By shifting the data right, the MSB from the ADC is aligned with the MSB associated with the Conversion Gain setting. As an example, for 16K Gain, a shift of one bit is performed therefore the input ADD15 would drive the output MX14. 8K Gain would result in a shift of 2 bits, 4K three bits and so on.

The Mux PALs also latch the data from the ADC. This is controlled by the LOAD* signal. The data is latched in order to allow the ADC to convert a second pulse when configured in the Overlap mode.

4.6 Digital Offset

The Digital Offset is subtracted from the Gain corrected data by adders U23 and U36. A twos complement addition is performed which subtracts the Digital Offset value from the output of the Conversion Gain Muxes. The Digital Offset is programmed via the ICB and stored in a register in U11. Based on the Digital Offset setting, the appropriate signal(s), DO128*, DO256*, DO512*, DO1K*, DO2K*, DO4K* and/or DO8K* will be low.

4.7 Range Control

The Range PAL, U9, tests the corrected data from the Conversion Gain Muxes (Q0-Q7) and the Digital Offset adders (Q8-Q15) for an over- or under-range condition. Over-range is defined as the condition where the data exceeds the Range setting programmed into U11 (CCRO-2*). Under-range occurs when the data is less than zero. This can happen when the input fails to exceed the digital offset value, the sliding scale causes a negative value, or the input fails to exceed the Zero Baseline setting. Q15 is used as a sign bit for the data, if this bit is high then the data is negative and considered under-range. Both under- and over-range conditions are indicated by the OFLO* signal being set low.

4.8 Control Logic (Sheet 4)

The Control Logic is made up of three PALs: the Input PAL, U18; the Output PAL, U5; and the State Machine PAL, U10.

The Input PAL collects inputs from the control register in U11, the GATE BNC and the peak detector. It generates two signals for the State Machine: Peak Detected (PHDX*) and GATEX*.

The Output PAL provides the signals required to interface the ADC to an MCA and amplifiers equipped with LTC/PUR.

The State Machine PAL is the heart of the control logic. There are six possible states plus an initialization state which sets all the outputs off. The remaining states are Linear Gate (STL), Peak Detection (STP), Wait (STW), Converter Busy (STC), Dump (STD), and Data Gating (STG). Please refer to the timing diagrams for the sequence of these states. The State Machine PAL generates the signals that control the Peak Detector and Linear Gate (THEN*, DUMP*, LGC*), the ADC Module (TRIG*, LOAD*) and the transfer of data from the ADC module to the output buffers, U15 and U16 on Sheet 3 (LOAD*).

The State Machine is driven by the 10 MHz oscillator, Y1, and controlled by an internally generated signal, Input Condition Met (ICM*). ICM informs the State Machine when the status of the ADC is correct to allow continuation to the next state. For example, when the State Machine is in the Linear Gate State, ICM* will remain false until an input has crossed the threshold (THD* low) for a PHA mode of operation. ICM also triggers the one-shot U2B which generates a delay (DLY*) time period of 0.5 µs.

4.9 **Computer Control Logic** (Sheet 5)

Computer control of the ADC is provided by the Field Programmable Gate Array (FPGA) U11 and the two Dual DACs U12 and U13. U11 provides the interface to the ICB and contains the registers required to hold the configuration of the ADC. U12 is a 12-bit Dual DAC that generates two +5 to –5 volt outputs VZ and CCGAIN. VZ controls the zero setting of the ADC while CCGAIN can be used to control the gain of the ADC. U13 is also a dual 12-bit DAC. U13's outputs VLLD and VULD are programmable from 0 to +5 volts and control the SCA window.

U14 is a nonvolatile RAM which contains the module Type ID and the module's serial number.

U37 is a 16-position binary encoded rotary switch which sets the module's ICB address.

4.10 **Dead Time Display** (Sheet 3 and Schematic B-27427)

U3 and U4 (Board 2) are integrated circuits that sense analog voltage levels and drive the two 10-segment bar graphs U1 and U2 (Board 2), providing a linear analog display of the ADC dead time. The analog voltage is integrated from the ADC dead time signal DISP by R76 and C31. R1 (Board 2) sets the reference voltage for U3 and U4 so that 100% dead time causes all 20 segments to be lit.

4.11 **Power Supplies** (Sheet 6)

VR2 and VR3 are 3-terminal regulators that supply the –15 V and +15 V supplies from the –24 V and +24 V NIM supplies. +5 V for the ADC logic is derived from the +6 V NIM Supply.

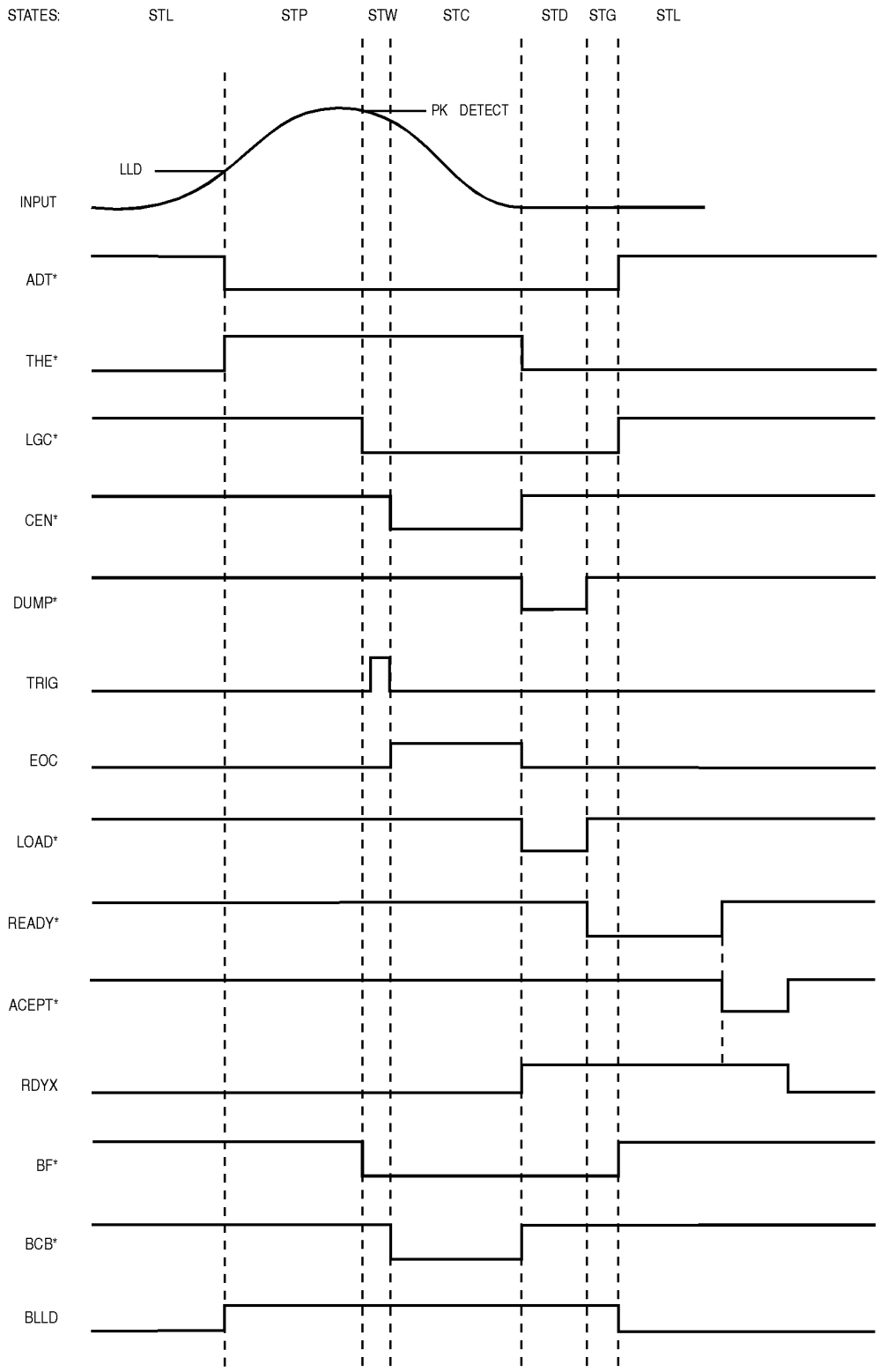

Figure 4.1 9633 Overlap Mode Timing

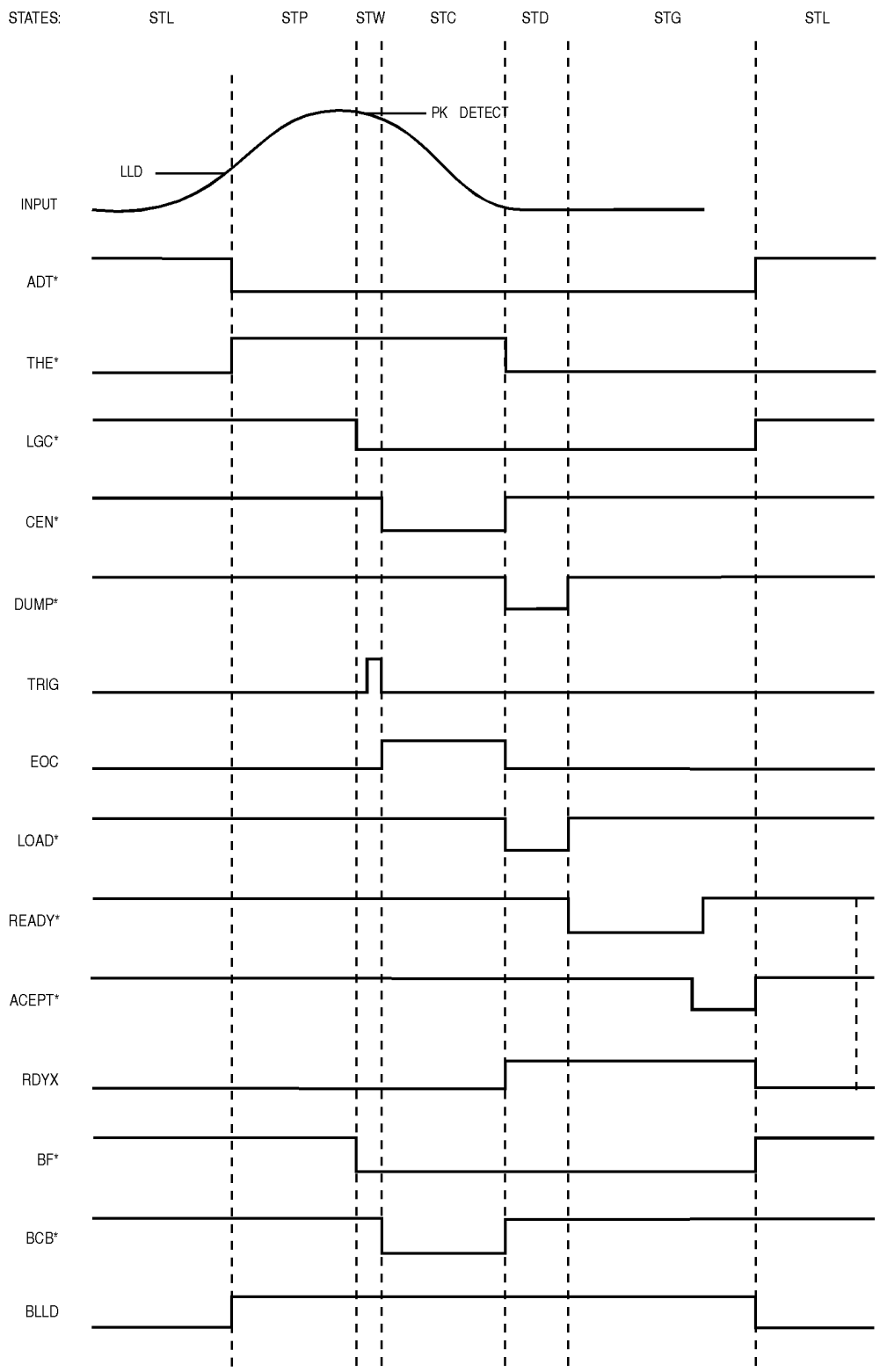

Figure 4.2 9633 Non-Overlap Mode Timing

A. Specifications

A.1 Inputs

ADC IN – Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for the SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 μs maximum; width 0.5 μs minimum; Z_{in} = 1 kΩ, direct coupled; front panel BNC.

GATE IN – Accepts a positive logic pulse or dc level; high amplitude ≥+2.5 V, low amplitude ≤400 mV, 0 to +7 V maximum; dc coupled; loading with Coincidence selected is 1 kΩ to +5 V and 1 kΩ to 0 V for Anticoincidence; width ≥250 ns; PHA analysis does not require a gate input; minimum gate pulse width for SVA is 1 μs.

DEAD TIME – Rear panel BNC connector which receives an external dead time INPUT. Accepts a negative or positive logic signal, jumper selectable, which is ORed with the ADC dead time; negative true amplitude ≤400 mV, positive true amplitude ≥+2.5 V, 0 to +7 V maximum; loading 2.2 kΩ to +5 V. The output composite dead time signal may be accessed through pin 6 of the rear panel DATA connector. Internal jumper plug selects the output composite dead time signal polarity, positive true or negative true; shipped in the NEG position; TTL compatible.

ICB – Provides for connection to the Instrument Control Bus. Computer control of the Model 9633 is through this interface.

A.2 Outputs

DATA – Provides 14 binary TTL-compatible output lines and the data transfer commands required by the MCA interface; rear panel 34-pin ribbon cable connector. Data lines are negative true. Two input lines are also provided for Model 8233 Digital Stabilizer correction voltages. Stabilizer control range: zero = ±3%; gain = ±3%.

LTC/PUR – Accepts Reject and Live Time signals from Canberra amplifiers equipped with PUR/LTC. It also provides Linear Gate to those units for full interactive operation; rear panel 3-pin Molex connector for use with Model C1514 PUR/LTC interface cable.

REJect – Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur during the ADC Linear Gate (LG) signal time; amplitude ≥2.5 V, 0 to 7 V maximum; width ≥100 ns; loading 1 kΩ to +5 V. Accessible through pin 2 of the rear panel LTC/PUR connector.

LG – Provides a negative true logic signal; logic low while the ADC acquires an input pulse, returns to a logic high when the pulse is captured. TTL compatible output, 47 Ω series resistor. Accessible through pin 1 of the rear panel LTC/PUR connector. The LG signal may be viewed at the front panel INSPect test point, positive true, 33 Ω resistor.

ICB – Provides feedback to the computer of the Model 9633's status.

A.3 Manual Controls

ADDRESS – Rotary switch selects 1 of 16 unique ICB Addresses; accessible through opening in the side cover.

A.4 ICB Programmable Controls

GAIN – Full scale resolution of the input signal; 256, 512, 1024, 2048, 4096, 8192, or 16 384 channels for a 10 V input pulse or level.

RANGE – 256, 512, 1024, 2048, 4096, 8192, or 16 384 channels as the ADC's output limit.

OFFSET – Digital offset of 0 to 16 256 channels in binary multiples of 128 channels.

LLD – Lower Level Discriminator for minimum input acceptance voltage; range 0 to +10 V dc; resolution 1 part in 4096 or 2.5 mV/step.

ULD – Upper Level Discriminator for maximum input acceptance voltage; range 0 to +10.5 V dc; resolution 1 part in 4096 or 2.6 mV/step.

ZERO – Analog zero level; adjustment range ±3% of the ADC full scale range; resolution 1 part in 4096 or 0.0015%/step.

PEAK DETECT – Automatic or Delayed. In Automatic an internal constant-fraction trigger operates on the falling edge of the input pulse. In Delayed mode, the conversion begins after a user selectable delay, initiated by the input signal rising through the LLD setting. An ADJustment potentiometer permits selection of a delay from 2 to 100 μs.

GATING MODE – Coincidence or Anticoincidence. In the Coincidence mode (Anticoincidence) a positive GATE pulse enables (disables) the conversion of the present input. If gating is used, the pulse must be present during the Linear Gate time.

PHA/SVA – Pulse Height or Sample Voltage Analysis mode. In PHA, the conversion cycle is initiated by the INPUT pulse. In SVA, the conversion cycle is initiated by a GATE pulse. In either mode, the LLD and ULD acceptance criteria apply. The SVA GATE pulse must be positive in COINC mode or inverted in ANTI mode.

DATA TRANSFER – Overlapped or Non-overlapped. In the Overlapped mode, the ADC is allowed to accept a second input for processing before the current results are transferred to the MCA. Non-overlapped mode requires the MCA to accept the current results before a second input will be processed.

A.5 Front Panel Indicators

READY – Two color LED; green when on-line; yellow for fault or error; off when the module is waiting for the computer to recognize it.

DEAD TIME – 20-segment LED indicator displays the converter's average dead time.

DELAYED – LED indicates that the Delayed Peak Detection mode is enabled.

A.6 Performance

OPERATING TEMPERATURE RANGE – 0 to 40 °C

INTEGRAL NONLINEARITY – <±0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY – <±0.9% over the top 99.5% of range .

GAIN DRIFT – <±0.005% of full scale/°C

ZERO DRIFT – <±0.005% of full scale/°C

LONG TERM DRIFT – <±0.005% of full scale/24 hours at a constant temperature.

PEAK SHIFT – <±0.025 of full scale at rates up to 100 kHz.

ADC DEAD TIME – Linear Gate Time + 5.9 μs.

CHANNEL PROFILE – Typically flat over 90% of channel width.

A.7 ICB Programming Summary

Setup Parameters	Read	Write
Conversion Gain	X	X
Conversion Range	X	X
Digital Offset	X	X
ULD	X	X
LLD	X	X
Zero Level	X	X
PHA/SVA	X	X
Coincidence Mode	X	X
Coincidence Timing	X	X
Peak Detect Mode	X	X
Data Transfer Timing	X	X
Module Status		
ICB Address	X	
Model Number	X	
Factory Serial Number	X	
Hardware Fault	X	
Control		
On-Line (READY LED – Green)	X	X
Off-Line (READY LED – Off)	X	X
Problem (READY LED – Yellow)	X	X

A.8 Power Requirements

+24 V – 135 mA +12 V dc – 0 mA
–24 V – 155 mA –12 V dc – 0 mA
+6 V dc – 650 mA

A.9 Physical

SIZE – Standard single width NIM module 3.42 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-0457T.

NET WEIGHT – 1.04 kg (2.3 lb)

SHIPPING WEIGHT – 2.1 kg (4.6 lb)

A.10 Cables

A 12-port connecting cable is supplied with each Model 556 AIM; if the cable is ordered separately, specify Model C1560 12-port ICB Connecting Cable.

C1703-x, Data Cable.

B. Rear Panel Connectors

This section lists the details of the ADC's rear panel interface and power connectors.

B.1 MCA Interface Connnector

This 34-pin ribbon conector (J102) provides all the necessay signals for connection to the MCA. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	CDT* or CDT
7	GND	8	ENC* or ENC
9	GND	10	READY*
11	GND	12	INB* (INV*)
13	ADC13*	14	ADC00*
15	ADC07*	16	ADC01*
17	ADC08*	18	ADC02*
19	ADC09*	20	ADC03*
21	ADC10*	22	ADC04*
23	ADC11*	24	ADC05*
25	ADC12*	26	ADC06*
27	Reserved	28	Reserved
29	BF*	30	VGAIN
31	BLLD	32	VZERO
33	BCB*	34	ADC13X*

Interface Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

SIGNAL	PIN	DESCRIPTION
ADC00*	14	OUTPUT: Binary data 2^0 (LSB)
ADC01*	16	OUTPUT: Binary data 2^1
ADC02*	18	OUTPUT: Binary data 2^2
ADC03*	20	OUTPUT: Binary data 2^3
ADC04*	22	OUTPUT: Binary data 2^4
ADC05*	24	OUTPUT: Binary data 2^5
ADC06*	26	OUTPUT: Binary data 2^6
ADC07*	15	OUTPUT: Binary data 2^7
ADC08*	17	OUTPUT: Binary data 2^8
ADC09*	19	OUTPUT: Binary data 2^9
ADC10*	21	OUTPUT: Binary data 2^{10}
ADC11*	23	OUTPUT: Binary data 2^{11}
ADC12*	25	OUTPUT: Binary data 2^{12}
ADC13*	13	OUTPUT: Binary data 2^{13} (MSB)
ADC13X*	34	OUTPUT: Binary data 2^{13} (Alternate MSB)
ENDATA*	4	INPUT (Enable Data): Used to enable the tri-state buffers driving the 14-bits of data onto the output lines ADC00* through ADC13*.
READY*	10	OUTPUT (Data Ready): Indicates that data is available for transfer to the MCA. READY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	INPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may reset when READY* resets (handshake).
INB*	12	OUTPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer must be completed, the data itself should be discarded by the MCA.
ENC* or ENC	8	INPUT (Enable Convertor): This signal enables or disables the ADC module. A jumper option (W3) allows selection of polarity. ENC = logic 1 enables ADC operation. ENC = logic 0 prevents the ADC from reopening the linear gate thereby inhibiting further operation.
CDT* or CDT	6	OUTPUT (Composite Dead Time): This signal indicates the time when the ADC or connected amplifier is busy and cannot accept another input event. It is used to gate the live time clock circuit in the MCA. A jumper option (W8) allows selection of polarity.
BF*	29	OUTPUT: This signal is set true at peak detect time and remains true until the leading edge of ACEPT*. This signal is meaningful in the NON-OVERLAP mode only.
BCB*	33	OUTPUT: This signal is set true at peak detect time and remains true until READY* is set true. It represents the conversion time of the internal ADC.

BLLD	31	OUTPUT: This signal is set true when the input pulse rises above the ADC Threshold level and remains true until the trailing edge of ACEPT*.
VZERO (Analog)	32	INPUT: This analog signal controls the ADC zero and it is normally provided by the spectrum stabilizer. The ZERO shift of the ADC is ±3% for a ±5 volt input signal. A more positive level on this signal causes spectral peaks throughout the spectrum to move downward.
VGAIN (Analog)	30	INPUT: This analog signal controls the ADC gain and is normally provided by the spectrum stabilizer. The GAIN shift of the ADC is ±3% for a ±5 volt input signal. A more positive level on this signal causes spectral peaks at the upper end of the spectrum to move downward (lowers the gain).
GND	1,3,5,7,9,11	DC common for all interface signals.

B.2 ICB Interface Connector

This 20-pin ribbon connector (J103) provides all the necessary signals for connection to the Instrument Control Bus (ICB). Negative true signals are shown with a trailing asterisk (LWE*); all other signals are positive true.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	LD0
3	LD1	4	GND
5	LD2	6	LD3
7	GND	8	LD4
9	LD5	10	GND
11	LD6	12	LD7
13	GND	14	LWE*
15	GND	16	LDS*
17	GND	18	LAS*
19	GND	20	LSRQ*

Interface Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatable. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

SIGNAL	PIN	DESCRIPTION
LD0	2	INPUT/OUTPUT: Address/Data line 0 (LSB).
LD1	3	INPUT/OUTPUT: Address/Data line 1.
LD2	5	INPUT/OUTPUT: Address/Data line 2.
LD3	6	INPUT/OUTPUT: Address/Data line 3.
LD4	8	INPUT/OUTPUT: Address/Data line 4.
LD5	9	INPUT/OUTPUT: Address/Data line 5.
LD6	11	INPUT/OUTPUT: Address/Data line 6.
LD7	12	INPUT/OUTPUT: Address/Data line 7. (MSB)
LWE*	14	INPUT (Write Enable): This signal is active when the ICB master is writing to the ICB.
LDS*	16	INPUT (Data Strobe): Used to latch the data into a slave during a write cycle or gate the data onto the bus during a read cycle.
LAS*	18	INPUT (Address Strobe): Used to latch the address which the ICB master is accessing into the slave unit.
LSRQ*	20	OUTPUT (System Request): This signal is set when the slave requires service from the ICB master.
GND	1, 4, 7, 10, 13, 15, 17, 19	DC common for all interface signals.

B.3 PUR/LTC Connector

The PUR/LTC 3-pin Molex connector provides the connection to the spectroscopy amplifier for pulse pileup rejection and accurate live time correction.

SIGNAL	PIN	DESCRIPTION
LG*	1	OUTPUT: This signal is set true when the input pulse rises above the ADC Threshold level and remains true until peak detection. An alternate signal (CB*) which is true during the ADC conversion time is optionally available via a programmable function of the ADC. Used for PUR live time correction in combination with the amplifier. Logic true = 0 to 0.5 volts; logic false = 3 to 5 volts.
REJ	2	INPUT: A positive level on this signal any time during LG* causes the ADC to reject the event in process. Used for PUR in combination with the amplifier. Logic true = 3 to 5 volts; Logic false = 0 to 0.5 volts
GND	3	Signal common.

B.4 DT Connector

The DT (deadtime) BNC connector accepts a negative or positive true amplifier busy signal, with polarity selectable via jumper W7. This signal is logically ORed with the ADC busy signal to provide proper live time correction in the MCA via signal CDT* on the MCA interface connector.

C. Setup Diagrams

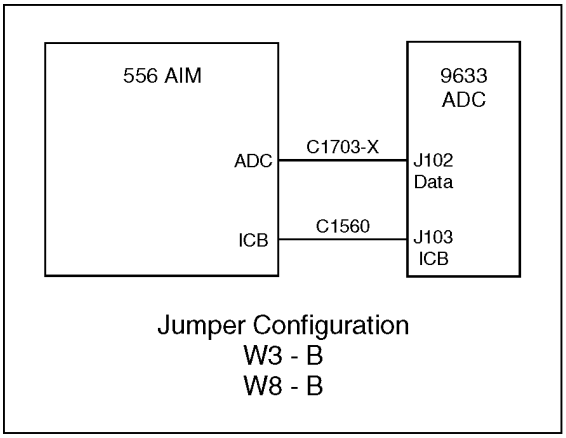

Figure 1

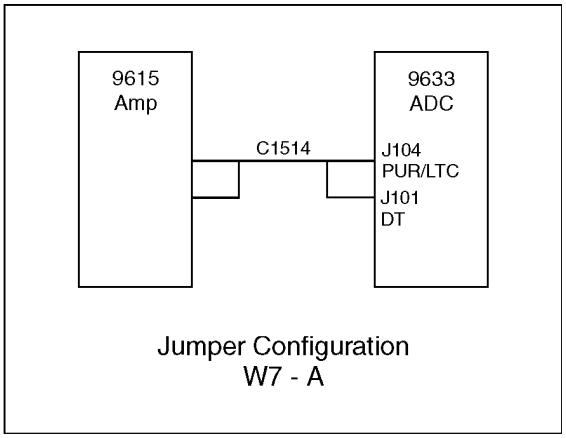

Figure 2

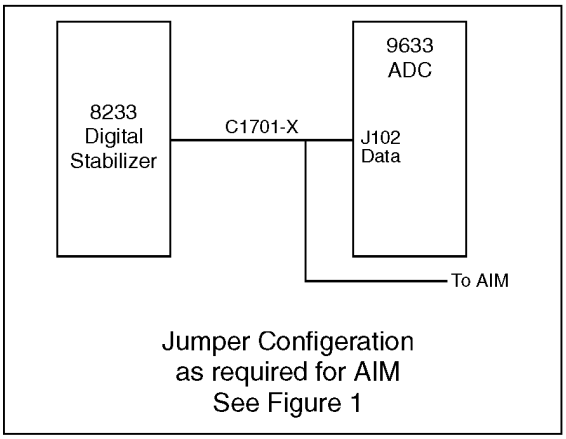

Figure 3

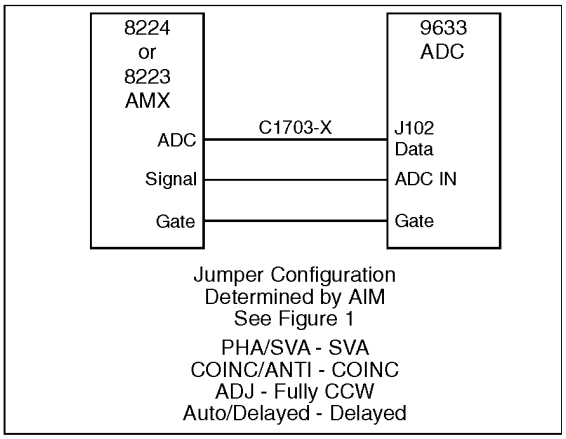

Figure 4

D. Environmental Specifications

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- a rack or tabletop enclosure fully closed on all sides with rear door access
- single point external cable access
- blank panels to cover open front panel Bin area
- compliant grounding and safety precautions for any internal power distribution
- the use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance to the specified EU requirements.

Operating Temperature: 0-50 degrees Centigrade
Operating Humidity: 0-80% Relative, Non-condensing
Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution degree 2

Preventative Maintenance

This unit does not require preventative maintenance.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap side or rear panels.

Warranty

Canberra's product warranty covers hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Canberra (we, us, our) warrants to the customer (you, your) that equipment manufactured by us shall be free from defects in materials and workmanship under normal use for a period of one (1) year from the date of shipment.

We warrant proper operation of our software only when used with software and hardware supplied by us and warrant that our software media shall be free from defects for a period of 90 days from the date of shipment.

If defects are discovered within 90 days of receipt of an order, we will pay for shipping costs incurred in connection with the return of the equipment. If defects are discovered after the first 90 days, all shipping, insurance and other costs shall be borne by you.

LIMITATIONS

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE.

EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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