Model 8701
ADC

User's Manual

8701-USR
4/97

ISO 9001
SYSTEM
CERTIFIED

CE

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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

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1. Introduction

The Model 8701 is a 100 MHz Wilkinson analog-to-digital converter designed to provide a full 8192 channels of resolution in a wide range of applications. Its exceptional linearity improves peak shape and resolution, thereby improving the overall performance of spectroscopy system.

Concentric Gain and Range controls together with digital Offset allow the user to maximize the use of limited MCA memory by selecting only a specific energy range of interest. This can be particularly useful for multi-input applications such as alpha spectroscopy, thus eliminating the need for older biased amplifiers. These digital controls accomplish the same end more accurately and repeatably.

Conversion for the Pulse Height Analysis (PHA) mode can be initiated Automatically using an internal constant-fraction peak detector operating on the trailing edge of the input pulse, or can be Delayed up to 100 μs after the leading edge of the input pulse passes the LLD. A front panel Inspect test point is provided so that the user can monitor the Linear Gate (LG) time between LLD crossing and the beginning of conversion for either mode. Conversions may be enabled/disabled by Coincidence/Anticoincidence gating applied at any time during the Linear Gate Interval.

Conversion for the Sample Voltage Analysis mode is initiated by the falling edge of a Gate pulse applied in the Coincidence mode. The same LLD and ULD limits are used for acceptance of the peak input during the positive gate time.

The 8701, provides front panel, screwdriver adjustable, multi-turn, potentiometers for the control of the Lower and Upper Level Discriminators, as well as the ADC Zero. The 8701 provides the connections required for use with current Canberra amplifiers that perform pileup rejection and live time correction (PUR/LTC). These ADC/amplifier interfaces are also required to use the Westphal loss free counting or precision live time techniques.[1]

The 8701 ADC is fully compatible with all current Canberra MCAs (with external ADC interface options), Digital Stabilizer and Analog Multiplexers.

Appendix C includes several block diagrams to help you set up your system.

1. G. P. Westphal, Nuclear Instruments and Methods 163 (1979) 189-196.

2. Controls and Connectors

2.1. Front Panel

This is a brief description of the 8701's front panel controls and connectors. For more detailed information, refer to Appendix A, Specifications.

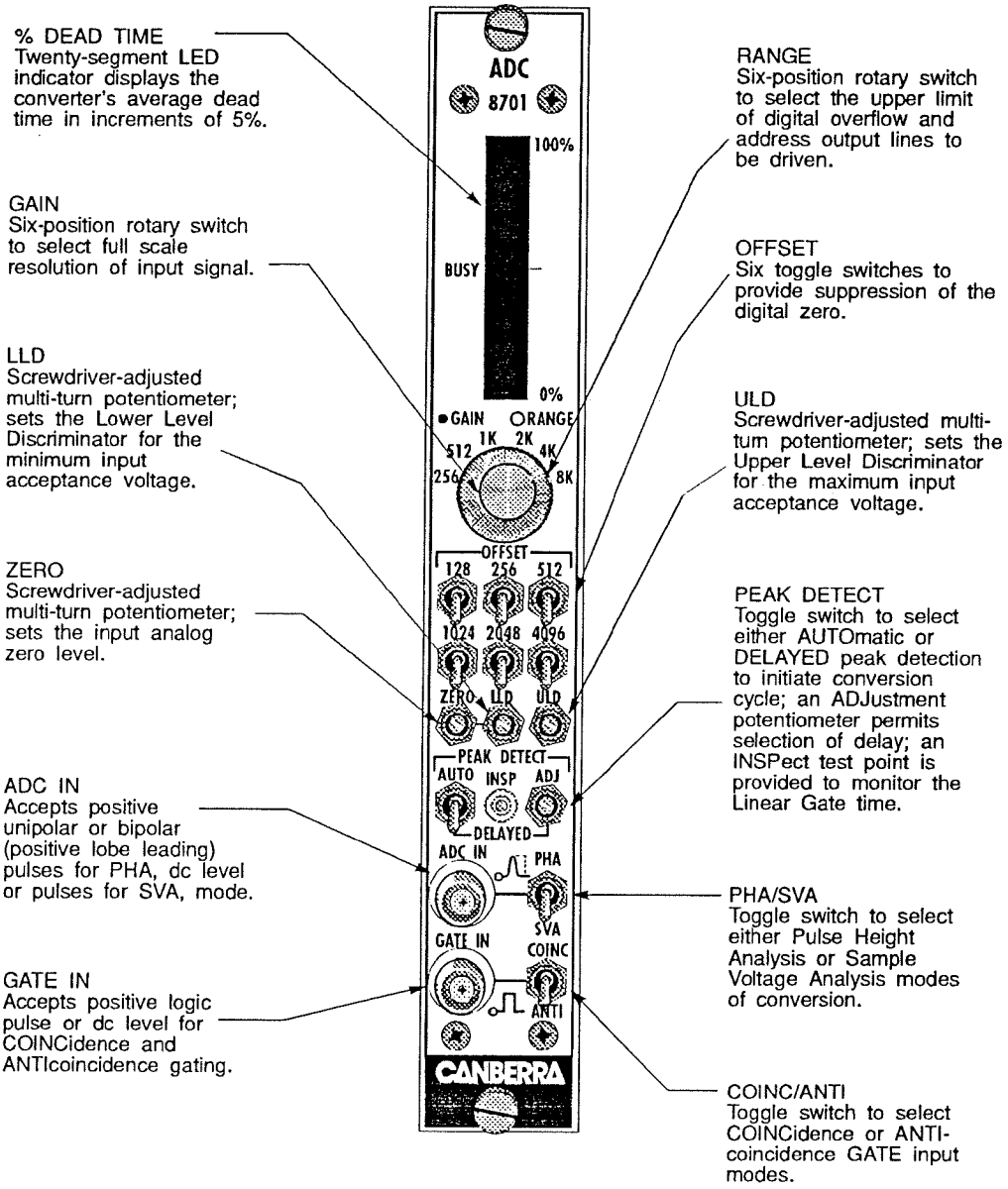


Figure 2.1 Front Panel Controls

2.2. Rear Panel

This is a brief description of the 8701's rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

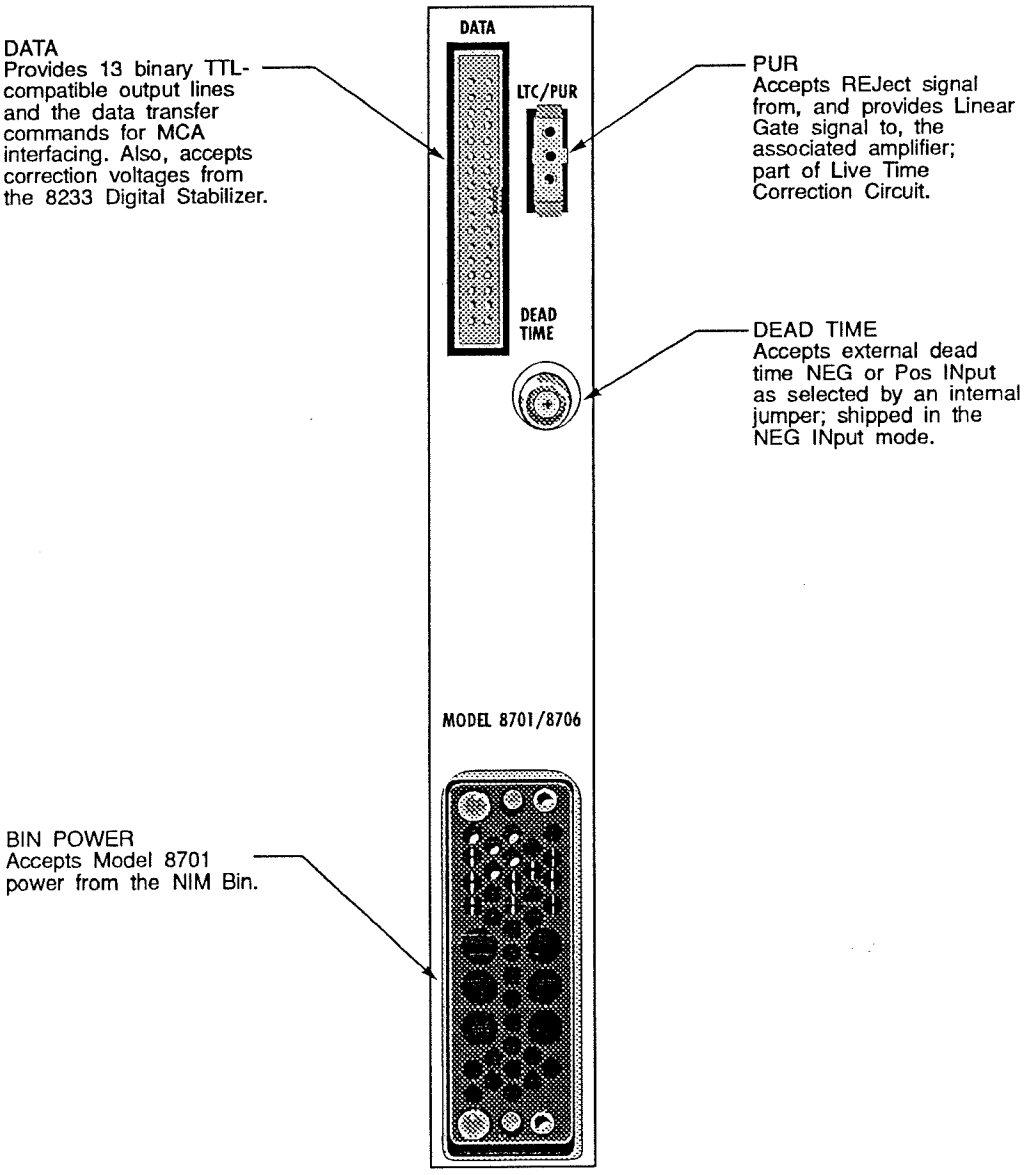


Figure 2.2 Rear Panel Controls

2.3. Internal Controls

The internal jumper plug controls should be set for your specific requirements before applying power to the module.

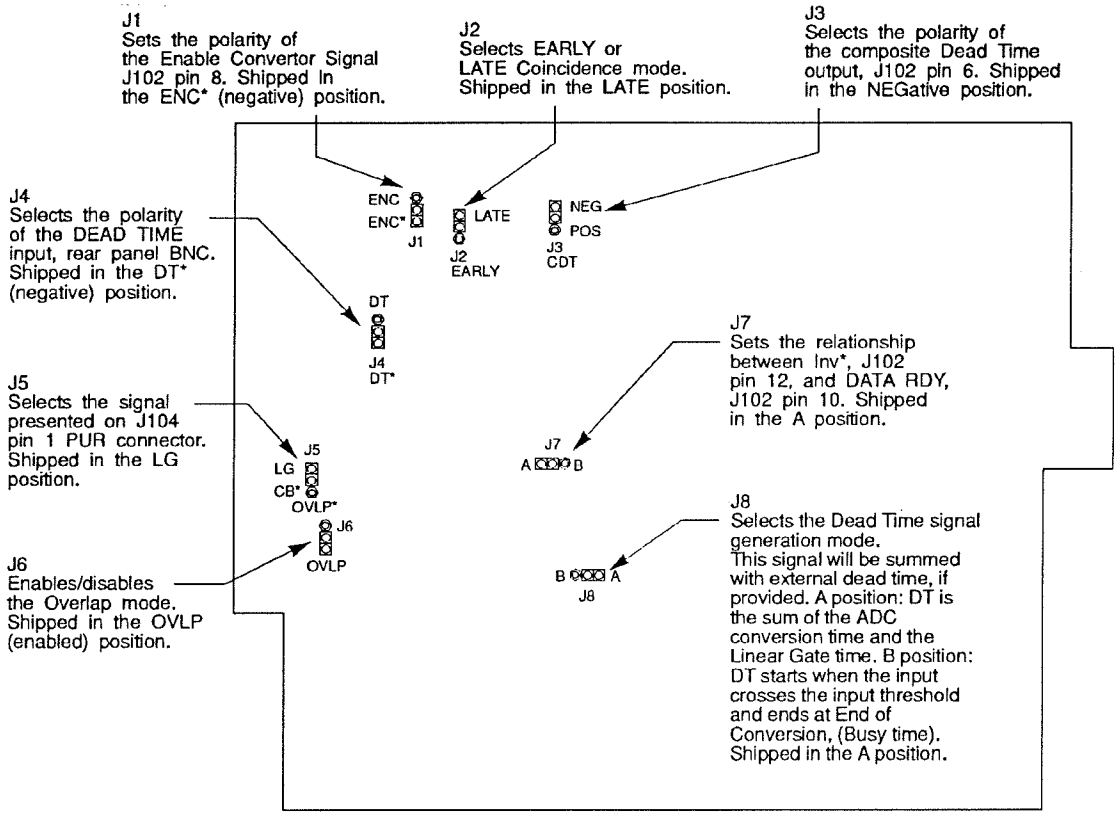


Figure 2.3 Internal Controls

3. Operation

This section discusses the use of the 8701's controls and functions.

3.1. Busy

The BUSY indicator is 20-segment LED display which shows the average dead time in increments of five percent. Dead time (selected by jumper J8 – see Figure 2.3) is the time that the ADC is busy converting an input and increases proportionately with increases in gain and conversions (or both) per unit time.

3.2. Gain

The GAIN controls the ADC's resolution; that is, the number of parts into which the full-scale (10 V) inputs can be divided. The larger the selected gain, the finer the divisions and the greater the resolution.

Note that dead time increases with higher gains because they take longer to convert from analog to digital form. For instance, with GAIN set to 8192 and no OFFSET, the maximum conversion time is 83.5 μs. But with GAIN set to 256 and no OFFSET, the maximum conversion time is only 4.1 μs.

3.3. Range

The RANGE switch is commonly set to equal the size of the MCA memory group assigned to the ADC. For instance a memory assignment of 4096 channels would require a RANGE of 4096.

Inputs which exceed the selected RANGE will not be stored in the MCA's memory. Since the range check is made after the input has been converted, these conversions will add to the ADC's dead time.

3.4. Offset

The OFFSET is used to precisely shift the memory assignment of the ADC's conversions. With no OFFSET (all switches down), the ADC's channel numbers are the same as the memory's channel numbers.

For example, if the GAIN is set to 8192 and the memory assignment is only 4096, an OFFSET of zero will allow only the lower half of the full-scale conversions to be stored. That is, pulses up to five volts will be stored, pulses greater than five volts will not be stored.

If, in this example, the OFFSET were set to 4096 (the 4096 switch up), channel 4096 of the ADC would be shifted down to correspond to channel zero of the memory. This offset would allow the upper half of the full-scale conversions, those above five volts, to be stored in the assigned MCA memory.

3.5. LLD and ULD

The Lower Level Discriminator (LLD) and the Upper Level Discriminator (ULD) controls set the limits for the input signals to be accepted by the ADC for conversion. If an input pulse

falls within the selected window (higher than the LLD setting but lower than the ULD setting) the input will be converted. If the input does not fall within the window, the input will not be converted. The window check is made at the conclusion of the linear gate time. An input pulse outside of the window will add to the ADC's dead time, since no pulses may be accepted for processing by the ADC while the linear gate is open.

3.6. Zero

The ZERO control varies the zero intercept of the ADC conversion so that zero energy is stored in the memory's channel zero. The Model 8701 is shipped with the ZERO set for a GAIN of 8192. For other gains, a slight adjustment of the control may be necessary for precise energy calibration.

For accurate setting of the ZERO control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. Connect the Pulser's SIGNAL OUT to the ADC Input.

2. Set the Pulser to HI, 0°, +, and 0.5 µsec Rise Time.

3. Set the ADC's GAIN control as desired.

4. Set all binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY on, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.

5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be switched in on the ADC. For instance, if the memory is 4096 channels and the GAIN is set for 8192, an OFFSET of 4096 must be added so that conversion can take place in the highest channel of the memory.

6. Turn all binary switches on the Model 8210 OFF, except the 1/64 switch, which should be left ON.

7. Set all OFFSET switches on the ADC to the OFF (down) position.

8. Adjust the ZERO control so that counts are being collected in the proper channel, as follows:

Gain	Channel
8192	128
4096	64
2048	32
1024	16
512	8
256	4

9. Repeat steps 4 through 8 until no further adjustments are necessary.

3.7. Peak Detect

In the AUTO mode, the linear gate, which allows a valid input pulse to be acquired, opens when the input rises above the input threshold. The input threshold level tracks the LLD setting up to 100 mV, maximum; therefore, the input signal's baseline must be less than 100 mV for proper ADC operation.

The linear gate closes when the input pulse falls below 90% of its peak amplitude. Wide input pulses may make the AUTOmatic detection of the 90% point less certain. To overcome this uncertainty, the DELAYED peak detect feature may be used. This feature allows input pulses up to 100 µs wide to be converted. In this mode the linear gate closes at the end of the selected delay time. The delay time can be selected with the ADJ control while monitoring the INSP test point next to the ADJ control.

In either peak detect mode, the INSP test point provides a positive logic pulse; the pulse width represents the linear gate time.

3.8. Gate

Input pulse conversions may be enabled or disabled by using the GATE function. This function is not the same as the linear gate, which is an internal circuit.

In the COINC mode, a positive logic pulse at least 250 ns wide or a positive dc level must be present at the GATE connector during the linear gate time. The opening and closing of the linear gate can be seen at the peak detect INSP test point.

If the GATE input is low during the linear gate time, conversion will not take place.

Internal jumper J2 (EARLY/LATE), is shipped in the LATE coincidence position, which means that the GATE pulse must be present sometime during the linear gate time to be effective. Since a common gating signal is the output of an independent SCA module, this late-arriving pulse can be accommodated by using the DELAYED peak detect mode and adjusting the linear gate time, as seen at the INSP test point, so that the linear gate closes after the SCA's output arrives. Thus the need for delaying the ADC INput signal can be eliminated.

If the jumper is changed to the EARLY coincidence position, the GATE signal must be present before the linear gate opens and remain for at least another 250 ns.

EARLY coincidence is preferable when a high count rate is being gated because appreciable dead time is introduced in the LATE coincidence mode. However, LATE coincidence gating is easier to do since a delay amplifier is not needed.

In the ANTIcoincidence mode, the logic sense of the GATE signal is inverted. That is, a logic low will enable the linear gate and a logic high will disable it.

Note that in the ANTIcoincidence mode, the gating logic must be set for LATE coincidence for proper operation.

In any gating mode, an open GATE (nothing connected to the GATE connector) acts as if an enabling level were present.

3.9. Sampled Voltage Analysis

The ADC is usually used in the Pulse Height Analysis (PHA) mode, but by changing the PHA/SVA switch to the SVA position, analog voltages can be sampled by the ADC. The result will be an amplitude distribution curve of the input signal. The input signal must be between 20 mV and 10 V in amplitude to be sampled. If desired, an amplitude window may be set with the LLD and ULD controls.

The GATE input supplies the sampling signal, which must be equal to or greater than 1 µs in width. However, for pulse inputs (rather than dc levels or slowly changing ac signals), the GATE input signal must be narrower than the input pulse width.

In SVA, the GATE input can also be used to trigger the Delay Timer by placing the AUTO/DELAYED switch to the DELAYED position. This mode allows the use of Gate Inputs which are narrower than 1 μs. In this configuration, the COINC/ANTI switch is used to select the triggering edge, rising or falling. COINC selects rising and ANTI selects falling. As in the PHA mode, the ADJ control is used to set the delay time.

The sampling rate should be at least twice the frequency of the input signal for accurate sampling.

For proper dead time in the SVA mode, J8 must be in the B position.

3.10. Rear Panel Connectors

J101 DEAD TIME – A BNC connector which is used as an external dead time input from Canberra Amplifiers equipped with PUR/LTC. This input is ORed with the ADC Dead Time. Accepts a negative or positive logic signal jumper, selectable via J4; shipped in the negative position.

J102 DATA – Used to connect the ADC to an MCA, an AMX, a Digital Stabilizer, or an LFC module. The proper cable is supplied with the MCA.

J104 LTC/PUR – Accepts the REJect signal from, and provides the Linear Gate (LG) signal to, Canberra Amplifiers equipped with PUR/LTC.

Further information and signal specifications for these connectors can be found in Appendix A, Specifications.

3.11. ADC Interfacing

This ADC improves its throughput by using a data buffer, or overlap mode, which allows it to accept another analog input and start converting it while the previous conversion is being transferred from the buffer to the memory unit. In the unlikely event that the conversion finishes before the previous data has been transferred from the buffer, the new data is momentarily held in the counter and no new conversion can start until the DATA ACCEPTED signal is received.

The result of the ADC's conversion is a 13-bit binary-coded number. At the end of the Wilkinson ramp time, this number is transferred into a holding register (buffer) and signal DATA READY is set true. The address data is valid and can be used by the MCA and the ADC is free to begin another conversion.

The DATA lines are driven by tri-state drivers that are controlled by the ENABLE DATA input. The DATA ACCEPTED input signals the ADC that the current output data has been transferred and the result of the next conversion can be loaded into the buffer.

In a synchronous application, such as Multiparameter Acquisition, it is necessary to operate the ADC in a non-overlap mode, disabling the internal buffer. In this mode, the ADC cannot accept a second input for conversion until the first conversion has been accepted by the MCA. The non-overlap mode is selected by placing J6 in the OVLP position. The ADC is also automatically placed in the non-overlap mode when used in SVA. This is required by the 8223 and 8224 AMX modules.

Invalid inputs normally are not stored by the MCA. In the overlap mode, invalid inputs are converted but are not stored in the buffer and the DATA READY signal is not generated. In the SVA and non-overlap modes, invalid events are converted and the ADC generates the

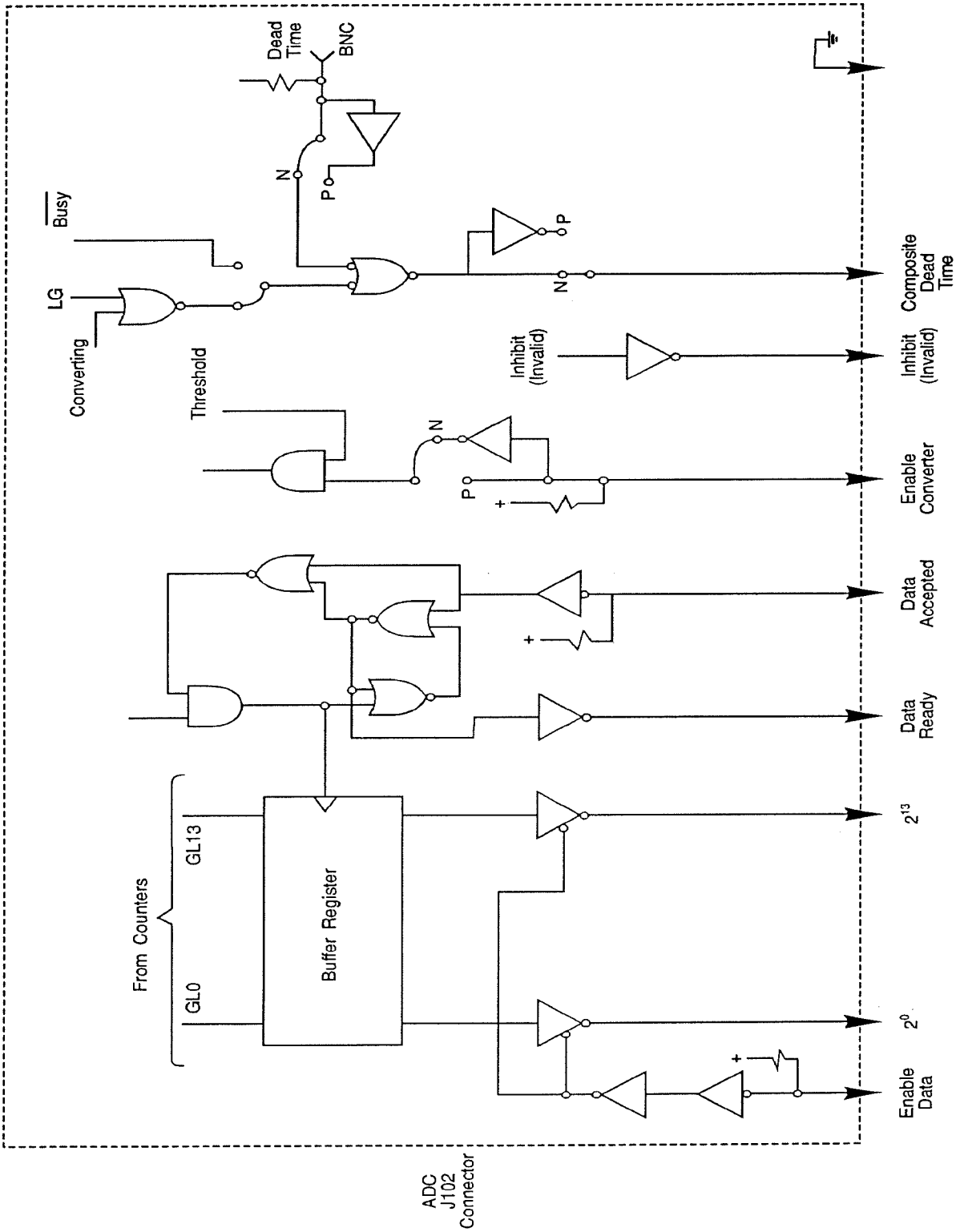


Figure 3.1 Interfacing Logic
(Refer to Schematic B-26960)

DATA READY and INHIBIT output signals. This causes the MCA to service the ADC; that is, the DATA ACCEPT and ENABLE DATA signals will be generated, but the data will not be stored by the MCA because of the INHIBIT signal. Invalid inputs are defined in "Invalid Flag Conditions" on page 10.

It may sometimes be necessary to record all inputs whether valid or not. This is true for Multiparameter or other synchronous applications. For this case, the ADC must be configured in the non-overlap mode, J6 in the OVLP* position, and J7 must be placed in the B position which will inhibit the generation of the DATA READY signal for invalid inputs. In this configuration the INHIBIT signal is now considered an INVALID signal, flagging an invalid input but not inhibiting storage.

The ADC is not normally inhibited from processing later events if the current conversion in invalid because the DATA READY signal is not generated when the ADC is configured to generate INVALID (instead of INHIBIT) signals. Thus, without using the GATE or ENABLE CONVERTER inputs, there is no INVALID/DATA synchronization.

The ENABLE CONVERTER input (J102, pin 8) or the front panel GATE input can be used to inhibit a later conversion and thus synchronize multiple ADCs.

The COMPOSITE DEAD TIME output is the sum of the conversion time and the time that the input is above the threshold (20 to 100 mV). The output signal begins when the input signal exceeds the input threshold and ends when the conversion is complete or the input signal goes back below the input threshold, whichever time is longer. An internal jumper, J8, can change the COMPOSITE DEADTIME to be the sum of the Linear Gate Time and the ADC Conversion Time. The output signal would start with the Linear Gate and end with the completion of the ADC conversion. It does not include the time that it may take the input to go below the threshold.

If an external Live Time Corrector (for example, the Model 2024 or 2025 Amp) is used, its BUSY signal is summed with the ADC DEAD TIME. The ENABLE CONVERTER signal and gate signal make no contribution to the dead time, although when false, they do inhibit conversion.

3.12. Invalid Flag Conditions

For a conversion to be accepted, it must meet all of the following criteria. When violated, the INVALID flag (J102, pin 12) will be set if the ADC is configured to do so (see Section 3.11).

SCA Window

Pulses not in the SCA's analog window will be rejected, initiating a dump cycle. An LLD or a ULD violation will generate the INVALID flag. Both states are interrogated at the 90% point.

Baseline

Input pulses not exceeding the ADC ZERO baseline will be rejected, initiating a dump cycle. The condition is interrogated at the 90% point, setting the INVALID flag when violated.

Digital Underflow

Input pulses resulting in a numeric conversion less than the counter back-bias or less than the digital offset, or both, will be rejected by inhibiting ADC READY. The INVALID flag will be set at EOC (end of conversion).

Digital Overflow

Input pulses resulting in a numeric conversion greater than the ADC RANGE will be rejected by inhibiting ADC READY. The INVALID flag will be set at EOC (end of conversion).

Late Coincidence/Anticoincidence

The GATE pulse width must be at least 250 ns wide and be true (high for coincidence, low for anticoincidence) for at least 100 ns before the 90% point or the end of Linear Gate. Otherwise the conversion is aborted by initiating a dump cycle. The INVALID flag will be set at the 90% point.

Early Coincidence/Anticoincidence

The GATE pulse width must be at least 250 ns wide and be true (high for coincidence, low for anticoincidence) for at least 100 ns before the initiation of ADC BUSY as determined by an ADC input pulse crossing the ADC input threshold. Otherwise the INVALID flag will be set at the trailing edge of the GATE pulse.

3.13. Preventative Maintenance

Preventative maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap, side or rear panels.

4. Theory of Operation

In this chapter, all negative true signals are shown with a trailing asterisk (RAMP ON*); all other signals are positive true. Each section of the Theory of Operation includes the relevant schematic sheet number after the section title. A timing diagram is included at the end of this section for reference.

4.1. Stretcher [Sheet 1]

The Stretcher is a discrete op-amp configured as a positive peak detector/holder including a calibrated precision ramp-down circuit. The peak holder has negative feedback via R28 and C9 providing a gain of +1. The Stretcher includes transistors Q5 through Q7, Q9 through Q23, and IC A55. Transistor array A55 is connected as a Darlington differential amplifier and allows a larger dynamic range at its input. Thus, the input signal is connected directly without attenuation, for an improved signal-to-noise ratio characteristic.

FET Q17 and transistor Q12 are connected to form a buffer providing low output and high input impedances. R21 and C7 form a low-pass filter limiting the input high-frequency noise and rise time. Diode D5 provides a negative input clamp. Q22 and Q23 are constant-current sources. Their bases are biased to about –16 volts and +16 volts respectively.

R34 sets Q22's collector current to about 6 mA, while R13 sets Q23's collector current to about 3 mA, allowing the differential stage to balance. RV10 can vary Q22's collector current by about ±2%, enabling the differential amplifier to be precisely balanced, establishing the Stretcher Output dc offset. The two current sources are slaved together providing good power supply rejection and thermal stability.

Pin 8 of the differential amplifier drives the base of Q18. When the differential amplifier receives a signal more positive than the peak holder output, A55 steers current, turning Q18 on. Q18 supplies current limited by R14 and charges capacitor C12 through Cascode Q16. The base of Q16 is biased by R17, R19 and R36 to about +10 volts. A55 and Q18 continue to source the precision current to C12. The resultant voltage generated on C12 is buffered to the Stretcher Output by FET follower Q17/Q12 and follows the positive transition of the input signal.

When the input signal slope reduces to zero, or goes negative, A55 steers all current through pin 12. Q23 now pulls the base of Q18 positive, turning it off. R18 is included to ensure that Q16 also turns off when current from Q18 extinguished. With the ramp and Q18 off, the voltage developed on C12 remains until the rampdown cycle begins. R29 adds a zero to the peak holder transfer-function, ensuring stability. Signals present on C12 are voltage-translated slightly negative because of the output-buffer offset.

The output buffer supplies a buffered signal to the differential-amplifier negative input (A55 pin 9) via feedback resistor R28, zero-crossing comparator, and Stretcher/Input interrogation comparators. During the ramp-down cycle, the peak holder is gated OFF; that is, input signals can no longer influence C12. Q19 and Q20 are connected as a differential switch which normally biases the base of Q21, in conjunction with R8 and R10, to about +12 volts. Thus, Q21's base-emitter junction is reversed-biased outside Q18's voltage-control range, allowing the peak holder to operate normally.

However, just before the ramp-down cycle, the STR OFF signal is set true and current through R7 is steered from Q20 to Q19. The base of Q21 is now increased to about +16.5 volts an reverse biases the base-emitter junction of Q18, disabling the Stretcher.

4.2. Ramp-down Generator [Sheet 1]

The ramp-down generator is a gated precision-current source. A constant sink-current is developed and switched between ground (ramp off) and the peak holder storage cap (ramp on). The ramp-down circuit includes diodes D6, D7, transistors Q5 through Q7, Q9 through Q11, Q13 through Q15 and op-amp A54. D6 and D7 are 6.2 volt Zener diodes, referenced to the –24 volt supply, producing a temperature stable reference voltage source of –11.6 volts referenced to ground. This reference voltage is attenuated by R51, R53, RV9 and applied to the input of op-amp A54.

Transistors Q5 and Q6 perform a voltage-to-current transformation. The op-amp input reference voltage (A54 pin3) also appears at the emitter of Q5, establishing a constant voltage across the current set (conversion gain) resistors (R54 through R60) producing a precision current-flow. Since the transistors' combined current gains are high, the same current also flows through their collectors. R54 and R55 set the 8192 gain or ramp current. Resistors R56, R57, R58, R59 and R60 set the 4096, 2048, 1024, 512, and 256 conversion gains or ramp currents respectively. The ramp current is precisely calibrated using RV9.

The precision ramp current is steered to ground or the peak-holder storage capacitor by current steering transistors Q13 and Q14. These transistors are connected as a differential switch. For the ramp down or track modes, the control logic sets RAMP ON* to a logic 0. Thus the base of Q11 is biased more negative than that of Q10. Collectors Q11 and Q10 bias the base of Q14 more positive than that of Q13, setting Q14 ON, and Q13 OFF. The precision ramp current flows through Q14 and Q15, sinking current from the holding capacitor.

Q15 is a Cascode with its base biased at about –5 volts by resistors R17, R19 and R36. This negative current flow continues for the duration of the RAMP ON* Signal. Capacitor C12 is discharged with a high degree of linearity towards –24 volts. However at the zero crossing, the control logic sets RAMP ON* to a logic 1 setting Q14 OFF and Q13 ON. The constant current is now steered to ground through Q13; current no longer flows from the storage capacitor.

For an invalid conversion, the Control Logic sets DUMP to a logic 1. Q7 and Q9 are both biased on, a current (significantly higher) determined by R46, independent of the precision current generator, now dominates, producing a much faster RAMP DOWN or DUMP cycle.

4.3. Stretcher/Input Interrogation Logic [Sheet 1]

The Stretcher/Input interrogation logic is made up of comparators A37, A38, and op-amp A34. A38 pin 7 generates a logic 0 (ITHR*) whenever the ADC input signal exceeds the threshold reference voltage. The threshold reference voltage is generated by R167, R64 and op-amp A34. R167 and R64 are set for +100 mV. Normally the output of A34 would follow the LLD voltage. However, if the LLD reference voltage is set higher than +100 mV, diode D8 reverse biases and the threshold reference voltage is limited to +100 mV. For LLD voltages of +100 mV and less, diode D8 forward biases, forcing the threshold reference voltage to track the LLD down to 0 volts.

The 90% comparator (A37) monitors both the Stretcher Output (pin 3) and ADC input (pin 2). The Stretcher Output is attenuated by 10%, determined by R31 and R77. Thus for a given ADC input, pin 2 is more positive than pin 3 (Stretcher output), setting A37 pin 7 to a logic 1. When the ADC input reduces about 10%, and becomes slightly lower in amplitude compared to the captured Stretcher signal, A37 pin 7 is set to a logic 0 (90% indication).

Comparator A37 has 3.5 mV of hysteresis determined by R76, and 5 mV of offset determined by the Stretcher Output offset. A38 has 5 mV of ac hysteresis determined by C31 and 8 mV of offset determined by R111. The Stretcher Output is connected to the 90% comparator through

a filter: R31, R32, R77, C14, C35 and L2. The filter limits the amount of digital and switching noise that might otherwise be fed back to the Stretcher Output.

4.4. SCA [Sheet 1]

Comparators A35 and A36 compare the Stretcher Output with the LLD and ULD reference voltages respectively. If the Stretcher Output is above the LLD threshold, A35 pin 7 is set to a logic 0 (LLD*). If the Stretcher Output is above the ULD threshold, A36 pin 7 is set to a logic 0 (ULD*). The LLD and ULD reference voltages are calibrated to +9.0 and +9.6 volts respectively, using R3. The LLD and ULD reference voltages are scaled in proportion to the front panel LLD (RV2) and ULD (RV1) settings, covering a range of 0 to +10.0 and 0 to +10.7 volts respectively, when referenced to the ADC Input.

Components R71, C28, R67, and C24 provide 12 mV of hysteresis and pre-bias for the LLD and ULD comparators respectively. Since the LLD comparator (A35) is prebiased to 20 mV, referenced to the ADC Input, the LLD's fully CCW position is also limited to 20 mV.

4.5. Zero-crossing Discriminator [Sheet 1]

The zero-crossing discriminator includes FET Q8 and comparators A53 and A48 (Sheet 2). The zero-crossing comparators interrogate the Stretcher Output (TP4), ending the ramp-down and synchronizer/counter cycles when the negative ramp reaches the baseline (zero) reference voltage. Two comparators (A53 and A48) are used in cascade for improved comparator gain, also providing analog-to-digital buffering.

FET Q8 serves as a limiter. For Stretcher Output signals 2 to 3 volts more positive than the comparator reference input (A53 pin 3), the FET pinches off and becomes a high impedance. For smaller signals, Q8 remains a low impedance, connecting the Stretcher Output to comparator input (A53 pin 2). Resistor R79 and diode D9 serve as a load when the FET is pinched off, maintaining a voltage more positive than that of the reference voltage.

For Stretcher signals more positive than the baseline (zero) reference voltage, A53 pin 7 is set to a logic 1. A 48 pin 7 is set to a logic 1 while A48 pin 5 is set to a logic 0, enabling the synchronizer and address counter. When the Stretcher ramps down until the Stretcher signal equals or become more negative than the baseline (zero) reference voltage, A53 pin 7 is set to a logic 0. A48 pin 1 sets its outputs (7 and 5) to a logic 0 and 1 respectively, ending the ramp-down and synchronizer/counter cycles.

The baseline (zero) reference voltage is set by the front panel ADC zero control RV3, and resistors R81 through R83 and R61 through R63. The control covers a range of ±5%. The baseline (zero) reference voltage can be remotely set to ±2% (determined by R84) for a ±5 volt signal at the VZERO input, pin 30 of J102.

4.6. 100 MHz Oscillator [Sheet 2]

The oscillator consists of Q2 through Q4, a 100 MHz crystal and associated resistors, capacitors and inductors. The oscillator is of the Colpitts design. L6 in parallel with C44 and C45 forms a tank circuit which resonates a 100 MHz. C47 is also in parallel with C44, C45 and L6 for fine tuning. The two tank capacitors, C44 and C45, also form a capacitor attenuator, providing voltage feedback through the 100 MHz crystal. This feedback is essential to sustain oscillation. L7 in parallel with the crystal resonates with the crystal capacitance, increasing its apparent series impedance, lowering its series current.

Q3 and Q4 are complementary emitter-followers biased class C. They drive resonant load L10 and C50 through ac coupling capacitor C49. The Oscillator Output is connected to the Synchronizer Input A43 pins 1 and 13, and Address Counter A44 pin 1, via resistors R95 and R96 respectively. D11 provides about 1.4 volts of bias to the Oscillator Output through inductor L10. L10, representing a low impedance to the dc bias voltage, appears as a high impedance to the 100 MHz clock signal.

4.7. Synchronizer [Sheet 2]

A43 is configured as a synchronizer and serves to synchronize the Ramp on and counter functions with the 100 MHz clock. When the control logic receives the START signal, SCD (Start Convert Delayed) is set to a logic 1, removing the synchronizer clear. A ramp-down sequence is initiated. On the very next negative clock transition, Q and Q* of A43a are clocked to logic 1 and 0 respectively. Q and Q* of A43b are clocked to a logic 1 and 0 on the negative transition of the second clock. Two things happen simultaneously: the address counter is armed to begin counting the 100 MHz clock, and the control logic initiates a Ramp On command by setting RMP ON* to a logic 0 via the SYNC* signal.

The ramp current is steered to the peak-holder storage cap and linearly discharges the cap at a rate proportional to the conversion gain setting. When a zero crossing is detected by the zero-crossing discriminator, the J and K inputs of A43a are set to a logic 0 and 1 respectively. On the second clock, Q and Q* of A43b are also set to a logic 0 and 1 respectively. Simultaneously, SYNC* is set to a logic 1 (false) and the address counter input is gated off. On the positive transition of SYNC*, the EOC (End of Conversion) logic is initiated.

4.8. Counter Logic [Sheet 2]

The address counter consists of A44 through A47 and is configured as a 14-bit ripple counter. The 14th bit is used for under- and overflow detection. During the ramp-down sequence, the ramp counter and ramp current are enabled and synchronized to the 100 MHz clock. When the zero-crossover point is reached, the zero-crossing discriminator and synchronizer gates the address counter off synchronously with 100 MHz clock. The resultant digital address in the address counter represents the magnitude of the ADC analog input.

Since the beginning of the ramp may be nonlinear, the counter is offset by –64 counts on 8192 conversion gain. This allows the counter to count using the more linear region of the ramp-down signal. An additional 16 counts are subtracted to cancel analog propagation delays in the ramp start-up. Thus the total counter offset for 8192 conversion gain is –80 counts. The zero-crossing discriminator is back-biased about –80 mV, compensating for the digital counter offset. As the ramp current increases for other conversion gains, less digital offset is required to compensate for the zero-crossing back-bias. Total counter and analog offsets for the various conversion gains are shown in the following table.

Conversion Gain	Digital Offset	Analog Zero Offset
8192	80 counts	80 mV
4096	48 counts	80 mV
2046	32 counts	80 mV
1024	32 counts	200 mV
512	32 counts	400 mV
256	32 counts	800 mV

Additional analog back-bias for 1K, 512 and 256 conversion gains is provided by resistors R61 through R63. The actual analog zero-offset required is slightly lower than the digital equivalent back-bias, since analog propagation delays are slightly less than the 16 channels assigned.

Digital offsets are selected using front panel switches (S2 through S7) to pull the respective counter preset line to logic 0. ADC digital offset presets the address counter in increments of 128, 256, 512, 1024, 2048 and 4096 counts. All counter offsets are loaded into the counter before the start convert command (SC*). The sliding-scale digital offset is also loaded into the counter before SC*.

A39 through A42 perform digital addition, adding the ramp counter data with the sliding-scale complement. The data, with sliding-scale removed, is presented to the octal three-state latched bus drivers A1/A2 to drive the data bus.

Transistor Q1 gates off the adders by removing 5 volt power, preventing the internal data bus from being active during the ramp-down sequence.

4.9. Sliding Scale [Sheet 2]

The Sliding-Scale Counter (A8) presets the address counter with a different preset, ranging from 0 to –15 counts, at the end of each conversion. With the address counter preset to a different offset for each conversion, logic noise from the counters will be reduced by an averaging process. At the end of each conversion (EOC) the control logic clocks A8, a 4-bit counter. The complement of the digital word is stored as a negative offset in the address counter before SC* (Start Convert). Adders A39 through A42 add the sliding-scale complement to the ramp address data. In effect, this removes the sliding-scale component from the address counter data.

4.10. Range/Overflow Logic [Sheet 2]

The address range data is selected by the Range switch SD1a for digital comparison. The range data and corresponding address bits QL8 through QL12 are compared by digital comparators A9 and A10. If the address counter does not count past the digital pre-bias or if it exceeds the range selected, the comparator <R (A10 pin 7) is set to a logic 0. The <R signal instructs the control logic to inhibit the ADC ready signal for that conversion. Thus the under- or overranged data is not stored in the MCA memory.

When the address counter offset is loaded, the 8192 bit is set to a logic 1. The counter must count past the digital pre-bias before the 8192 bit is set back to the logic 0. Thus the 8192 bit is also used as an underflow indication. If at the end of a rampdown sequence of the 8192 bit remains high, the <R flag would again be set, inhibiting the ADC ready for that underflow conversion.

4.11. Control Logic [Sheets 3 and 4]

The 8701's Control Logic is described in detail in the following seven subsections.

Initialize

At power ON, A3 pin 6 generates PR, the power-reset pulse. The SC flip-flop (start convert A20a) is cleared via A14 pin 10, the 90 flip-flop (A25d) is preset, setting A12 pin 6 to a logic 0. Since A12 pins 6 and 5 are both logic 0, A 12 pin 4 sets DUMP true (logic 1). The Dump cycle concludes when the Stretcher Output returns below the Stretcher zero-crossing reference (GZR) or LLD reference, as determined by their respective comparators. The 90 flip-flop (A25d) is cleared via A28a, A23b, A24b, and A26c. DUMP returns to logic 0 via A25d and A12b, ending the Dump cycle. PR also generates RESET via A22 (on sheet 5).

RESET clears the BUSY (A21b) and COINC (A16) flip-flops. Since the SC (A20) and 90 (A25d) flip-flops have both been cleared, STR OFF and DUMP are false, logic 0. LOAD* is true, logic 0, the sliding-scale preset is loaded into the address counter. Since the Busy flip-flop (A21b) was cleared, TRK (track) is set to a logic 1 via A32c, A23a, A5b, and A12a. With TRK set true, RMP ON* is set to a logic 0. Thus both the peak holder and ramp are active. The Stretcher now acts as a voltage-follower op-amp and will track the ADC input signals.

PHA (Pulse Height Analysis) Mode

When PHA is selected, by S8, the B inputs of multiplexer A26 are connected to its Y outputs.

The arrival of an ADC Input signal having an amplitude that exceeds the input reference threshold sets ITHR* to a logic 0. Assume that ENABLE CONVERTER (J102-8) is at the proper logic level to enable the ADC and J2 is set for the LATE coincidence mode. The D input of the BUSY flip-flop (A21 pin 12) is set to a logic 1. ITHR* sets the BUSY flip-flop (A21b) to busy. Linear Gate (LG*) is set true (logic 0) via A32c, A23a, A28b, and A33f. Track (TRK) is set to a logic 1 via A32c, A23a, A5b, and A12a. TRK sets A19 pin 4 to a logic 1 and RMP ON* (A19 pin 6) to a logic 0. The ramp is switched off, setting the Stretcher to the acquire mode. When the Stretcher is charged to the peak value of the ADC Input and the input signal reduces about 10% in amplitude, 90% is set to a logic 0.

The 90% signal is connected to a leading-edge discriminator via AUTO/DELAYED switch S7 and A16, (on sheet 5) labeled TOP* (time of peak). With LG* set to a logic 0, A30c is enabled and a positive logic pulse is multiplexed to the Start Convert flip-flop (A20a) via A26b and the 90 flip-flop (A25d) via A26b and A14d (called START). With COINC, PHA BUSY* and GZR* set true, A29c and A30b are enabled. If the ADC Input and Stretcher Output signal amplitudes are above the LLD and below the ULD, with no external REJ (reject), VALID (A30 pin 6) enables the Start Convert flip-flop (A20a) by setting its D input to a logic 1. Thus both the Start Convert (A20) and 90 (25c) flip-flops are set.

With the 90 flip-flop (A25d) set, A28 pin 6 is set to a logic 1 via A18f. Thus LG* has ended, disabling A30c and preventing any further TOP* and start logic pulses that might otherwise appear. Notice LG* is set low only during the Stretcher Acquisition Mode. With the Start Convert flip-flop set, the Stretcher is gated off via the STR OFF signal. The Stretcher is now holding the peak value of the ADC Input signal waiting for the Ramp down cycle to begin. A20 pin 5 sets the LOAD* signal false (logic 1) and the address counter is ready to count.

About 50 ns later, determined by A27a, A27b, R126 and C69, SCD is set true (logic 1) enabling the synchronizer. The synchronizer, as described in "Counter Logic" on page 15, sets SYNC* to a logic 0, initializing the ramp-down cycle. SYNC* re-enables the Stretcher ramp via A18c and A19b. SYNC* also sets the EOC (end of conversion) flip-flop, setting

monostable A17 pin 9 to a logic 1. A12d interrogates the status of the DAC (data accepted), and RDY (ready) signals. If, from a previous conversion, these signals have concluded, A12 pin 13 enables gate A24c. When the ramp-down cycle is completed, resulting from a zero crossing detection, SYNC* returns to a logic 1 initiating the EOC cycle. Monostable A17b generates a pulse about 500 ns in duration.

The leading edge of A17 pin 12 sets flip-flop A25a (on sheet 5), setting ADDEN* (adder enable) to a logic low via A27d, enabling the adders and the internal address bus. When A17b times-out, A17a is set, generating EOC and, through A13a, clocks the address data (QL0 through QL12) into the octal latch three-state Bus drivers A1 and A2. EOC also clocks the RDY flip-flop (A20b) and, if the RANGE criteria were not violated, A20b sets DATA READY true, initiating the MCA data storage cycle.

At the conclusion of EOC, flip-flop A25a is reset and the adders are disabled by setting ADDEN* to a logic 1 via A27d. When the MCA has completed the data storage cycle, the MCA generates the DATA ACCEPTED signal setting ADCR* (ADC release) to a logic 0. ADCR performs several tasks: clocks the three-state octal latch bus drivers, loads all logic "1's" from the disabled adders via A13a; and clears the RDY (A20b) and INVALID (A22) flip-flops. The RDY, and DAC signals also inhibit any subsequent EOC/data storage cycles by inhibiting A24c via A12d until the MCA data storage cycle is complete.

EOC also initiates a RESET command via A22. RESET flip-flop (A25b) remembers that EOC has occurred. When the Stretcher Output has returned below the LLD or zero-crossing reference and the ADC Input have returned below the input threshold reference, the 90 flip-flop (A25d) is cleared via A28a, A23b, A24b, and A26c.

The 90 flip-flop clear (90CLR*) is gated with the RESET flip-flop data by A27c, clearing the Start Convert flip-flop (A20a) via A14c. The ADC Conversion cycle is now complete; the ADC is enabled to begin another conversion.

If the conversion was invalid because of a digital under- or overflow, the <R flag would be set low, inhibiting the RDY flip-flop (A20b) from being set. The data storage cycle would not have taken place and the invalid data would be thrown away setting INV (invalid) true.

Auto Clear

A18a and A19a are configured as a trailing edge discriminator. If A19a is enabled, it will generate a positive pulse when the ADC input signal returns below the input threshold reference via ITHR* returning to a logic 1.

For a valid conversion, both the SC flip-flop and 555 timer are set. Depending on whether DELAYED or AUTO PEAK DETECT mode has been selected, A16 routes the respective signal to A19 pin 13 inhibiting the AUTO clear functions. For certain conditions it is possible for the BUSY flip-flop (A21B) to be set without the 90% or manual 555 being set. For this case the SC flip-flop would also not get set, A19a would be enabled. The BUSY (A21b) and COINC (A16) flip-flop would then be cleared via A33e, A18a, A19a, and A14a when the ADC Input signal returned through the input threshold.

Delayed Peak Detect

If the DELAYED PEAK DETECT Mode has been selected, the 90% interrogation comparator is replaced by a 555 timer via A31 and A16. Thus the TOP signal that starts the ADC ramp, EOC, and MCA storage cycles is now initiated by the trailing edge of A31 pin 3. A31 is configured as a front-panel programmable monostable, covering a range of about 2 to 100 µs, by RV4, R150 and C85. The leading edge of LG (Linear GATE) used to start the monostable time-out period is detected by A15c, A15d, R170 and C124.

Coincidence Logic

LATE Coincidence, ANTI Coincidence and EARLY Coincidence may be performed. The GATE Signal must be 250 ns or wider, and for LATE coincidence, must occur within the Linear Gate time. EARLY Coincidence may be selected by moving the EARLY/LATE jumper plug (J2) to the EARLY position. The EARLY GATE signal must precede the ADC Input Threshold Crossing by 50 ns.

With LATE Coincidence selected, S9a connects R129 to +5 volts, biasing the GATE input to the enable mode (logic 1). During the Linear Gate, A16 pin 17 is set to a logic 1 via A28c and A11a. If GATE remains positive during LG, the Coinc flip-flop A16 is set. A16 pin 20 enables A29c. If the LLD, ULD and REJ criteria are satisfied, the Start Convert flip-flop VALID proposition will be set true and allow the conversion to take place.

With ANTI-LATE Coincidence selected, S9a connects R129 to –12 volts, biasing the GATE input to a logic 0. A16 pin 20 enables A29c and allows the pending Conversion to take place provided the LLD, ULD, REJ criteria remain satisfied. However if the GATE input is set positive during Linear Gate, the COINC flip-flop will be set. A16 pin 20 will now be set to a logic 0 disabling A29c. At the conclusion of Linear Gate, the ADC will go into the Dump mode and abort the respective event. In all cases the COINC flip-flop is reset by RESET via A21d at the end of each Conversion attempt.

Dump

If the ADC input signal did not satisfy the LLD/ULD, Coincidence criteria or a REJ was initiated, the pending Conversion will be aborted. For this case both the 90 flip-flop (A25d) and SC flip-flop (A20a) are clocked as before. However, the SC flip-flop proposition (A20 pin 2) is false (logic 0) and the flip-flop will not get set. With only the 90 flip-flop (A25d) set, DUMP is set true (logic 1) via A12b. The Dump cycle rapidly discharges (about 6.7 V/µs) the Stretcher holding capacitor C12.

When ITHR* and GZR* or LLD* return to a logic 1, the 90 flip-flop (A25d) is cleared ending the Dump cycle and arming the ADC for the next Conversion attempt. An INV (invalid) flag will be set, RDY (ready) will not be set, and an MCA Storage cycle will not occur. REJ (reject) is gated with LG* via A16, therefore, to perform a reject/Dump; reject must occur during the LG time window. PR (power reset) also initiates a dump sequence via A3b, A14c, and A14d.

SVA (Sampled Voltage Analysis) Mode

With SVA selected, the A inputs of multiplexer A26 are connected to the Y outputs. PHA is set to a logic 0 disabling the Busy flip-flop (A21b) via A13c. TRK is set to a logic 0 via A5b and A12a. Only gates A33a and A18d are used for the Gate function; the remainder of the Coincidence logic is not used. Before a positive Gate pulse, the SC flip-flop A20a is held cleared via A16, A26d, A27c, and A14c. The 90 flip-flop (A25d) is held preset via A16 pin 10 and A26c.

Both RMP ON and DUMP are set true while STR OFF is held false. Thus the Stretcher is in the fast-track mode and follows the ADC input signal. When the Gate signal is set positive, the 90 flip-flop (A25d) is cleared via A16 pin 10 and A26c. RMP ON* and DUMP are set false, placing the Stretcher in the hold mode. If the Stretcher Output signal is within the SCA Window, pin 2 of the SC flip-flop (A20a) will be set a logic 1 via A30a and A26a, enabling the flip-flop.

Coincident with the trailing edge of Gate, the SC (A20a) and 90 (A25d) flip-flops are set via A16 pin 10, A26b and A16 pin 10, and A26b and A14d, respectively. The ramp, EOC, and MCA storage take place sequentially as described in "PHA" on page 17.

In the SVA DELAYED mode, the SVAGAT signal at A16 pin 10 is extended by the one-shot, A31, which is triggered on either the rising or falling edge of the GATE input pulse as determined by the COINC/ANTI switch: COINC selects the rising edge, ANTI selects the falling edge.

4.12. Invalid Logic [Sheet 5]

For events which don't satisfy the LLD, ULD, REJ, and COINC criteria, the event is said to be invalid and the ADC defaults to the Dump mode at the Linear Gate conclusion. For events which result in a digital under- or overflow, invalid condition is determined at the End of Conversion, and the data is discarded.

Invalid events are handled in different ways based on the ADC's mode of operation. In SVA mode, an invalid event will set both the DATA READY and INHIBIT signals. This is also true when the non-overlap mode is selected via J6. In the overlap mode, neither the DATA READY nor INHIBIT signals are set, allowing for the fastest system throughput.

The invalid logic is contained in the PAL A22. The following description defines the conditions which would set the INHIBIT signal assuming the ADC was set to the proper mode as defined above. The Dump signal's leading edge clocks the invalid flip-flop to a true state generating the INHIBIT (INVALID) signal at A22 pin 17. The only instance where this is not the case is in the occurrence of REJ. If REJ occurs during Linear Gate, the Invalid flip-flop is disabled and the generation of INHIBIT is blocked.

Events that result in digital underflow or overflow will set INHIBIT. <R is interrogated during the EOC cycle. If <R is low at this time the Invalid flip-flop is preset, setting the INHIBIT signal.

Invalid for Early Coincidence is detected by a second flip-flop in A22. With the EARLY/LATE jumper (J2) in the EARLY position, signal GATEB* becomes active. PHABUSY* is the D proposition of the flip-flop and GATEB* is the flip-flop's clock. If PHABUSY* is not low at the trailing (rising) edge of GATEB* the flip-flop is clocked true, which presets the Invalid flip-flop.

The Invalid flip-flop is reset by the next ADCR* (Data Accepted) to the ADC. The REJ flip-flop is reset with 90CLR*.

4.13. Dead Time Display [Sheet 5 and B-27008]

U1 and U2 (Board 2) are integrated circuits that sense analog voltage levels and drive the two 10-segment bar-graphs Z1 and Z2 (Board 2), providing a linear analog display of the ADC dead time. The analog voltage is integrated from the ADC dead-time signal provided from A5a. Resistors R1-R4 set the gain of U1 and U2 so that 100% DT causes all 20 bar-graph segments to be lit.

4.14. Five Volt Power Supply [Sheet 6]

The +5V logic power supply is synthesized by a push-pull switching inverter which operates off the +12 V and –12 V NIM voltages. Q21 and Q22 are operated as saturating switches in a relaxation oscillator through the power transformer. The operating frequency is set by the transformer primary inductance and C95 at about 50 kHz. The feedback winding of the transformer alternates drive between Q21 and Q22 to generate a push-pull voltage to the primary. Rectifiers D19 and D20 convert the push-pull ac to a full-wave output. XFMR-1 in

the +12 V line, driving the center tap of the power transformer, couples an ac waveform to the secondary at the output of the rectifiers in a phase and level which effectively cancels the ripple voltage in the dc output. C96 and C97 are used to integrate the small residual ripple and reduce noise in the logic output.

Q24 and Q25 provide short-circuit protection of the output by sensing the input dc current to the inverter via R155, and switching off the drive to Q21 and Q22 if a fault is detected. Q24 is normally off and Q25 normally on. When an over-current fault is detected, Q24 switches on, and Q25 off. Positive feedback through R159 and C93 latch Q25 off for about one second.

As C93 completely charges to –12 V (with Q25 off), Q24 is again switched off and Q25 on to permit R155 to resample the input current. If a fault persists, Q24 is again switched on and Q25 off to again disable the inverter. This results in a periodic resampling of the load condition, limiting the stress on Q21 and Q22. C98, C94, and the input toroid together prevent generation of any interference back on the ±12 V supplies from the inverter operation.

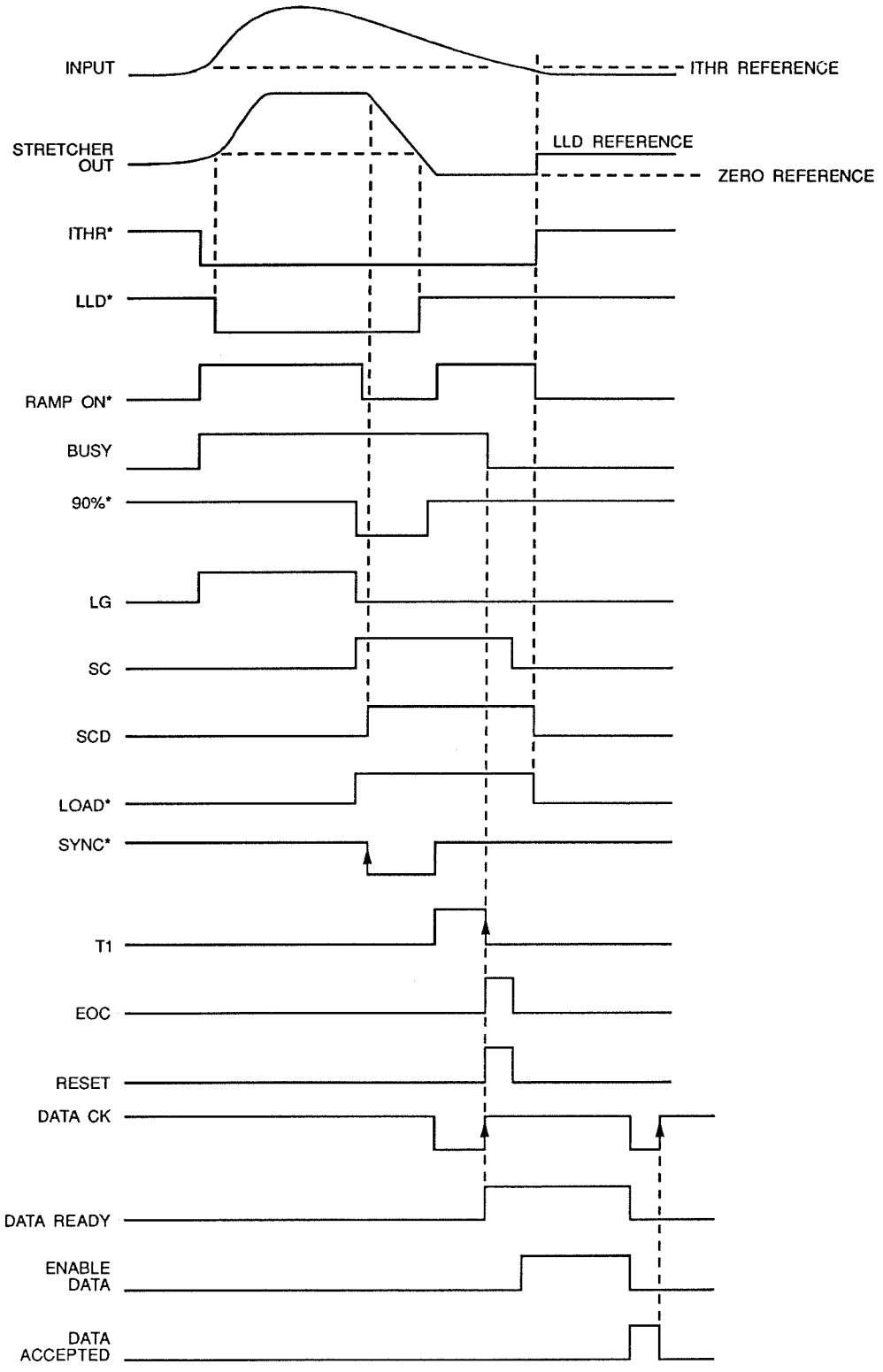


Figure 4.1 Model 8701 Timing Diagram

A. Specifications

A.1. Inputs

ADC IN - Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for the SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 µs maximum; width 0.5 µs minimum; Z_{in} 1 kΩ, direct coupled; front panel BNC.

GATE IN - Accepts a positive logic pulse or dc level; high amplitude ≥+2.5, Low amplitude ≤400 mV, 0 to +7 V maximum; dc coupled; Loading with COINCidence selected is 27 kΩ to +5 V and 27 kΩ to -12 V for ANTIcoincidence; width ≥250 ns; PHA analysis does not require a gate input; minimum gate pulse width for SVA is 1 µs.

DEAD TIME - Rear panel BNC connector which receives an external dead time INPUT. Accepts a negative or positive logic signal, jumper selectable, which is ORed with the ADC dead time; negative true amplitude ≤400 mV, positive true amplitude ≥+2.5 V, 0 to +7 V maximum; loading 4.7 kΩ to +5 V. The composite dead time signal may be accessed through pin 6 of the rear panel DATA connector. Internal jumper plug selects the output composite dead time signal polarity, positive true or negative true; shipped in the NEG position; TTL compatible with 4.7 kΩ to +5 V.

A.2. Outputs

DATA - Provides 13 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 34-pin ribbon cable connector. Data lines are negative true. Two input lines are also provided for the Model 8233 Digital Stabilizer correction voltages. Stabilizer Control range; zero: ±2%, gain: ±5%.

PILEUP REJECTOR/LIVE TIME CORRECTOR - Accepts Reject and Live Time signals from Canberra amplifiers equipped with PUR/LTC. It also provides Linear Gate to those units for full interactive operation; rear panel 3-pin Molex connector for use with Model C1514 PUR/LTC interface cable.

REJect - Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur during the ADC Linear Gate (LG) signal time; amplitude ≥ 2.5, 0 to 7 V maximum; width ≥100 ns; loading 22 kΩ to -12 V. Accessible through pin 2 of the rear panel PUR connector.

LG - Provides a negative true logic signal; logic low while the ADC acquires an input pulse, returns to a logic high at the pulse acquisition conclusion. TTL compatible output, 47 Ω series resistor. Accessible through pin 1 of the rear panel PUR connector. The LG signal may be viewed on the front panel INSPect test point, positive true, series 220 Ω resistor.

A.3. Front Panel Controls

GAIN - Six-position rotary switch to select full scale resolution of the input signal; selection of 256, 512, 1024, 2048, 4096 or 8192 channels for a 10 V input pulse or level.

RANGE - Six-position rotary switch to select 256, 512, 1024, 2048, 4096 or 8192 channels as the upper output address limit.

OFFSET - Six toggle switches to digitally offset the spectrum to the left; subtracts 0 to 8064 channels in binary multiples of 128 channels.

LLD - Screwdriver-adjusted multi-turn potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range 0.02 to +10 V dc.

ULD - Screwdriver-adjusted multi-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range 0.02 to +10.5 V dc.

ZERO - Screwdriver-adjusted multi-turn potentiometer sets the input analog zero level; adjustment range ±5% of the ADC full scale range.

PEAK DETECT - Toggle switch to select either AUTOmatic or DELAYED initiation of conversion cycle. In AUTOmatic an internal constant-fraction trigger operates on the falling edge of the input pulse. In DELAYED mode, the conversion begins after a user selectable delay, initiated by the input signal rising through the LLD setting. An ADJustment potentiometer permits selection of a delay from 2 to 100 µs. An INSPect test point is provided to monitor the Linear Gate time delay adjustment, positive true, series 220 Ω resistor.

COINC/ANTI - Toggle switch to select either the COINCidence or the ANTIcoincidence gating mode. In the COINCidence mode (ANTIcoincidence) a positive GATE pulse enables (disables) the conversion of the present input. If gating is used, the pulse must be present during the Linear Gate time as monitored on the INSPect test point.

PHA/SVA - Toggle switch to select the Pulse Height or Sample Voltage Analysis mode. In PHA, the conversion cycle is initiated by the INPUT pulse. In SVA, the conversion cycle is initiated by a GATE pulse. In either mode, the LLD and ULD acceptance criteria apply. The GATE pulse must be positive in COINC mode or inverted in ANTI mode.

A.4. Indicators

DEAD TIME - 20 segment LED indicator displays the average dead time of the converter.

A.5. Performance

INTEGRAL NONLINEARITY - <±0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY - <±0.7% over the top 99.5% of range including effects from integral nonlinearity.

GAIN DRIFT - <±0.009% of full scale/°C

ZERO DRIFT - <±0.0025% of full scale/°C

LONG TERM DRIFT - <±0.005% of full scale/24 hours at a constant temperature.

PEAK SHIFT - <±0.025 of full scale at rates up to 100 kHz.

ADC DEAD TIME - Linear Gate Time + Conversion Time.

CONVERSION TIME - 1.5 µs +0.01 (N + X) µs where N = address count, and X = effective digital OFFSET.

CHANNEL PROFILE - Typically flat over 90% of channel width.

A.6. Power Requirements

+24 V - 75 mA	+12 V - 150 mA
–24 V - 75 mA	–12 V - 150 mA

A.7. Physical

SIZE - Standard single width NIM module 3.42 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-00457T

NET WEIGHT - 0.9 kg (1.9 lb)

SHIPPING WEIGHT - 1.8 kg (4.0 lb)

A.8. Cables

Cable not supplied; MCA must support 34-pin ADC Standard. Consult factory if required.

B. Rear Panel Connectors

This chapter lists the details of the ADC's rear panel interface and power connectors.

B.1. Data Interface Connnector

This 34-pin ribbon conector (J102) provides all the necessay signals for connection to the MCA. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	CDT* or CDT
7	GND	8	ENC* or ENC
9	GND	10	READY*
11	GND	12	INB* (INV*)
13	Reserved	14	ADC00*
15	ADC07*	16	ADC01*
17	ADC08*	18	ADC02*
19	ADC09*	20	ADC03*
21	ADC10*	22	ADC04*
23	ADC11*	24	ADC05*
25	ADC12*	26	ADC06*
27	Reserved	28	Reserved
29	BF*	30	VGAIN
31	BLLD	32	VZERO
33	BCB*	34	Reserved

Interface Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

SIGNAL	PIN	DESCRIPTION
ADC00*	14	OUTPUT: Binary data 2^0 (LSB)
ADC01*	16	OUTPUT: Binary data 2^1
ADC02*	18	OUTPUT: Binary data 2^2
ADC03*	20	OUTPUT: Binary data 2^3
ADC04*	22	OUTPUT: Binary data 2^4
ADC05*	24	OUTPUT: Binary data 2^5
ADC06*	26	OUTPUT: Binary data 2^6
ADC07*	15	OUTPUT: Binary data 2^7
ADC08*	17	OUTPUT: Binary data 2^8
ADC09*	19	OUTPUT: Binary data 2^9
ADC10*	21	OUTPUT: Binary data 2^{10}
ADC11*	23	OUTPUT: Binary data 2^{11}
ADC12*	25	OUTPUT: Binary data 2^{12} (MSB)
ENDATA*	4	INPUT (Enable Data): Used to enable the tri-state buffers driving the 13-bits of data onto the output lines ADC00* through ADC12*.
READY*	10	OUTPUT (Data Ready): Indicates that data is available for transfer to the MCA. READY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	INPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may reset when READY* resets (handshake).
INB*	12	OUTPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer must be completed, the data itself should be discarded by the MCA.
ENC* or ENC	8	INPUT (Enable Convertor): This signal enables or disables the ADC module. A jumper option (J1) allows selection of polarity. ENC = logic 1 enables ADC operation. ENC = logic 0 prevents the ADC from reopening the linear gate thereby inhibiting further operation.
CDT* or CDT	6	OUTPUT (Composite Dead Time): This signal indicates the time when the ADC or connected amplifier is busy and cannot accept another input event. It is used to gate the live time clock circuit in the MCA. A jumper option (J3) allows selection of polarity.
BF*	29	OUTPUT: This signal is set true at peak detect time and remains true until the leading edge of ACEPT*. This signal is meaningful in the NON-OVERLAP mode only.

BCB*	33	OUTPUT: This signal is set true at peak detect time and remains true until READY* is set true. It represents the conversion time of the internal ADC.
BLLD	31	OUTPUT: This signal is set true when the input pulse rises above the ADC Threshold level and remains true until the trailing edge of ACEPT*.
VZERO (Analog)	32	INPUT: This analog signal controls the ADC zero and it is normally provided by the spectrum stabilizer. The ZERO shift of the ADC is ±2% for a ±5 volt input signal. A more positive level on this signal causes spectral peaks throughout the spectrum to move downward.
VGAIN (Analog)	30	INPUT: This analog signal controls the ADC gain and is normally provided by the spectrum stabilizer. The GAIN shift of the ADC is ±2% for a ±5 volt input signal. A more positive level on this signal causes spectral peaks at the upper end of the spectrum to move downward (lowers the gain).
GND	1,3,5,7,9,11	DC common for all interface signals.

B.2. LTC/PUR Connector

The PUR/LTC 3-pin Molex connector provides the connection to the spectroscopy amplifier for pulse pileup rejection and accurate live time correction.

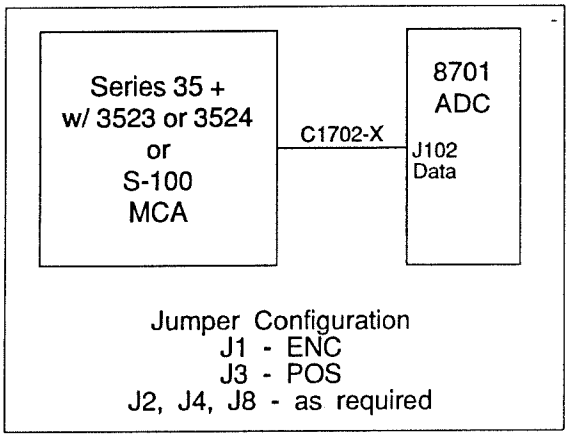
SIGNAL	PIN	DESCRIPTION
LG*	1	OUTPUT: This signal is set true when the input pulse rises above the ADC threshold level and remains true until peak detection. An alternate signal (CB*) which is true during the ADC conversion time is optionally available via internal jumper J5. Used for PUR livetime correction in combination with the amplifier. Logic true = 0 to 0.5 volts; logic false = 3 to 5 volts.
REJ	2	INPUT: A positive level on this signal any time during LG* causes the ADC to reject the event in process. Used for PUR in combination with the amplifier. Logic true = 3 to 5 volts Logic false = 0 to 0.5 volts
GND	3	Signal common.

B.3. Dead Time Connector

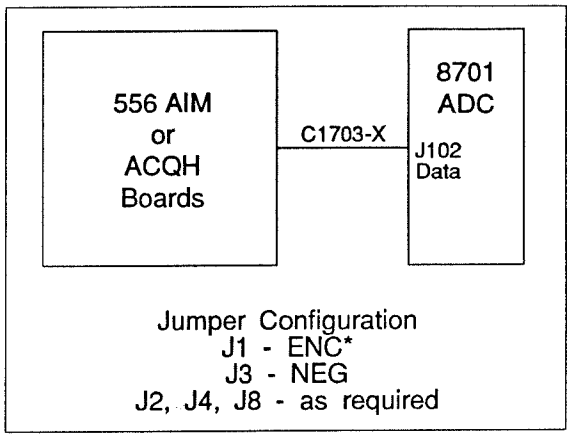
The Dead Time BNC connector accepts a negative or positive true amplifier busy signal, with polarity selectable via jumper J4. This signal is logically ORed with the ADC busy signal to provide proper livetime correction in the MCA via signal CDT* on the MCA interface connector.

C. Setup Diagrams

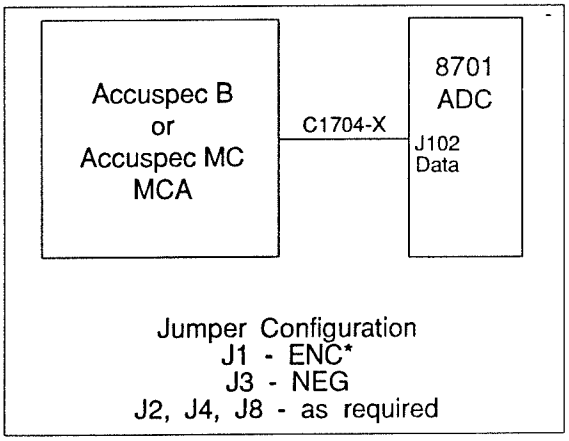
These block diagrams are included to help you set up your system.



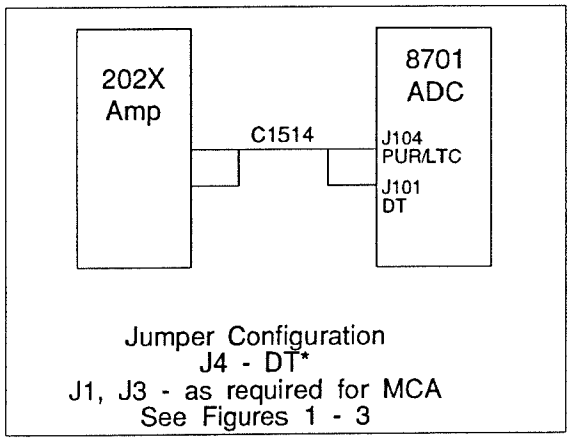
Jumper Configuration
J1 - ENC
J3 - POS
J2, J4, J8 - as required



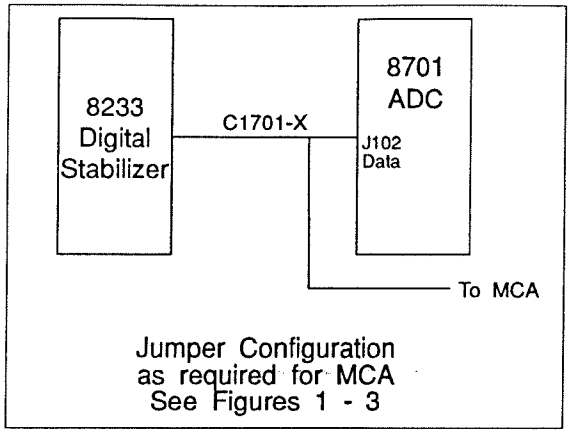
Jumper Configuration
J1 - ENC*
J3 - NEG
J2, J4, J8 - as required



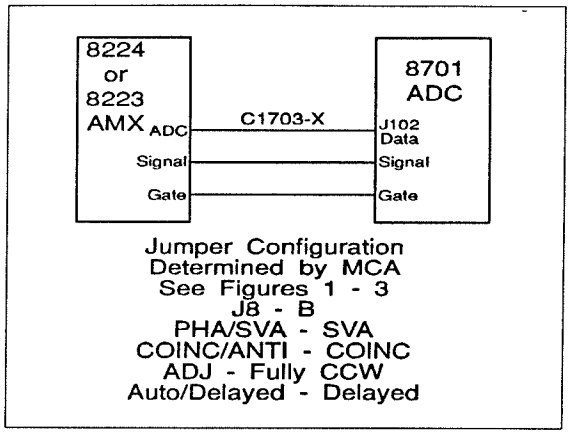
Jumper Configuration
J1 - ENC*
J3 - NEG
J2, J4, J8 - as required



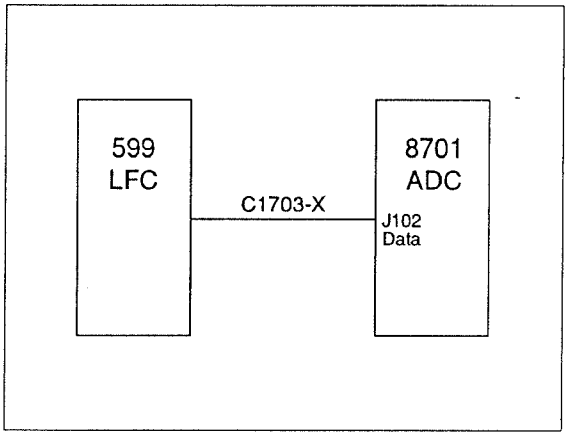
Jumper Configuration
J4 - DT*
J1, J3 - as required for MCA
See Figures 1 - 3

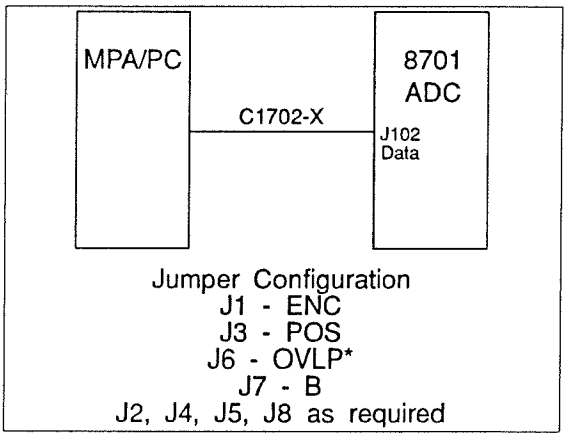


Jumper Configuration
as required for MCA
See Figures 1 - 3



Jumper Configuration
Determined by MCA
See Figures 1 - 3
J8 - B
PHA/SVA - SVA
COINC/ANTI - COINC
ADJ - Fully CCW
Auto/Delayed - Delayed





Jumper Configuration
J1 - ENC
J3 - POS
J6 - OVLP*
J7 - B
J2, J4, J5, J8 as required

D. Environmental Specifications

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- a rack or tabletop enclosure fully closed on all sides with rear door access
- single point external cable access
- blank panels to cover open front panel Bin area
- compliant grounding and safety precautions for any internal power distribution
- the use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance to the specified EU requirements.

Operating Temperature: 0-50 degrees Centigrade
Operating Humidity: 0-80% Relative, Non-condensing
Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution degree 2

Request for Schematics

Schematics for this unit are available directly from Canberra. Write, call or FAX:

Training and Technical Services Department
Canberra Industries
800 Research Parkway, Meriden, CT 06450
Telephone: (800) 255-6370 or (203) 639-2467
FAX: (203) 235-1347

If you would like a set of schematics for this unit, please provide us with the following information.

Your Name _____

Your Address _____

_____

_____

_____

_____

Unit's model number _____

Unit's serial number _____

Note: Schematics are provided for information only; if you service or repair or try to service or repair this unit without Canberra's written permission you may void your warranty.

Warranty

This warranty covers Canberra hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Equipment manufactured by Canberra is warranted against defects in materials and workmanship for one year from the date of shipment.

Canberra warrants proper operation of its software only when used with software and hardware supplied by Canberra and warrants software media to be free from defects for 90 days from the date of shipment.

If defects are discovered within 90 days of the time you receive your order, Canberra will pay transportation costs. After the first 90 days, you will have to pay the transportation costs.

LIMITATIONS

Upon notification of defects in the software media or hardware, Canberra will repair or replace the defective items at its discretion.

THIS IS THE ONLY WARRANTY PROVIDED BY CANBERRA; THERE ARE NO OTHER WARRANTIES, EXPRESSED OR IMPLIED. ALL WARRANTIES OF MERCHANTABILITY AND FITNESS FOR AN INTENDED PURPOSE ARE EXCLUDED. CANBERRA SHALL HAVE NO LIABILITY FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES CAUSED BY FAILURE OF ANY EQUIPMENT OR SOFTWARE MANUFACTURED BY CANBERRA.

EXCLUSIONS

This warranty does not cover equipment which has been modified without Canberra's written permission or which has been subjected to unusual physical or electrical stress as determined by Canberra's Service Personnel.

Canberra is under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage due to neutrons or heavy charged particles or from physical abuse. Failure of beryllium, carbon composite, or polymer windows or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

Canberra is not responsible for damage sustained in transit. Examine shipments carefully when you receive them for evidence of damage caused in transit. If damage is found, notify Canberra and the carrier immediately. Keep all packages, materials and documents, including your freight bill, invoice and packing list.

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