Instruction Manual

TIMING SINGLE CHANNEL ANALYZER
MODEL 835

Canberra 800 Series of
Modular Nuclear Instruments

PHYS. 247

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1.0 GENERAL

1.1 Description

The Canberra Industries Model 835 Timing SCA combines in one module the two functions of single channel pulse height (energy) analysis and pulse crossover or leading edge (timing) discrimination.

If the energy restrictions established by the front panel baseline and window width controls are met, the timing portion of the Model 835 generates an output (or logic) signal when a bipolar input signal crosses the zero voltage baseline, or at the leading edge of a unipolar input signal. Leading edge timing may also be used for bipolar input signals by selecting the Unipolar operating mode.

By means of front panel switch selection, the Model 835 may therefore be used as a single channel analyzer, a leading edge timing discriminator, a zero crossing discriminator, or as both a timing unit and pulse height analyzer simultaneously.

In all operating modes, the logic output may be delayed up to 300 nanoseconds by front panel control.

1.2 Applications

Because of its inherent design flexibility, the Model 835 Timing SCA is useful in a wide variety of nuclear applications where accurate energy analysis or precise leading edge or zero crossing timing is required. The Model 835 may be used with the outputs from double delay line shaping, RC shaping, or multimode amplifiers whose outputs range from 0 to +10 volts.

When used as a regular SCA, the Model 835 permits energy analysis to be performed on detected nuclear events. It also permits nuclear counting to be limited to events in a specific energy range, as well as providing a means of reducing incoming data so that further processing and analysis is performed only on selected events.

The timing capabilities of the Model 835 may be used for fast coincidence evaluation from the leading edge or the crossover point of input pulses. The zero crossing mode of operation is typically used with scintillation detectors or small semiconductor detectors, generally with double delay line shaping amplifiers. The leading edge crossing capability is typically used with large semiconductor detectors having long charge collection times, typically with RC shaping main amplifiers.

In all modes of timing operation, the input pulses must meet the established energy requirements in order to enable the timing output signal. Thus, fast/slow coincidence experiments may be performed without the need for an additional slow coincidence module.

2.0 SPECIFICATIONS

2.1 Performance

Baseline Linearity: better than 0.5% of full scale

Window Width Linearity: better than 0.5% of full scale (with optional ten-turn potentiometer)

Baseline Stability: better than 0.1% of full scale over 24 hours

Window Width Stability: better than 0.1% of full scale over 24 hours

Delay Stability: better than ± 1 nanosecond/°C

Crossover Walk: for double delay line shaped signals with rise time less than 400 nanoseconds, less than 5 nanoseconds over a 0.5 to 10 volt input signal range

Leading Edge Walk: for double delay line shaped signals with rise time less than 125 nanoseconds, less than 25 nanoseconds over 1.0 to 10 volt input signal range, less than 35 nanoseconds over 0.5 to 10 volt input signal range

2.2 Controls, Inputs, Outputs

2.2.1 Controls

Baseline: ten-turn potentiometer to establish minimum energy for input signal; 0.25 to 10 volts

Window Width: single-turn potentiometer to establish range above baseline setting for input signal; 0 to 10 volts (ten-turn control optional for $25.)

Variable Delay: single-turn potentiometer; 0 to 300 nanoseconds (ten-turn control optional for $25.)

Fixed Delay: 0 or 300 nanoseconds via front panel toggle switch

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Input Mode: unipolar or bipolar via front panel
toggle switch

2.2.2 Input

Input: positive unipolar or bipolar 0.25 to 10
volt pulses, rise time less than 10 microseconds,
width greater than 75 nanoseconds; input impedance
greater than 1000 ohms

2.2.3 Output

Output: positive 10 volts, 1 microsecond wide, rise
time less than 50 nanoseconds; output impedance less
than 100 ohms

3.0 NITIAL OPERATION

3.1 Setup

Insert module in AEC compatible base unit/power supply such
as Canberra Model 800; turn on power switch

Connect output from pulse shaping amplifier such as Canberra
Model 810 to input connector of module; using a "tee" connector,
simultaneously observe amplifier output on oscilloscope (2v/cm,
1 usec/cm), or observe amplitude on multichannel analyzer

. Set baseline potentiometer to 5.00

Set window width potentiometer to .0

. Set variable delay potentiometer to 0

. Set fixed delay switch to 0

. Set input mode switch to UNI(polar)

. Connect output of module to second input on oscilloscope
(5v/cm, 1 usec/cm), or to scaler

3.2 Initial Checkout

. Increase amplifier signal slowly until Model 835 output is just observed;
increase amplitude until output is fully on; imput pulse amplitude at
half-maximum output should be 5.00 ±0.10. Range between full OFF
and full ON is a measure of amplifier peak to peak noise; check this
range by increasing Baseline setting until Model 835 output disappears
and decreasing until output is fully ON

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• Measure amplifier amplitude visually on oscilloscope or on calibrated multichannel analyzer and compare with the Baseline readings observed previously - amplifier amplitude at half-maximum SCA output should be 5.00 to $\pm$0.10 - return Baseline setting to 5.00

Increase amplifier output until Model 835 output begins to disappear; repeat tests of previous step by varying Window Width control settings and verify setting is accurate at 1.0 - return Window Width setting to 1.0 and Baseline to 5.00

Vary Baseline and Window Width settings and repeat Steps 1, 2, and 3; a plot of input amplitude versus Baseline (or Window Width) settings will give the linearity curves, which should be within $\pm$0.5% of full scale; or $\pm$50mv; if a detailed check of this specification is contemplated, correspond with the factory for aid

Rotate Variable Delay from 0 to 200; observe 200 nanosecond delay range on oscilloscope

Switch fixed delay to "300" setting; note 300 nanosecond delay in output. This control introduces a fixed 300 nsec delay regardless of the variable delay control.

Change input to bipolar signal; by switching Input mode between UNI(polar) and BI(polar), notice on oscilloscope the shift in output pulse when the 835 acts as a leading edge discriminator (UNI mode) and a zero crossover discriminator (BI mode)

4.0 MODULE OPERATION

4.1 Control Functions

• Baseline: a front panel ten-turn potentiometer used to establish the energy level which the input signals must exceed before a logic output will be generated. This potentiometer may be set from 250 millivolts to 10 volts

• Window Width: a front panel single-turn potentiometer (ten-turn control optional) which establishes the energy range above the baseline within which the input signal must fall to permit the 835 to generate an output pulse. This potentiometer may be set from 0 to 10 volts

• Variable Delay: a front panel single-turn potentiometer (ten-turn control optional) used to select the time (from 0 to 300 nanoseconds) by which the logic output will be delayed after the nominal leading

edge triggering or crossover point of the input pulse. This control is typically used to adjust for cabling and circuitry delays among fast coincidence analysis channels.

Fixed Delay: a front panel toggle switch which introduces a fixed 300 nanosecond delay in the output regardless of the variable delay control setting

Input Mode: a front panel toggle switch permitting operation of the 835 as either a leading edge discriminator when in the UNI position, or as a zero crossing discriminator when in the BI position. Bipolar signals may be used for either input mode; unipolar input signals require that the unit be operated in the UNI(polar) input mode

4.2 Input Requirements

Signal: positive unipolar or bipolar pulses 0.25 to 10 volts in amplitude, rise time less than 10 microseconds, width greater than 75 nanoseconds; input impedance greater than 1000 ohms; BNC connector

Output Specifications

Signal: positive 10 volt logic pulse, 1 microsecond wide, rise time less than 50 nanoseconds; output impedance less than 100 ohms; BNC connector