# Model 8233
# Digital Stabilizer

## User's Manual

9231709A

ISO 9001
SYSTEM
CERTIFIED

CE

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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

Printed in the United States of America.

# Table of Contents

# 1. Introduction

The Model 8233 maintains the stability of high resolution spectroscopy systems in nuclear applications involving long count times or high count rates. It accomplishes this by correcting the conversion gain and/or the zero intercept of a binary analog-to-digital converter (ADC). It can be used to correct for both conversion gain and zero intercept drift simultaneously if required.

The 8233 detects the drift of all system components up to and including the ADC by monitoring the digital output of the ADC. Consequently all system drift can be compensated for by applying a correction to the ADC only.

The 8233 remains passive unless drift correction is required, unlike other digital stabilizers that alternately add or subtract counts in a correction register, even when drift does not occur. Because of this, the 8233 produces less peak broadening and better overall resolution.

Operation of the Model 8233 is the same for either the gain or zero intercept correction, except for the relative location of the reference channel. In either case the user selects a reference channel and a "window", centered on the reference channel. This channel is used by the stabilizer to monitor and correct for drift.

A high end spectral channel is selected for gain stabilization, since gain drift is more pronounced in the upper channels. A low end channel reference is selected for zero intercept stabilization to prevent interference from the effects of gain drift. In either case the analog output range can be adjusted to compensate for expected or encountered drift in the system.

The 8233's front panel bar graph indicates the magnitude and direction of the system's zero or gain drift, as well as an approximation of the correction rate. A second display shows a digital value for the correction rate, the window width, the peak channel, or the analog range setting. The rear panel provides analog recorder outputs that allow the user to monitor system drifts over extended periods of time.

# 2. Controls and Connectors

This is a brief description of the 8233's front panel controls and connectors. For more detailed information, refer to Appendix A, Specifications.

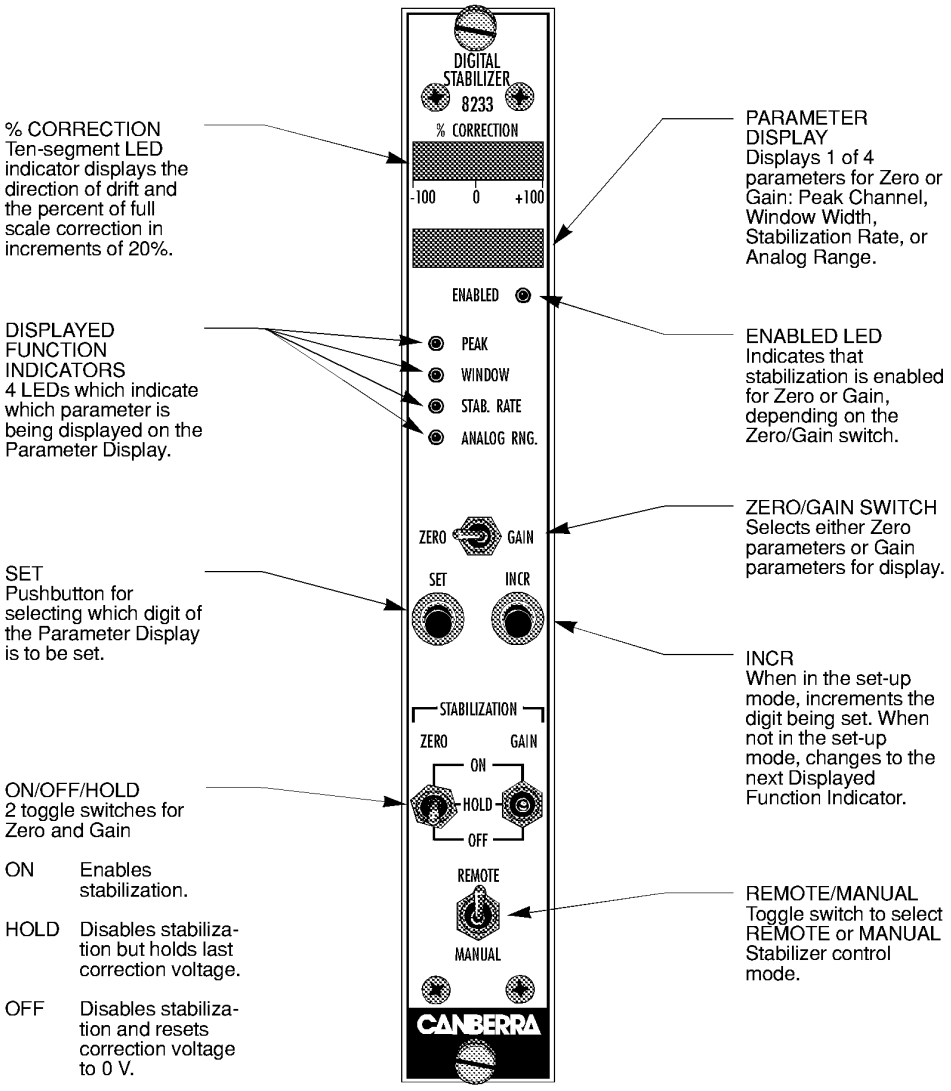



Figure 2.1 Front Panel Controls

This is a brief description of the 8233's rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

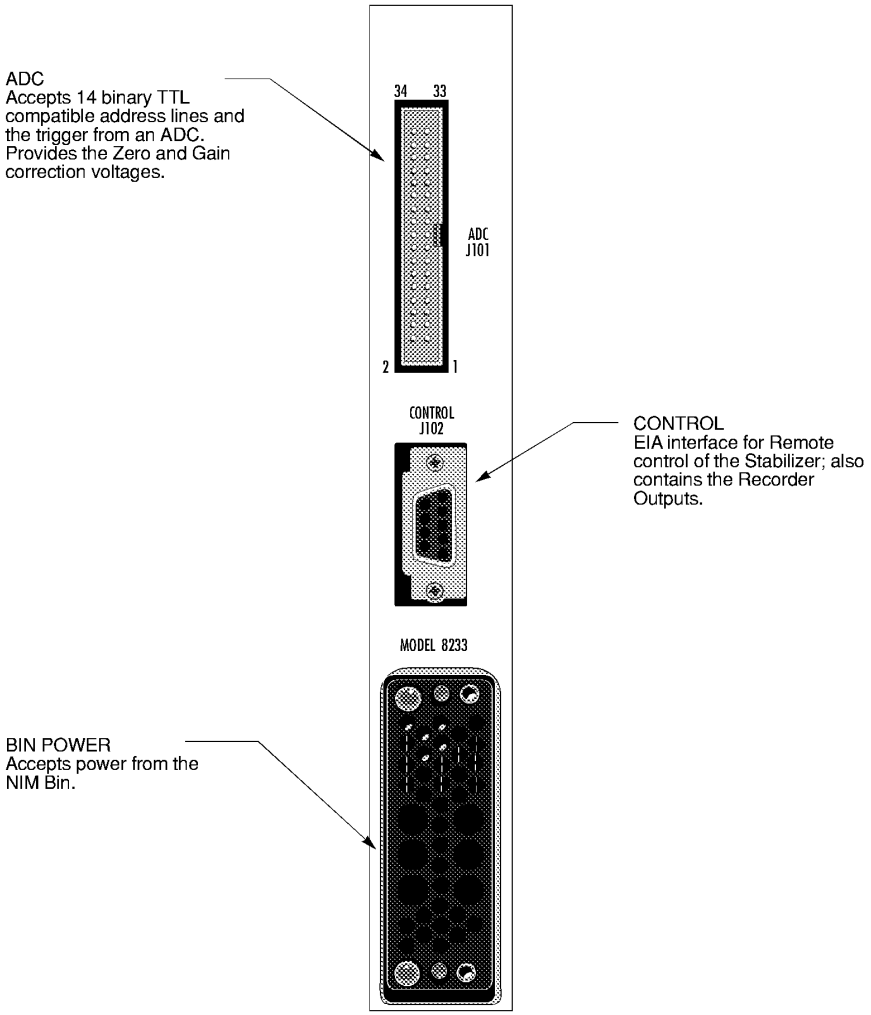
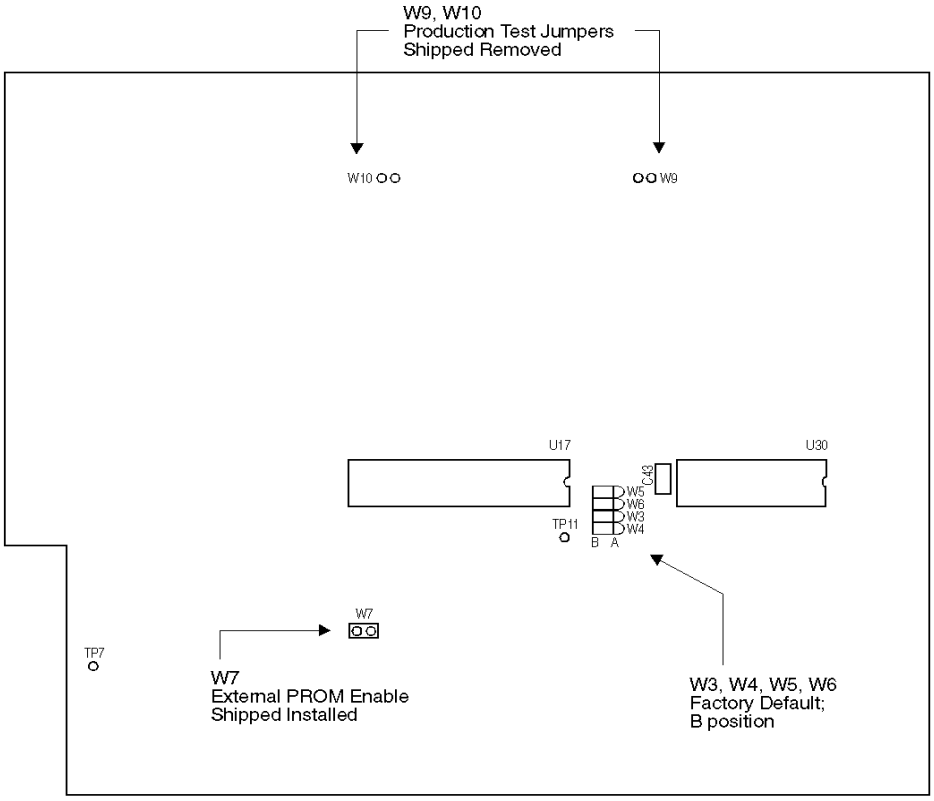



Figure 2.2 Rear Panel Connectors

The internal jumper plug controls should be set for your specific requirements before applying power to the module.




PARITY

| FUNCTION | W3 | W4 |
|---|---|---|
| OFF | — | B |
| ODD | B | A |
| EVEN | A | A |

BAUD

| RATE | W5 | W6 |
|---|---|---|
| 300 | B | B |
| 1200 | B | A |
| 2400 | A | B |
| 9600 | A | A |

Figure 2.3 Internal Controls

# 3. Manual Operation

When the 8233 is turned on, the Peak Channel, Window Width, and Analog Range parameters are loaded from non-volatile memory into working memory. Once they are in working memory, these parameters can be modified with the front panel controls, as described in this section.

The parameters in non-volatile memory can be modified as described in "Parameter Setup" on page 8.

## 3.1 Correction

The % CORRECTION indicator, a zero center, ten-segment LED bar graph, shows the direction and percent of full scale correction being applied, in increments of twenty percent. Either Zero or Gain correction can be seen, depending on the position of the ZERO/GAIN switch.

## 3.2 Parameter Display

Displays one of four parameters for Zero or Gain, depending on the position of the ZERO/GAIN switch. One of the four Displayed Function indicators will show which parameter is being displayed: Peak, Window, Stabilizer Rate, or Analog Range. The desired parameter is selected using the INCRement pushbutton when not in the set-up mode.

### Peak

The Peak parameter shows the PEAK channel which the Stabilizer is correcting on. Valid settings range from 0 to 16 383 in steps of 1 channel.

Note that the 8233 Stabilizer uses channel 0 as the first memory address. For MCA systems which use channel 1 as the first memory address, such as the AccuSpec or Genie-PC, the 8233 peak channel should be set to a value of one less than the desired channel. For example, if the desired PEAK channel is 4096, then the 8223 should be set for 4095.

### Window

The Window parameter shows the number of channels used by the Stabilizer as its sampling range. The Window is centered about the Peak channel, but not allowed to wrap around 0 or 16 383. Valid settings for the Window are 1 to 999 channels in odd valued increments of 2.

### Stab. Rate

The Stabilization Rate parameter shows the count rate of the input data which will change the correction voltage. This display is in counts per second (CPS). Input data which causes a change in the correction voltage are the data which fall inside the Window but are not equal to the Peak channel.

### Analog Rng.

The Analog Range parameter shows the value of the Analog Attenuation Factor. The attenuation is applied to the ±5 V range of the correction voltage from the Stabilizer to the

ADC. For example, if the attenuation factor is set to 0.5, the range of the correction voltage is ±2.5 V.

The attenuation factor is useful when the expected system drift does not require the full range of correction and a smoother correction is desired. This smoother correction will lessen the stabilizer's peak-broadening effect. The attenuation factor does not affect the Recorder Outputs. The settings for Analog Range are 1.0, 0.5, 0.25, or 0.125.

## 3.3 Enabled

The ENABLED indicator is illuminated when stabilization is ON. The ZERO/GAIN switch selects display of ZERO enabled or GAIN enabled. Stabilization can be enabled manually with the front panel switches or remotely by the serial port.

## 3.4 Zero/Gain

The ZERO/GAIN switch selects either Zero or Gain parameters and status for the Parameter Display. Stabilization can be activated for Zero or Gain regardless of the position of the ZERO/GAIN switch.

## 3.5 Set

The SET pushbutton enables the Setup mode and selects the digit of the displayed parameter to be set. Pressing the SET button will start the least significant digit of the display blinking. If Analog Range is displayed, all digits will start blinking.

Each succeeding button press will change the blinking digit to the next significant digit. When the most significant digit is blinking, pressing the SET pushbutton will exit the setup mode and store the parameters in nonvolatile memory.

## 3.6 Increment

The Increment pushbutton has two functions. In the Setup mode, pressing INCR will increment the value of the digit being set (blinking). When not in the setup mode, pressing INCR will increment the Displayed Function Indicators and the Parameter Display to the next function.

## 3.7 Stabilization Control Switches

These two three-position switches control Zero and Gain Stabilization.

In the OFF position, stabilization is disabled and the correction voltage is held to zero volts.

In the ON position, stabilization is enabled: the Stabilizer will compare the incoming data to the Peak setting and the window limits and add one step to or subtract one step from the correction voltage, depending on whether the incoming data was above or below the Peak Channel.

In the HOLD position, stabilization is disabled, but the correction voltage is maintained at the output.

## 3.8 Remote/Manual Mode Switch

When this switch is set to Remote, serial port control is enabled and the front panel Set and Stabilization Control switches are disabled. With the switch in Manual, the serial port is disabled and the Set and Stabilization Control switches are enabled.

Remote control allows you to use a series of Escape Sequences, defined in Appendix C, to set parameters, duplicate the function of the Stabilization Control switches, and read out the Stabilizer parameters or status.

## 3.9 Preventative Maintenance

Preventative maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap, side or rear panels.

# 4. Remote Operation

When the front panel Remote/Manual switch is in the Remote position, the rear panel Control connector (J101), a serial port, receives and transmits remote control signals using EIA RS-232C standard signal levels. A DTR line is also provided which shows that the 8233 is in Remote and ready to accept data.

The data format is: one start bit, 8 data bits, parity bit if enabled, and one stop bit. Baud rates are 300, 1200, 2400, or 9600. Parity and baud are selected by internal jumpers, shown in Figure 2.3.

## 4.1 Parameter Setup

Using the escape sequences defined in Appendix C, Peak Channel, Window Width, and Analog Range can be modified for both Gain and Zero.

After the parameters are entered, an escape sequence can store them in nonvolatile memory. If this is not done, the previous parameter settings remain in the nonvolatile memory, and the parameters just entered will be used only until the power is turned off.

## 4.2 Commanded Reports

Gain or Zero Setup Parameters and Gain, Zero, and Unit Status can be read out through the Control connector.

Note: If a readout is in process, further report requests will be ignored.

### Setup Parameters

The Gain and Zero Setup Parameters (Peak Channel, Window Width, and Analog Range), can be read from the 8233. The Setup Parameter report formats are defined in Appendix C.9 and C.11.

### Status

The Gain or Zero Status can be read from the 8233. The Status consists of the position of the two Stabilization Control switches (On/Off/Hold), Present Correction, and Stabilization Rate. The Status report formats are defined in Appendix C.10 and C.12.

### Unit Status

The Unit Status, which is an error code indicating a fault in an escape sequence received by the 8233, can be read from the unit. The Unit Status format and error codes are listed in Appendix C.13.

## 4.3 Stabilization Control

The Stabilization Control status can be set through the serial port. One of three modes, On, Hold, or Off, can be enabled for both Gain and Zero using an Escape Sequence. These Escape Sequences are listed in Appendix C.7 and C.8.

# 5. Theory of Operation

## 5.1 Hardware

The Model 8233's hardware is based on the Intel 8031 microcontroller, which is the ROMless version of the 8051. The program code for the 8031 is contained entirely in one 27C64 PROM. The program RAM is internal to the 8031. The setup parameters are stored in the external non-volatile RAM (NVRAM).

A conversion address is latched into the ADC Interface by the ADC. This storage also generates an interrupt in the 8031. The 8031 services this interrupt by reading the address from the ADC Interface and comparing that address to the Peak and Window settings for Zero and Gain, if they are enabled. If the address falls in one of the Windows and is not equal to the Peak Channel, the Zero or Gain Correction DAC is appropriately adjusted. Each conversion which is above the peak and below the upper limit of the Window subtracts one from the value stored in the DAC. A conversion below the Peak Channel adds one to the present value stored in the Correction DAC. The output of the Correction DAC is used as the reference voltage for the Attenuation DAC.

An 8253 Programmable Interval Timer, U24, is used to divide the incoming count rate by N. The value of N is set to keep the interrupt rate to the microcontroller below 6 kHz.

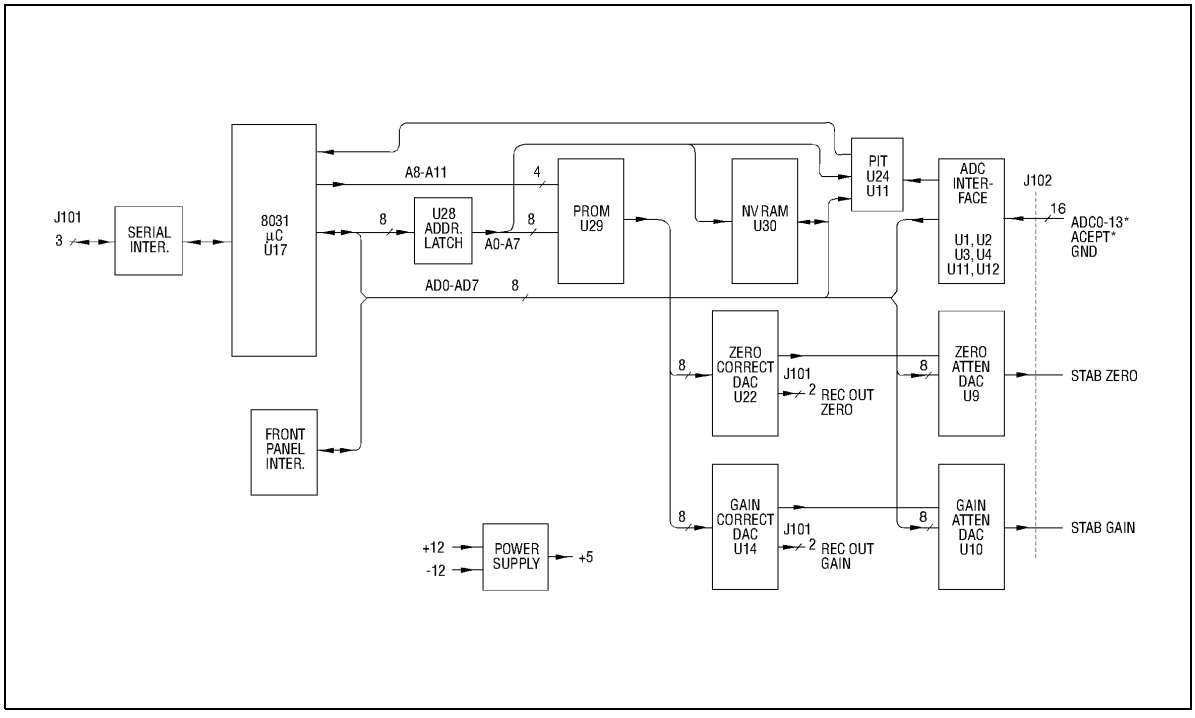



Figure 5.1 Model 8233 Hardware Block Diagram

The output from the Attenuation DACs is connected to the ADC. An increase or decrease in this correction voltage will result in an increase or decrease in the ADC's zero or gain setting. The Analog Range setting is passed to the Attenuation DACs. Therefore, the Correction DAC Output is multiplied by the Attenuation Factor. An Attenuation Factor of 1 results in a code of $FF_H$ being loaded into the Attenuation DAC. The code for 0.5 is $7F_H$, for 0.25 it is $3F_H$, and for 0.125 is $1F_H$.

The front panel interface consists of the switch buffer and the display controller. The switch buffer, which consists of U25, U26, U32 and U33, is periodically read by the firmware. The display controller U27, controls the bar graph, the 5-digit parameter display and the Displayed Function LEDs. The display controller generates the scan rate and the seven-segment code for the 5-digit display. The only requirement of the firmware is to load the proper binary code and digit address for the character to be displayed.

The major portion of the serial interface is internal to the 8031. The UART and the Baud Rate generator are both integral parts of the 8031. The only external parts required are EIA-to-TTL-level translators, U5 and U16.

## 5.2 Five Volt Power Supply

The +5 V logic power supply is synthesized by a push-pull switching inverter which operates off the +12 V and –12 V NIM voltages. Q1 and Q2 are operated as saturating switches in a relaxation oscillator through the power transformer. The operating frequency is set by the transformer primary inductance and C23 at about 70 kHz. The feedback winding of the transformer alternates drive between Q1 and Q2 to generate a push-pull voltage to the primary. Rectifiers D9 and D10 convert the ac to a full-wave output. XFMR-1 in the +12 V line, driving the center tap of the power transformer, couples an ac waveform to the secondary at the output of the rectifiers in a phase and at a level which effectively cancels the ripple voltage in the dc output. C28 and C29 are used to integrate the small residual ripple and reduce noise in the logic output.

Q3 and Q4 provide short-circuit protection of the output by sensing the inverter's input dc current via R42 and switching off the drive to Q1 and Q2 if a fault is detected. Q4 is normally off and Q3 normally on. When an over-current fault is detected, Q4 switches on and Q3 off. Positive feedback through R40 and C19 latch Q3 off for about one second. As C19 completely charges to –12 V (with Q3 off), Q4 is again switched off and Q3 on to permit R42 to resample the input current. If a fault persists, Q4 is again switched on and Q3 off to again disable the inverter. This results in a periodic resampling of the load condition, limiting the stress on Q1 and Q2. C24, C27, and the input toroid together prevent generation of any interference back on the ±12 V supplies from the inverter operation.

## 5.3 Firmware

The Idle Loop, which updates the bar graph, the 5-digit display, and the Displayed Function LEDs as well as reading the present position of the front panel switches, is the main part of the firmware. The Idle Loop also services the serial buffer when it contains a command received from an external EIA device.

All of the other routines are entered because of internal or external interrupts. The ADC Interrupt Service Routine starts its processing by reading the conversion address from the

ADC interface logic. This read is performed as two bytes: the low byte first then the high byte. Reading the high byte also clears the interrupt and allows the ADC interface logic to accept another input from the ADC.

The ADC Interrupt Service Routine then compares the conversion address to the gain and zero window limits and to the gain and zero peak channels. If the address falls within one of the windows and is not equal to the peak channel, the routine will cause a change in the correction output. The final function performed by the ADC Interrupt Service Routine is to update the appropriate Stabilization Rate Register.

Pushing either the SET or INCR front panel pushbutton will generate an interrupt and cause the processor to enter the Push Button Interrupt Service Routine. This routine first determines which button has been pressed by reading the switch interface. If the SET pushbutton has caused the interrupt, the Push Button Interrupt Service Routine will increment an internal register used to show which digit is being set. If it was the INCR pushbutton that caused the interrupt, the Push Button Interrupt Service Routine will increment the digit being set if the Set Mode is enabled or increment the Displayed Function LEDs register if the Set Mode is not enabled.

The first step of the Serial Interrupt Service Routine is to determine if the interrupt is a receiver or transmitter interrupt. The receiver interrupt has priority over the transmitter interrupt. If a receiver interrupt is received, the Serial Interrupt Service Routine moves the character from the internal UART to the Receiver Buffer, testing each character to determine if it is a terminator. When a terminator is encountered, a flag is set indicating the buffer contains a complete command the Idle Loop services that flag.

If a transmitter interrupt is received, the Serial Interrupt Service Routine moves a character from the transmitter buffer to the internal UART for transmission. This process continues until the transmitter buffer is emptied or the transmission process is aborted by an escape sequence.

# A. Specifications

## A.1 Inputs

ADC - Binary maximum of 14 bits, parallel access; compatible with the Canberra 8700 series External ADC Interface.

## A.2 Outputs

CORRECTION SIGNAL - Resolution 1 part in 4096; stability: closed-loop self-correcting; output voltage range ±5 V with selectable attenuation factors; one each for Gain and Zero; $Z_{out}$=1 kΩ.

RECORDER OUTPUT - Resolution 1 part in 4096; stability ≤0.01%/°C; range ±5 V; one each for Gain and Zero; $Z_{out}$ 1 kΩ.

## A.3 Displays

LED Bar Graph - Displays % Correction for either Gain or Zero.

LED Display - Displays Peak Channel, Window Width, Correction Rate or Analog Range for either Zero or Gain; selection is made with front panel controls.

## A.4 Controls

Zero/Gain - Toggles display between Zero and Gain parameters.

SET - Pushbutton initiates the setup mode and then selects the digit of the parameter to be set.

INCR - Pushbutton increments display through Peak, Window, Stabilization Rate, and Analog Range parameters and, in setup mode, increments the selected digit.

ON/HOLD/OFF - Toggle switch: ON enables stabilization; HOLD disables stabilization but retains last correction voltage; OFF disables stabilization and resets correction voltage to zero.

LOC/REM - Toggle switch: LOCal enables front panel controls; REMote enables EIA Control connector and disables front panel.

## A.5 Connectors

ADC - 34-pin rectangular ribbon connector; rear panel; pin-out compatible with Canberra 8700 and 9600 series ADC connector.

CONTROL - 9-pin female D-type; connects 8233 to an EIA device. Baud rate is selectable from 300 to 9600. Controls setup parameters and stabilization enable/disable. Readout of setup parameters and other display information is provided. Rear panel mounted.

## A.6 Cables

CABLE - A 34-pin 60 cm (2 ft.) ribbon cable (C1701-2) is supplied with the 8233 for use with Canberra 8700 and 9600 series ADCs. Consult the factory for other cable lengths.

## A.7 Power Requirements

+12 V dc - 160 mA –12 V dc - 160 mA

## A.8 Physical

SIZE - Standard single width NIM module 3.43 x 22.12 cm, (1.35 x 8.71 in.) per DOE/ER-00457T.

NET WEIGHT - 0.9 kg (1.9 lb).

SHIPPING WEIGHT - 1.8 kg (4.0 lb).

# B. Connector Signals

NOTE: Negative true signals are shown with an asterisk (SA2$^{0}$*).

## B.1 J101 ADC

| Pin | Signal | Description |
|---|---|---|
| 14 | ADC00* | |
| 16 | ADC01* | |
| 18 | ADC02* | |
| 20 | ADC03* | |
| 22 | ADC04* | |
| 24 | ADC05* | Binary Address data. Negative true logic. |
| 26 | ADC06* | Input from an external device. |
| 15 | ADC07* | |
| 17 | ADC08* | |
| 19 | ADC09* | |
| 21 | ADC10* | |
| 23 | ADC11* | |
| 25 | ADC12* | |
| 13 | ADC13* | |
| 30 | VGAIN | Gain Correction Voltage. |
| 32 | VZERO | Zero Correction Voltage. |
| 2 | ACEPT* | Pulse from external device; indicates valid address present. |
| 1,3,5,7,9,1 | GND | Ground. |

## B.2 J102 Control

| Pin | Signal | Description |
|---|---|---|
| 2 | GND | Ground for Gain Recorder Output. |
| 3 | REC OUT GAIN | Gain Recorder Output. |
| 4 | GND | Ground for Zero Recorder Output. |
| 5 | REC OUT ZERO | Zero Recorder Output. |
| 6 | DATA IN | Serial Data Input to 8233. |
| 7 | GND | Ground for Serial Port. |
| 8 | DATA OUT | Serial data transmitted from 8233. |
| 9 | DTR | Data Terminal Ready; indicates 8233 ready to accept serial transmission. |

# C. Remote Control Escape Sequences

## C.1 Set Gain Peak Channel

**ESC Pn@**

Pn is the decimal Peak value expressed as a 1 to 5 character ASCII string.

## C.2 Set Gain Window Width

**ESC PnA**

Pn is the decimal window value expressed as a 1 to 3 character ASCII string.

## C.3 Set Gain Analog Range

**ESC Ps B**

Ps is a selective parameter expressed as an ASCII character, where:

0=Full, 1.0
1=Half, 0.5
2=Quarter, 0.25
3=Eighth, 0.125

## C.4 Set Zero Peak Channel

**ESC Pn C**

Pn is the decimal peak value expressed as a 1 to 5 character ASCII string.

## C.5 Set Zero Window Width

**ESC Pn D**

Pn is the decimal window value expressed as a 1 to 3 character ASCII string.

## C.6 Set Zero Analog Range

**ESC Ps E**

Ps is a selective parameter expressed as an ASCII character, where:

0=Full, 1.0
1=Half, 0.5
2=Quarter, 0.25
3=Eighth, 0.125

## C.7 Gain Stabilization On/Hold/Off

**ESC Ps F**

Ps is a selective parameter expressed as an ASCII character, where:

0=Off
1=Hold
2=On

## C.8 Zero Stabilization On/Hold/Off

**ESC Ps G**

Ps is a selective parameter expressed as an ASCII character, where:

0=Off
1=Hold
2=On

## C.9 Report Gain Setup

**ESC H**

Initiates the report (response from 8233).

**Report Format**

ESC Pp; Pw; Pr H

Where:

Pp = 5 digits, decimal value of the Peak
Pw = 3 digits, decimal value of the Window Width
Pr = 1 digit, Analog Range; format the same as Ps for Set Analog Range

## C.10 Report Gain Status

**ESC I**

Initiates the report (response from 8233).

**Report Format**

ESC Po; Pr; Pc I

Where:

Po = On/Hold/Off, format the same as Ps for Set Gain Stabilization
Pr = 5 digits, which indicate the Stabilization Rate
Pc = 3 digits, Percent Correction

## C.11 Report Zero Setup

**ESC J**

Initiates the report (response from 8233).

Report format is the same as the format for Gain Status except J is the terminator.

## C.12 Report Zero Status

**ESC K**

Initiates the report (response from 8233).

Report format is the same as the format for Gain Status except K is the terminator.

## C.13 Report Unit Status

**ESC L**

Initiates the report (response from 8233).

**Report Format**

ESC Pe L

where Pe is an error code, where:

0=no error
1=number of characters received exceeded the number allowed for the parameters of the escape sequence; spaces are ignored
2=Parameter not an ASCII 0-9
3=Invalid terminator received
4=Data received not preceded by an ESC
5=Value of Ps exceeded 3 for Analog Range setup or 2 for Stabilization On/Hold/Off
6=Number of P's not consistent with terminator

## C.14 Store Parameters

**ESC M**

This command copies the setup parameters from the internal RAM to the non-volatile memory.

## C.15 Terminate Report

**ESC N**

Terminates any report in progress

# D. Self Tests

The 8233 is equipped with diagnostics which can verify its operation.

Sections D.1 through D.7 describe the seven tests. Section D.8 details the test procedure.

## D.1 Test 1 NVRAM

Test 1 checks the non-volatile RAM, U30. The first part of the test writes the address into the RAM and then reads it back. If this test passes, it continues to the next step. If it fails, it displays a 0 and jumps to Test 2.

The second part of the test performs a store cycle on the NVRAM, which places what's in RAM into internal EEPROM, clears the RAM, recalls the data from the EEPROM and then checks for the correct pattern. If this part passes, a P is displayed and Test 2 is started. If this part fails, a 1 is displayed before starting Test 2.

## D.2 Test 2 Serial Port

Test 2 checks the serial port internal to the 8031 and the EIA driver and receiver. The 8031 transmits a $55_H$, waits to receive the transmitted character, then checks to see if a $55_H$ was received.

A P display in the second digit from the right indicates that the test passed, a 0 in this digit indicates that a character was not received within 80 ms, and a 1 indicates that a character was received, but it was the wrong value.

## D.3 Test 3 Ramps

Test 3 checks the correction DACs (U22 and U14), the attenuation DACs (U9 and U10), and the associated circuitry.

The ramps are generated by writing a digital word into the correction DACs, which is increased by 1 before each write cycle until it overflows 12 bits, then the ramp starts over. A write cycle is performed in three steps. The first step writes the upper 8 bits of the digital word to Address $X001_H$, where X is 4 for the Gain DAC and 3 for the Zero DAC.

The second step writes the lower 4 bits of the digital word, seen on the upper 4 bits of the data bus to Address $X000_H$. The third step initiates an internal DAC transfer cycle by writing to Address $X002_H$.

Using the INCR pushbutton in Test 3 changes the attenuation factor. The 4 attenuation factors are 1, 0.5, 0.25, and 0.125. These attenuation factors are stored in the attenuator DACs by writing a digital word of $FF_H$, $7F_H$, $3F_H$, or $1F_H$. These words are stored by writing to Address $2000_H$ for the Gain Attenuator DAC or Address $1000_H$ for the Zero Attenuator DAC.

## D.4 Test 4 Offset Adjustment

Test 4 is used to adjust the Offset voltages of U13 and U21. A digital word of 0 is written into the correction DACs and the adjustment is then performed, using RV1 and RV2.

## D.5 Test 5 Bar Graph

Test 5 writes the appropriate codes to the Display Controller, U27, to enable each segment of Bar Graph Display. This test writes at a rate of 0.5 seconds as determined by an internal timer of the 8031.

## D.6 Test 6 Displayed Function LEDs

Test 6 writes the appropriate codes to the Display Controller, U27, to step through each of the Displayed Function LEDs: Peak, Window, Stab. Rate, and Analog Rng. The rate is determined by the same internal timer as in Test 5.

## D.7 Test 7 ADC Interface

Test 7 checks the ADC interface, which consists of buffers U1 and U4, latches U2 and U3 and the interrupt logic U11 and U12. The idea of the test is to verify that each bit received from an ADC works independently of any other bit.

Test 7 services the ADC interrupt by reading the data from the latches U2 and U3. It converts the binary word to BCD and displays the result on the 5-digit display.

## D.8 Diagnostic Test Procedure

Before applying power to the 8233, connect TP11 to TP7 (ground). When power is applied, the 8233 will enter the diagnostic routines.

For Test 2, connect J102 pins 6 and 8 together before running the test.

1. Observe the front panel and verify the following display:

   Bar Graph - Off
   LEDs - Off
   5 Digit Display - MSD LSD
   3 PP

   The MSD indicates the present test number. The LSD indicates the status of Test 1, and P indicates that it passed. A 0 or a 1 indicates a failure. The next significant digit indicates the status of Test 2, a P for passed and a 0 or a 1 for failed. Refer to Appendix D.1 through D.7 for descriptions for the tests.

2. With the Unit in Test 3, use a scope referenced to TP 10 to verify a ramp from +5 to –5 V ±0.25 V at TP 2 and TP3.

3. Press the INCR pushbutton once and verify that the ramps on TP2 and TP3 are now from +2.5 to –2.5 V ±0.125 V.

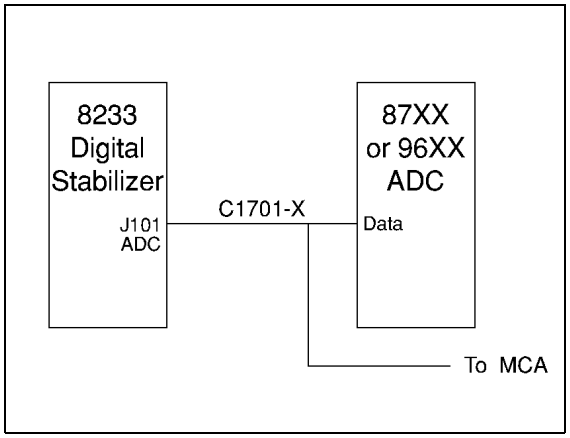
4. Press the INCR pushbutton again and verify that the ramps are not +1.25 to –1.25 V ±0.0625 V.

5. Press the INCR pushbutton a third time and verify that the ramps are now +0.625 to –0.625 V ±0.0312 V.

6. Press the SET pushbutton to step to Test 4. This should be indicated by the MSD of the display.
7. Reference the DVM to TP10 and connect the positive lead to TP12. Install a shunt jumper on W9.
8. Adjust RV2 for a reading of 0.0 ±0.5 mV on the DVM.
9. Move the meter from TP12 to TP9 and the shunt jumper from W9 to W10.
10. Adjust RV1 for a reading of 0.0 ±0.5 mV on the DVM.
11. Remove the DVM and the shunt jumper.
12. Press the SET pushbutton to step to Test 5. This should be indicated by the MSD of the display.
13. Test 5 checks the Bar Graph by turning on the segments starting at the 0 position and working toward the –100 position then working towards the +100 position. When all segments are lit the test repeats. Verify proper operation of Test 5.
14. Press the SET pushbutton to step to Test 6. This should be indicated by the MSD of the display.
15. Test 6 checks the Displayed Function LEDs: PEAK, WINDOW, STAB. RATE, and ANALOG RNG. Test 6 individually enables these four LEDs. Verify proper operation of Test 6.
16. Press the SET pushbutton to step to Test 7. The display is now used to display the ADC data received by the 8233.
17. Connect a Model 8210 Precision Pulser to the ADC IN BNC.
18. Verify that the 8233 displays the BCD representation of the conversion address generated by the ADC.
19. Check that each address bit, $2^0$ to $2^{13}$, generated by the ADC is received by the 8233 independently of the other address bits. This is done by comparing the conversion address with the 8233 display. By adjusting the amplitude of the 8210 pulser, each address line may be enabled independently. The binary weight of the address enabled should be the same as the value displayed on the 8233.
20. Turn the NIM BIN Off and remove the ground from TP11.

# E. Setup Diagram

This block diagram is included to help you set up your system.



# Warranty

Canberra's product warranty covers hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

**DOMESTIC WARRANTY**

Canberra (we, us, our) warrants to the customer (you, your) that equipment manufactured by us shall be free from defects in materials and workmanship under normal use for a period of one (1) year from the date of shipment.

We warrant proper operation of our software only when used with software and hardware supplied by us and warrant that our software media shall be free from defects for a period of 90 days from the date of shipment.

If defects are discovered within 90 days of receipt of an order, we will pay for shipping costs incurred in connection with the return of the equipment. If defects are discovered after the first 90 days, all shipping, insurance and other costs shall be borne by you.

**LIMITATIONS**

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE.

**EXCLUSIONS**

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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# F. Environmental Specifications

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- a rack or tabletop enclosure fully closed on all sides with rear door access
- single point external cable access
- blank panels to cover open front panel Bin area
- compliant grounding and safety precautions for any internal power distribution
- the use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance to the specified EU requirements.

Operating Temperature: 0-50 degrees Centigrade
Operating Humidity: 0-80% Relative, Non-condensing
Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution degree 2