DIGITAL STABILIZER
Model 8232

0585

Operator's Manual

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

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Section 1. Introduction

The Model 8232 is used to maintain the stability of a nuclear spectrometer system in high resolution experiments of long duration. It accomplishes this by automatically correcting the conversion gain and/or zero intercept of a binary analog-to-digital converter (ADC). The Model 8232 can be used to correct both conversion gain and zero intercept simultaneously, if required. Errors are detected by monitoring the ADC digital output, which reflects drift from all preceding system components. Consequently, all system drift can be compensated for by applying correction to the ADC only. The Model 8232 accepts parallel entry of up to 14 bits (16 384 channels) from the ADC.

Operation of the Model 8232 is the same for either conversion gain or zero intercept correction, except for the relative location of the reference channel selected. A high-numbered channel is selected for gain stabilization, since it will exhibit a more pronounced gain drift effect than a low-numbered channel. A low-numbered channel is selected for zero stabilization to minimize gain drift interaction. The stabilization reference channel is selected along with a "window", which is centered about the reference channel. The analog output range can be varied to compensate for expected or encountered drift of the system. Drift direction, magnitude, and rate of correction are indicated by a zero-center LED bar graph display. A digital readout of correction rate is also available.

Analog recorder outputs on the rear panel enable drift monitoring over extended periods of time. A serial interface is also provided to allow remote control of the 8232. The setup parameters, status information and enabling or disabling of stabilization can all be accessed with an EIA device.

Section 2. Specifications

2.1 INPUTS

ADC - Binary maximum of 14 bits, parallel access, compatible with the Canberra External ADC Interface.

2.2 OUTPUTS

CORRECTION SIGNAL - Output impedance 1 kilohm; resolution 1 part in 4096; stability closed-loop self-correcting; output voltage range -5 V to +5 V with selectable attenuation factors. This range will result in a ±2% change in the zero setting and a ±5% change in the gain setting for 8075 and 8077 type ADCs.
RECORDER OUTPUT - Output impedance 1 kilohm; resolution 1 part in 4096; stability better than 0.01%/°C; range -5 V to +5 V.

2.3 DISPLAYS

LED BAR GRAPH - Displays percent Correction for either Gain or Zero.
5 DIGIT LED DISPLAY - Displays Peak Channel, Window Width, Correction Rate, or Analog Range for either Zero or Gain. Selection is made via front panel controls.
DISPLAYED FUNCTION INDICATORS - 4 LEDS which indicate which parameter is being displayed on the 5 digit display
ENABLED LED - Indicates that stabilization is enabled for Zero or Gain, depending on the Zero/Gain switch.

2.4 CONTROLS

ZERO/GAIN TOGGLE SWITCH - Chooses Zero or Gain parameters for display.
SET PUSHBUTTON - Initiates the setup mode then selects the digit of the parameter to be set.
INCREMENT PUSHBUTTON - Increments display through Peak, Window, Stabilization Rate, and Analog Range parameters and, in setup mode, increments selected digit.
ON/HOLD/OFF TOGGLE SWITCHES

ON Stabilization enabled
HOLD Stabilization disabled but last correction voltage remains.
OFF Stabilization disabled and correction voltage reset to 0 V.

REMOTE/MANUAL - Manual enables front panel controls. Remote enables EIA control and disables front panel.
REMOTE CONTROL - Rear panel CONTROL connector permits input and output of setup parameters, input of stabilization control, and output of stabilization status. Refer to Appendices A and B.
PARITY - Internal jumpers (J3 - J4) select even, odd, or no parity for EIA data I/O. Refer to section 3.3
BAUD - Internal jumpers (J5 - J6) select 300, 1200, 2400, or 9600 Baud for EIA data I/O. Refer to section 3.3.

2.5 CONNECTORS

ADC - 26-pin rectangular ribbon connector; rear panel; pin-out compatible with Canberra NIM ADC connector.
CONTROL - 9-pin female D-type; rear panel mounted.

2.6 CABLES AND ACCESSORIES

CABLE - A 26-pin 10 cm (4 in.) ribbon cable is supplied; mates with Canberra NIM ADCs. Other cable lengths are available, consult factory. For Canberra ADCs requiring a 25-pin D-type cable connector, specify Canberra cable C-8075A.

2.7 POWER REQUIREMENTS

+12 V dc — 140 mA
-12 V dc — 140 mA

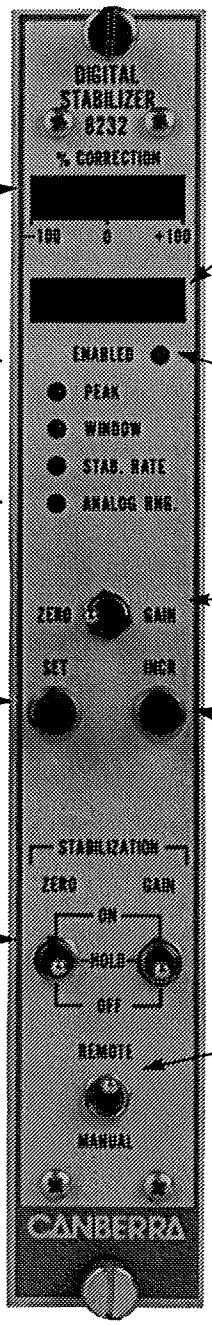
2.8 PHYSICAL

SIZE - Standard single width NIM module 3.43 × 22.12 cm (1.35 × 8.71 in.).
NET WEIGHT - 0.9 kg (1.9 lbs.)
SHIPPING WEIGHT - 1.8 kg (4.0 lbs.)

Section 3.
Controls and Connectors

3.1 FRONT PANEL

Refer to Section 2 for additional information and signal specifications.



% CORRECTION
Ten-segment LED indicator displays the direction of drift and the percent of full scale correction in increments of 20%.

DISPLAYED FUNCTION INDICATORS
4 LEDs which indicate which parameter is being displayed on the 5-digit, display.

SET
Pushbutton for selecting which digit of the displayed parameter is to be set.

ON/OFF/HOLD
2 toggle switches for Zero and Gain
ON Enables stabilization.
HOLD Disables stabilization but holds last correction voltage.
OFF Disables stabilization and resets correction voltage to 0 V.

5 digit LED display. Displays 1 of 4 parameters for Zero or Gain: Peak Channel, Window Width, Stabilization Rate, or Analog Range.

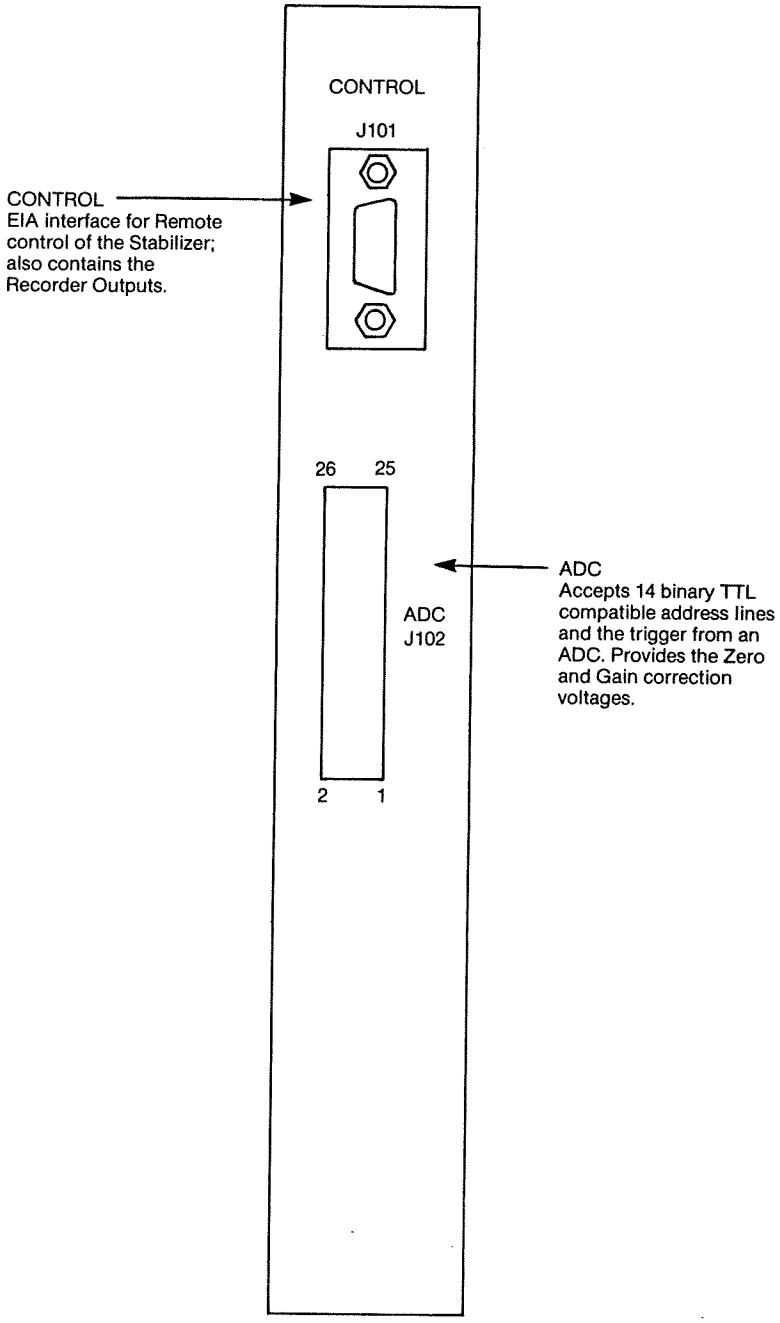
ENABLED LED
Indicates that stabilization is enabled for Zero or Gain, depending on the Zero/Gain switch.

ZERO/GAIN SWITCH
Selects either Zero or Gain parameters for display.

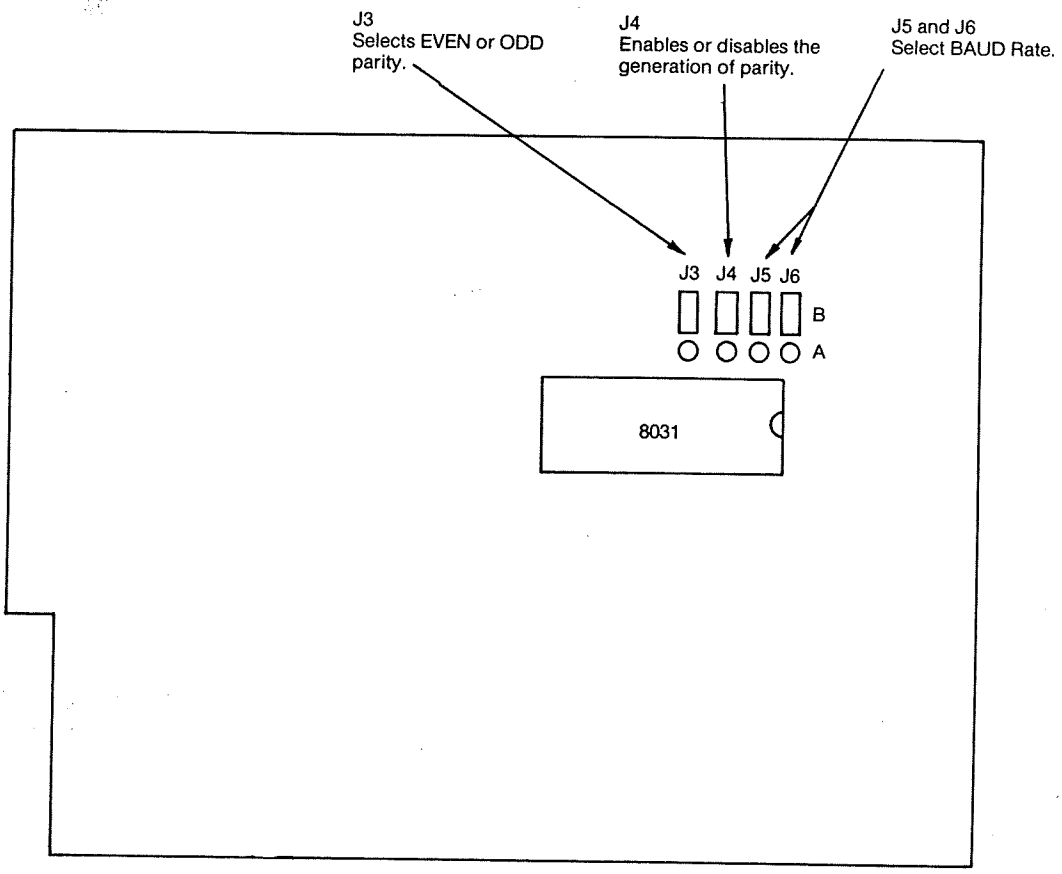
INCR
When not in the set-up mode, used to increment through the Displayed Function Indicators. When in the set-up mode, used to increment the digit being set.

REMOTE/MANUAL
Toggle switch to select REMOTE or MANUAL Stabilizer control mode.

3.2 REAR PANEL



3.3 INTERNAL CONTROLS



PARITY

FUNCTION	J3	J4
OFF	—	B
ON	—	A
ODD	B	A
EVEN	A	A

BAUD

RATE	J5	J6
300	B	B
1200	B	A
2400	A	B
9600	A	A

Section 4. Operation

4.1 % CORRECTION

The % CORRECTION indicator is a ten segment LED bar graph, which indicates the percentage of full scale correction being applied in increments of twenty percent. The indicator is a center zero type; therefore, it also indicates the direction of the drift which the Stabilizer is correcting for, Zero or Gain, depending on the position of the ZERO/GAIN switch.

4.2 5 DIGIT DISPLAY

Displays one of the four parameters for Zero or Gain. The displayed parameter is indicated by the Displayed Function LEDs.

PEAK

Indicates the PEAK channel which the Stabilizer is correcting on. Valid settings range from 0 to 16 383 in steps of 1 channel.

WINDOW Width

Indicates the number of channels used by the Stabilizer as its sampling range. The Window is centered about the Peak channel, but not allowed to wrap around 0 or 16 383. Valid settings for the Window are 1 to 999 channels in odd valued increments of 2.

STABilization RATE

Indicates the count rate of the input data which gives rise to a change in the correction voltage. This display is in Counts Per Second (CPS). Input data which give rise to a change in the correction voltage are the data which fall inside the window but are not equal to the peak setting.

ANALOG RANGE

Indicates the value of the Analog Attenuation Factor. The attenuation is applied to the ±5 V range of the correction voltage from the Stabilizer to the ADC. For example, if the attenuation factor is set to 0.5, the range of the correction voltage is ±2.5 V. The attenuation factor is useful when the expected system drift does not require the full range of correction and a smoother correction is desired. This smoother correction will lessen the stabilizer's peak-broadening effect. The attenuation factor does not affect the Recorder Outputs. The settings for Analog Range are 1.0, 0.5, 0.25, or 0.125.

4.3 DISPLAYED FUNCTION INDICATORS

The DISPLAYED FUNCTION INDICATORS are four LEDs which, in conjunction with the ZERO/GAIN switch, indicate which parameter is being displayed. The desired parameter is selected using the INCRement pushbutton when not in the set-up mode.

4.4 ENABLED LED

The ENABLED LED indicates that stabilization is ON. The ZERO/GAIN switch selects display of ZERO enabled or GAIN enabled. Stabilization can be enabled via the front panel switches (MANUAL) or the serial port (REMOTE).

4.5 ZERO/GAIN

The ZERO/GAIN switch selects either the Zero or the Gain parameters and status for display and set-up purposes. Stabilization can be activated for Zero or Gain regardless of the position of the ZERO/GAIN switch.

4.6 SET

The SET pushbutton enables the Set-up mode and selects the digit of the displayed parameter to be set. Pressing the SET button will start the least significant digit of the display blinking. If Analog Range is displayed, all digits will start blinking. Subsequent pushes will change the blinking digit to the next significant digit. When the most significant digit is blinking, pressing the SET pushbutton will exit the set-up mode and store the parameters in nonvolatile memory.

4.7 INCRement

The INCRement pushbutton is a dual-function button. When not in the set-up mode, pressing the INCRement button will increment the Displayed Function Indicators and the display to the next function. When in the Set-up mode, pressing the INCRement button will increment the value of the digit being set (blinking).

4.8 ZERO and GAIN ON/HOLD/OFF

These two three-position switches control ZERO and GAIN Stabilization. With the switch in the OFF position, stabilization is disabled and the correction voltage is held to zero volts. Putting the switch in the ON position enables the stabilization process. The Stabilizer will compare the incoming data to the Peak setting and the window limits and add or subtract one step to or from the correction voltage, depending on whether the incoming data was above or below the Peak Channel. When the switch is in the HOLD position, the correction voltage is not updated, but the last correction voltage is maintained at the output.

4.9 REMOTE/MANUAL

The REMOTE/MANUAL switch selects either the Remote mode or the Manual mode. The Manual mode is used when front panel control is desired. With the switch in MANUAL, the serial port is disabled. The Remote mode is used when serial port control is desired. Control consists of being able to set parameters, duplicate the function of the ON/HOLD/OFF switch and read out the parameters or status of the stabilizer. Remote control is accomplished through a series of Escape Sequences which are defined in Appendix B. With the switch in the REMOTE position, the SET button and the ON/HOLD/OFF switches are disabled.

Section 5.
Serial Port Operation

5.1 SPECIFICATIONS

Remote Control of the 8232 is accomplished via a serial port accessed through the rear panel CONTROL connector (J101). Received and transmitted data are accommodated using EIA RS-232C standard signal levels. A DTR line is also provided which indicates that the 8232 is in Remote and ready to accept data.

The data format is: one start bit, 8 data bits, parity bit if enabled, and one stop bit. Parity is selectable via internal jumpers, see section 3.3. Baud is jumper selectable for rates of 300, 1200, 2400, or 9600. Refer to section 3.3 for jumper positions.

5.2 PARAMETER SETUP

Each setup parameter can be modified through the remote control interface. Using an escape sequence, summarized in Appendix B, Peak Channel, Window Width, or Analog Range can be modified for both Gain and Zero. Each parameter is entered with its own escape sequence.

After the parameters are entered, it may be desirable to store these new parameters in the nonvolatile memory using an escape sequence. If this is not done, the previous parameter settings remain in the nonvolatile memory.

5.3 COMMANDED REPORTS

Unit Status and Gain or Zero Setup Parameters and Gain, Zero, and Unit Status can be read out through the CONTROL connector.

NOTE: Any report requests issued before the completion of the transmission of a previously requested report will be ignored.

5.3.1 Setup Parameters

The Gain or Zero Setup Parameters can be read from the 8232. The report consists of Peak Channel, Window Width, and Analog Range. The report formats are defined in Appendix B.9 and B.11.

5.3.2 Status

The Gain or Zero Status can be read from the 8232. The Status consists of ON/HOLD/OFF information, Present Correction, and Stabilization Rate. The report formats are defined in Appendix B.10 and B.12.

5.3.3 Unit Status

The Unit Status, which is an error code indicating a fault in an escape sequence received by the 8232, can be read from the unit. The format and error codes are listed in Appendix B.13.

5.4 STABILIZATION CONTROL

The Stabilization status can be controlled via the serial port. One of three modes, ON, HOLD, or OFF, can be enabled for Gain or Zero using an Escape Sequence. These Escape Sequences are listed in Appendix B.7 and B.8.

Section 6.
Theory of Operation

6.1 HARDWARE

The Model 8232's hardware is based around the Intel 8031 microcontroller, which is the ROMless version of the 8051. The program code for the 8031 is contained entirely in one 27C32 PROM. The program RAM is internal to the 8031. The setup parameters are stored in the external nonvoltatile RAM (NVRAM).

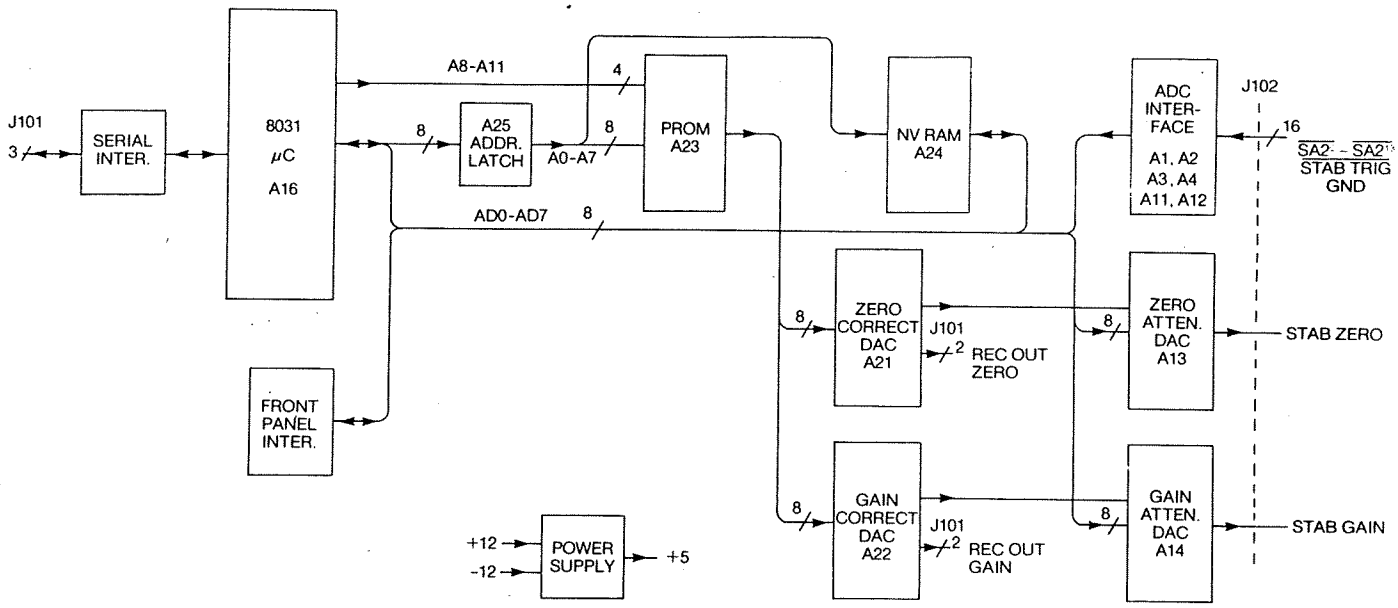
A conversion address is latched into the ADC Interface by the ADC. This storage also generates an interrupt to the 8031. The 8031 services this interrupt by reading the address from the ADC Interface and comparing that address to the Peak and Window settings for Zero and Gain, if they are enabled. If the address of conversion falls in one of the Windows and is not equal to the Peak Channel, then the Zero or Gain Correction DAC is appropriately adjusted. Each conversion which is above the peak and below the upper limit of the Window subtracts one from the value presently stored in the DAC. A conversion below the Peak Channel adds one to the present value stored in the Correction DAC.

The output from the Attenuation DACs is connected to the ADC. An increase in this correction voltage will result in an increase in the ADC's zero or gain setting, a decrease will result in a decrease in the ADC's zero or gain setting.

The Analog Range setting is passed to the Attenuation DACs. The output of the Correction DAC is used as the reference voltage for the Attenuation DAC; therefore, the Correction DAC Output is multiplied by the Attenuation Factor. An Attenuation Factor of 1 results in a code of FF_H being loaded into the Attenuation DAC. The code for 0.5 is $7F_H$, for 0.25 it is $3F_H$, and for 0.125 is $1F_H$.

The front panel interface consists of the switch buffer and the display controller. The switch buffer, which consists of A26, A27, A32 and A33, is periodically read by the Firmware. The display controller A10, controls the bar graph, the 5-digit display and the Displayed Function LEDs. The display controller generates the scan rate and the seven-segment code for the 5-digit display. The only requirement of the firmware is to load the proper binary code and digit address for the character to be displayed.

The major portion of the serial interface is internal to the 8031. The UART and the BAUD Rate generator are both integral parts of the 8031. The only external parts required are EIA-to-TTL-level translators, A9 and A29.



Model 8232
Hardware Block Diagram

6.2 5 VOLT POWER SUPPLY

The +5 V logic power supply is synthesized by a push-pull switching inverter which operates off the +12 V and -12 V NIM voltages. Q1 and Q2 are operated as saturating switches in a relaxation oscillator through the power transformer. The operating frequency is set by the transformer primary inductance and C23 at about 70 kHz. The feedback winding of the transformer alternates drive between Q1 and Q2 to generate a push-pull voltage to the primary. Rectifiers D9 and D10 convert the ac to a full-wave output. XFMR-1 in the -12 V line, driving the center tap of the power transformer, couples an ac waveform to the secondary at the output of the rectifiers in a phase and level which effectively cancels the ripple voltage in the dc output. C28 and C29 are used to integrate the small residual ripple and reduce noise in the logic output.

Q3 and Q4 provide short-circuit protection of the output by sensing the inverter's input dc current via R42, and switching off the drive to Q1 and Q2 if a fault is detected. Q4 is normally off and Q3 normally on. When an overcurrent is detected, Q4 switches on and Q3 off. Positive feedback through R40 and C19 latch Q3 off for about 1 second. As C19 completely charges to -12 V (with Q3 off), Q4 is again switched off and Q3 on to permit R42 to resample the input current. If a fault persists, Q4 is again switched back on and Q3 off to again disable the inverter. This results in a periodic resampling of the load condition in a manner which limits the stress on Q1 and Q2. C24, C27, and the input toroid together prevent generation of any interference back on the ±12 V supplies from the inverter operation.

6.3 FIRMWARE

The Idle Loop is the main body of the firmware. The Idle Loop updates the bar graph, the 5-digit display, and the Displayed Function LEDs along with reading the present position of the front panel switches. The Idle Loop also services the serial buffer when it contains a command received from an external EIA device.

All of the other routines are entered due to internal or external interrupts. The ADC Interrupt Service Routine starts its processing by reading the conversion address from the ADC interface logic. This read is performed as two bytes: the low byte first then the high byte. Reading the high byte also clears the interrupt and allows the ADC interface logic to accept another input from the ADC.

The ADC Interrupt Service Routine then compares the conversion address to the gain and zero window limits and to the gain and zero peak channels. If the address falls within one of the windows and is not equal to the peak channel, it will cause a change in the correction output. The final function performed by the ADC Interrupt Service Routine is to update appropriate Stabilization Rate Register.

Pushing either of the front panel push buttons, SET or INCR, will generate an interrupt and cause the processor to enter the Push Button Interrupt Service Routine. This routine first determines which push button has been pressed by reading the switch interface. If the SET push button has caused the interrupt, the Push Button Interrupt Service Routine will increment an internal register used to indicate

which digit is being set. If it was the INCR push button that caused the interrupt, the Push Button Interrupt Service Routine will increment the digit being set if the set mode is enabled or increment the Displayed Function LEDs register if the set mode is not enabled.

The first step of the Serial Interrupt Service Routine is to determine if the interrupt is a receiver or transmitter interrupt. The receiver has priority over the transmitter interrupt. If the interrupt is a receiver interrupt, the Serial Interrupt Service Routine moves the character from the internal UART to the Receiver Buffer, testing each character to determine if it is a terminator. When a terminator is encountered, a flag is set indicating the buffer contains a complete command and the Idle Loop services that flag.

If the interrupt is a transmitter interrupt, the Serial Interrupt Service Routine moves a character from the transmitter buffer to the internal UART for transmission. This process continues until the transmitter buffer is emptied or the transmission process is aborted by an escape sequence.

Appendix A. Connector Signals

NOTE: Negative true signals are shown as $SA2^0/$.

A.1 J102 ADC

Pin	Signal	Description
1 3 5 7 9 11 13 15 17 19 21 23 25 4	$SA2^0/$ $SA2^1/$ $SA2^2/$ $SA2^3/$ $SA2^4/$ $SA2^5/$ $SA2^6/$ $SA2^7/$ $SA2^8/$ $SA2^9/$ $SA2^{10}/$ $SA2^{11}/$ $SA2^{12}/$ $SA2^{13}/$	Binary Address data. Negative true logic. Input fron an external device.
14	STAB GAIN	Gain Correction Voltage
16	STAB ZERO	Zero Correction Voltage
20	STAB TRIGGER	Pulse from external device, indicates valid address present
22	GND	Ground

A.2 J101 CONTROL

Pin	Signal	Description
2	GND	Ground for Gain Recorder Output
3	REC OUT GAIN	Gain Recorder Output
4	GND	Ground for Zero Recorder Output
5	REC OUT ZERO	Zero Recorder Output
6	DATA IN	Serial Data Input to 8232
7	GND	Ground for Serial Port
8	Data OUT	Serial data transmitted from 8232
9	DTR	Data Terminal Ready, indicates 8232 ready to accept serial transmission

Appendix B. Remote Control Escape Sequences

B.1 SET GAIN PEAK CHANNEL

ESC Pn @

Pn is the decimal Peak value expressed as a 1 to 5 character ASCII string.

B.2 SET GAIN WINDOW WIDTH

ESC Pn A

Pn is the decimal window value expressed as a 1 to 3 character ASCII string.

B.3 SET GAIN ANALOG RANGE

ESC Ps B

Ps is a selective parameter expressed as an ASCII character, where:

0 = Full, 1.0
1 = Half, 0.5
2 = Quarter, 0.25
3 = Eighth, 0.125

B.4 SET ZERO PEAK CHANNEL

ESC Pn C

Pn is the decimal peak value expressed as a 1 to 5 character ASCII string.

B.5 SET ZERO WINDOW WIDTH

ESC Pn D

Pn is the decimal window value expressed as a 1 to 3 character ASCII string.

B.6 SET ZERO ANALOG RANGE

ESC Ps E

Ps is a selective parameter expressed as an ASCII character, where:

0 = Full, 1.0
1 = Half, 0.5
2 = Quarter, 0.25
3 = Eighth, 0.125

B.7 GAIN STABILIZATION ON/HOLD/OFF

ESC Ps F

Ps is a selective parameter expressed as an ASCII character, where:

0 = OFF
1 = HOLD
2 = ON

B.8 ZERO STABILIZATION ON/HOLD/OFF

ESC Ps G

Ps is a selective parameter expressed as an ASCII character, where:

0 = OFF
1 = HOLD
2 = ON

B.9 REPORT GAIN SETUP

ESC H

Initiates the report (response from 8232).

Report Format

ESC Pp; Pw; Pr H

where:

Pp = 5 digits, decimal value of the Peak
Pw = 3 digits, decimal value of the Window Width
Pr = 1 digit, Analog Range; format the same as Ps for Set Analog Range

B.10 REPORT GAIN STATUS

ESC I

Initiates the report (response from 8232).

Report Format

ESC Po; Pr; Pc I

where:

Po = ON/HOLD/OFF, format the same as Ps for Set Gain Stabilization
Pr = 5 digits, which indicate the Stabilization Rate
Pc = 3 digits, Percent Correction

B.11 REPORT ZERO SETUP

ESC J

Initiates the report (response from 8232).

Report format is the same as the format for Gain Setup report except J is the terminator.

B.12 REPORT ZERO STATUS

ESC K

Initiates the report (response from 8232).

Report format is the same as the format for Gain Status except K is the terminator.

B.13 REPORT UNIT STATUS

ESC L

Initiates the report (response from 8232).

Report Format

ESC Pe L

where Pe is an error code, where:

0 = no error
1 = number of characters received exceeded the number allowed for the parameters of the escape sequence; spaces are ignored
2 = Parameter not an ASCII 0-9
3 = Invalid terminator received
4 = Data received not preceded by an ESC
5 = Value of Ps exceeded 3 for Analog Range set-up or 2 for Stabilization ON/HOLD/OFF
6 = Number of P's not consistent with terminator

B.14 STORE PARAMETERS

ESC M

This command copies the set-up parameters from the internal RAM to the non-volatile memory.

B.15 TERMINATE REPORT

ESC N

Terminates any report in progress.

Appendix C.
Self Tests

The 8232 is equipped with diagnostics which can verify the 8232's operation.

Sections C.1 through C.7 describe the seven tests. Section C.8 details the test procedure.

C.1 TEST 1 NVRAM TEST

Test 1 checks the non-volatile RAM, A24. The first part of the test writes the address into the RAM and then reads it back. If this test passes, it continues to the next step. If it fails, it displays a 0 and jumps to Test 2.

The second part of the test performs a store cycle on the NVRAM, which places what's in RAM into internal EEPROM, clears the RAM, recalls the data from the EEPROM and then checks for the correct pattern. If this part passes, a P is displayed and Test 2 is started. If this part fails, a 1 is displayed before starting Test 2.

C.2 TEST 2 SERIAL PORT TEST

Test 2 checks the serial port internal to the 8031 and the EIA driver and receiver. The 8031 transmits a 55_H, waits to receive the transmitted character, then checks to see if a 55_H was received.

A P display in the second digit from the right indicates that the test passed, a 0 in this digit indicates that a character was not received within 80 ms, and a 1 indicates that a character was received, but it was the wrong value.

C.3 TEST 3 RAMPS

Test 3 checks the correction DACs (A21 and A22), the attenuation DACs (A13 and A14), and the associated circuitry.

The ramps are generated by writing a digital word into the correction DACs, which is increased by 1 before each write cycle until it overflows 12 bits, then the ramp starts over. A write cycle is performed in three steps. The first step writes the upper 8 bits of the digital word to Address $X001_H$. The second step writes the lower 4 bits of the digital word, seen on the upper 4 bits of the data bus to Address $X000_H$. The third step initiates an internal DAC transfer cycle by writing to Address $X002_H$. X is 4 for the Gain DAC and 3 for the Zero DAC.

Using the INCR pushbutton in Test 3 changes the attenuation factor. The 4 attenuation factors are 1, 0.5, 0.25, and 0.125. These attenuation factors are stored in the attenuator DACs by writing a digital word of FF_H, $7F_H$, $3F_H$, or $1F_H$. These words are stored by writing to Address 2000_H for the Gain Attenuator DAC or Address 1000_H for the Zero Attenuator DAC.

C.4 TEST 4 OFFSET ADJUSTMENT

Test 4 is used to adjust the Offset voltages of A19 and A34. A digital word of 0 is written into the correction DACs and the adjustment is then performed, using RV1 and RV2.

C.5 TEST 5 BAR GRAPH TEST

Test 5 writes the appropriate codes to the Display Controller, A10, to enable each segment of Bar Graph Display. This test writes at a rate of 0.5 seconds as determined by an internal timer in the 8031.

C.6 TEST 6 DISPLAYED FUNCTION LEDs

Test 6 writes the appropriate codes to the Display Controller, A10, to step through each of the Displayed Function LEDs: Peak, Window, Stab Rate, and Analog Rng. The rate is determined by the same internal timer as in Test 5.

C.7 TEST 7 ADC INTERFACE TEST

Test 7 checks the ADC interface, which consists of buffers A1 and A11, latches A2 and A12 and the interrupt logic A3 and A4. The idea of the test is to verify that each bit received from an ADC works independently of any other bit.

Test 7 services the ADC interrupt by reading the data from the latches A2 and A12. It converts the binary word to BCD and displays the result on the 5-digit display.

C.8 DIAGNOSTIC TEST PROCEDURE

Before applying power to the 8232, connect A16 pin 8 to TP7 (ground). When power is applied, the 8232 will enter the diagnostic routines.

For Test 2, connect J101 pins 6 and 8 together before running the test.

C.8.1

Observe the front panel and verify the following display:

Bar Graph — OFF
LEDs — OFF

5 Digit Display —	MSD	LSD
	3	PP

The MSD indicates the present test number. The LSD indicates the status of Test 1, a P indicates that it passed. A 0 or a 1 indicates a failure. The next significant digit indicates the status of Test 2, a P for passed and a 0 or a 1 for failed. Refer to Appendix C.1 through C.7 for descriptions of the tests.

C.8.2

With the unit in Test 3, use a scope referenced to TP 10 to verify a ramp from +5 to -5 V ±0.25 V at TP 2 and TP3.

C.8.3

Press the INCR pushbutton once and verify that the ramps on TP2 and TP3 are now from +2.5 to -2.5 V ±0.125 V.

C.8.4
Press the INCR pushbutton again and verify that the ramps are now +1.25 to -1.25 V ±0.0625 V.

C.8.5
Press the INCR pushbutton a third time and verify that the ramps are now +0.625 to -0.625 V ±0.0312 V.

C.8.6
Press the SET pushbutton to step to Test 4. This should be indicated by the MSD of the display.

C.8.7
Reference the DVM to TP10 and connect the positive lead to TP8. Install a shunt jumper on J9.

C.8.8
Adjust RV2 for a reading of 0.0 ±0.5 mV on the DVM.

C.8.9
Move the meter from TP8 to TP9 and the shunt jumper from J9 to J10.

C.8.10
Adjust RV1 for a reading of 0.0 ±0.5 mV on the DVM.

C.8.11
Remove the DVM and the shunt jumper.

C.8.12
Press the SET pushbutton to step to Test 5. This should be indicated by the MSD of the display.

C.8.13
Test 5 checks the Bar Graph by turning on the segments starting at the 0 position and working toward the -100 position then working towards the +100 position. When all segments are lit the test repeats. Verify proper operation of Test 5.

C.8.14
Press the SET pushbutton to step to Test 6. This should be indicated by the MSD of the display.

C.8.15
Test 6 checks the Displayed Function LEDs: PEAK, WINDOW, STAB. RATE, and ANALOG RNG. Test 6 individually enables these four LEDs. Verify proper operation of Test 6.

C.8.16
Press the SET pushbutton to step to Test 7. The display is now used to display the ADC data received by the 8232.

C.8.17
Connect the 8210 Precision Pulser to the ADC IN BNC.

C.8.18
Verify that the 8232 displays the BCD representation of the conversion address generated by the ADC.

C.8.19
Check that each address bit, 2^0 to 2^{12}, generated by the ADC is received by the 8232 independently of the other address bits. This is done by comparing the conversion address with the 8232 display. By adjusting the amplitude of the 8210 pulser, each address line may be enabled independently. The binary weight of the address enabled should be the same as the value displayed on the 8232.

C.8.20
Turn the NIM BIN OFF and remove the ground from A16 pin 8.