Model 8224
Analog Multiplexer

User's Manual

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ISO 9001
SYSTEM
CERTIFIED

CE

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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

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1. Introduction

The 8224 AMX module allows multiplexing of up to eight analog input signals through a single ADC. Multiplexing provides a cost effective method of handling a large number of low count rate input signals with one ADC and is ideal for environmental analysis and alpha spectroscopy applications. With additional 8224 modules, up to 32 input signals per ADC can be handled simultaneously. When used with a fast ADC, such as the Model 8715 800 ns Fixed Dead Time ADC, the 8224 provides cost effective multiple input capability with good count rate performance.

The 8224 contains one PDH (Peak Detect and Hold) circuit for each of the eight input signals. These analog memory circuits hold the peak value of each input pulse as a dc voltage level. The 8224's internal logic continuously scans the status of the eight PDH circuits at a rate of 500 kHz. When one of the PDH circuits captures a pulse, the scanner stops and connects the PDH to the ADC input. The 8224 then generates a gate pulse which initiates the ADC conversion cycle. When the conversion is complete, scanning resumes. Each event processed by the ADC is automatically routed into the associated memory group by appending routing bits to the digital ADC output word.

Each of the eight inputs to the 8224 is assigned a specific group size. For example, if the MCA is configured to provide 8192 channels of memory, and the 8224 is configured to provide eight 1K groups, data from input 1 is stored in the first 1024 channel group, data from input 2 is stored in the second 1024 group, and so on. This results in eight individual spectra, each representing one input signal, effectively simulating an individual ADC processing each input.

In addition, the 8224 provides live and real time clocks to accurately indicate the acquisition time for each group. The elapsed live and real time in seconds is accumulated in the first two channels of each group.

Internal DIP switches allow the user to select the group size, number of active inputs, module number assignment and master/slave designation of each 8224 in a system. These switches are accessible by removing the module's side panel.

LLD adjustment for all eight input signals is provided by a common front panel control.

Analog multiplexing can be performed in an external trigger mode which allows processing of dc voltage levels applied to the 8224's inputs. In this mode, each time a positive trigger signal arrives at the rear panel Trigger input, the 8224 takes a snapshot of the voltage levels of all active inputs. One event is acquired in each group with each trigger signal.

External control of each input (start/stop) can be provided by AccuSpec PC, Genie PC, or Genie VAX System Software. The MCA System also requires a parallel interface for individually controlling each input. An eight-bit interface can control one 8224 module.

2. Controls and Connectors

Front Panel

This is a brief description of the 8224's front panel controls and connectors. For more detailed information, refer to Appendix A, Specifications.

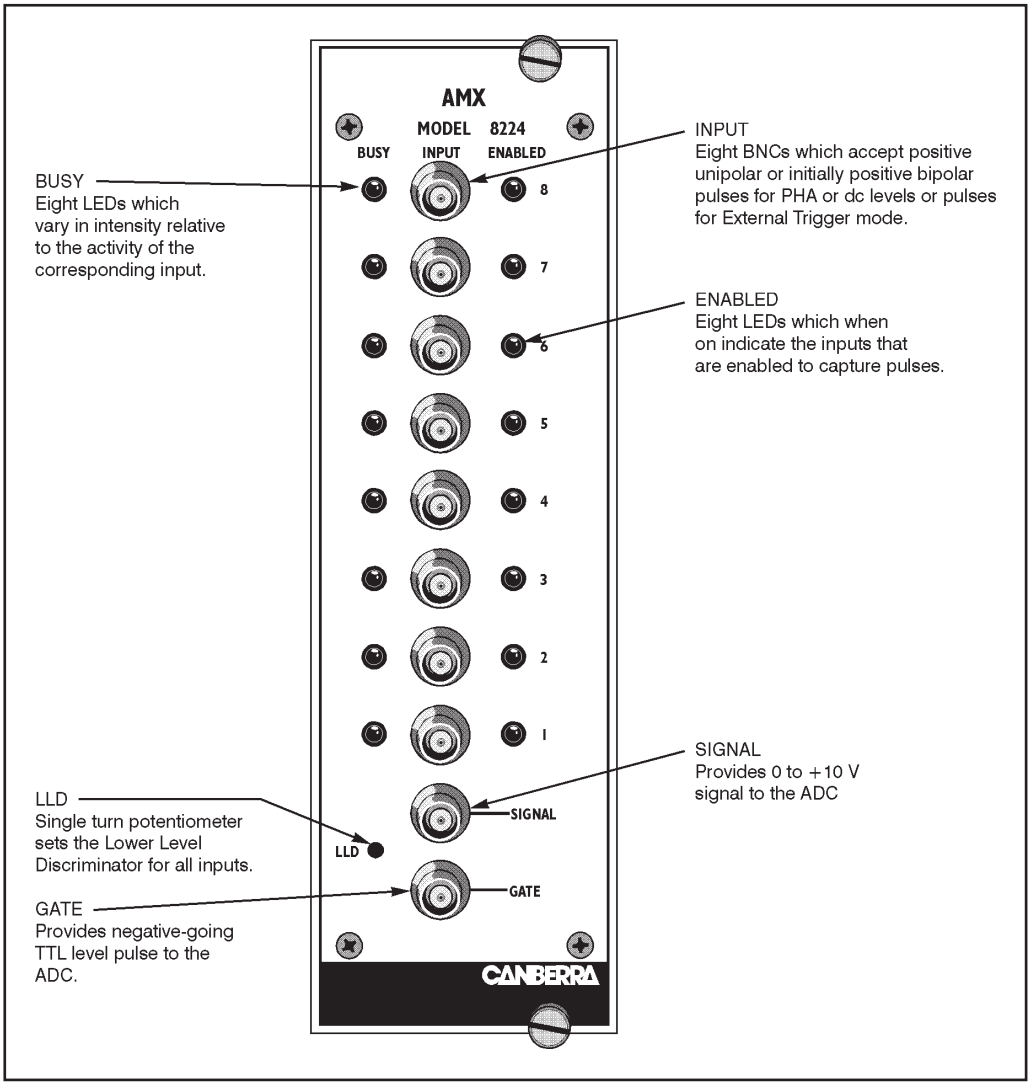

Figure 1 Front Panel Controls and Connectors

Rear Panel

This is a brief description of the 8224's rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

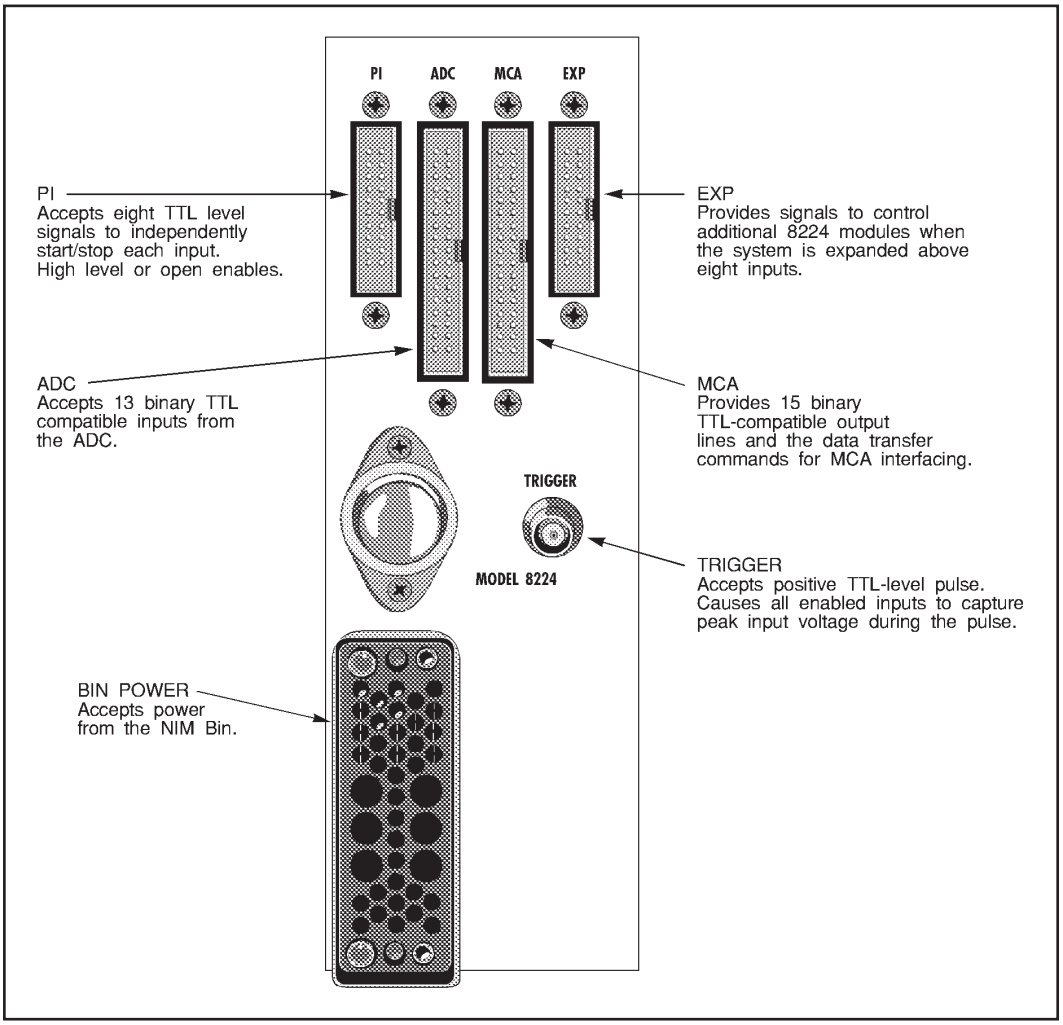

Figure 2 Rear Panel Controls

Internal Controls

The internal jumper plug controls should be set for your specific requirements before applying power to the module.

The factory default jumper settings are:

Inputs – 8
Module no. – 1 (switches 7 and 8 ON)
Group size – 512
Time Enable – ON

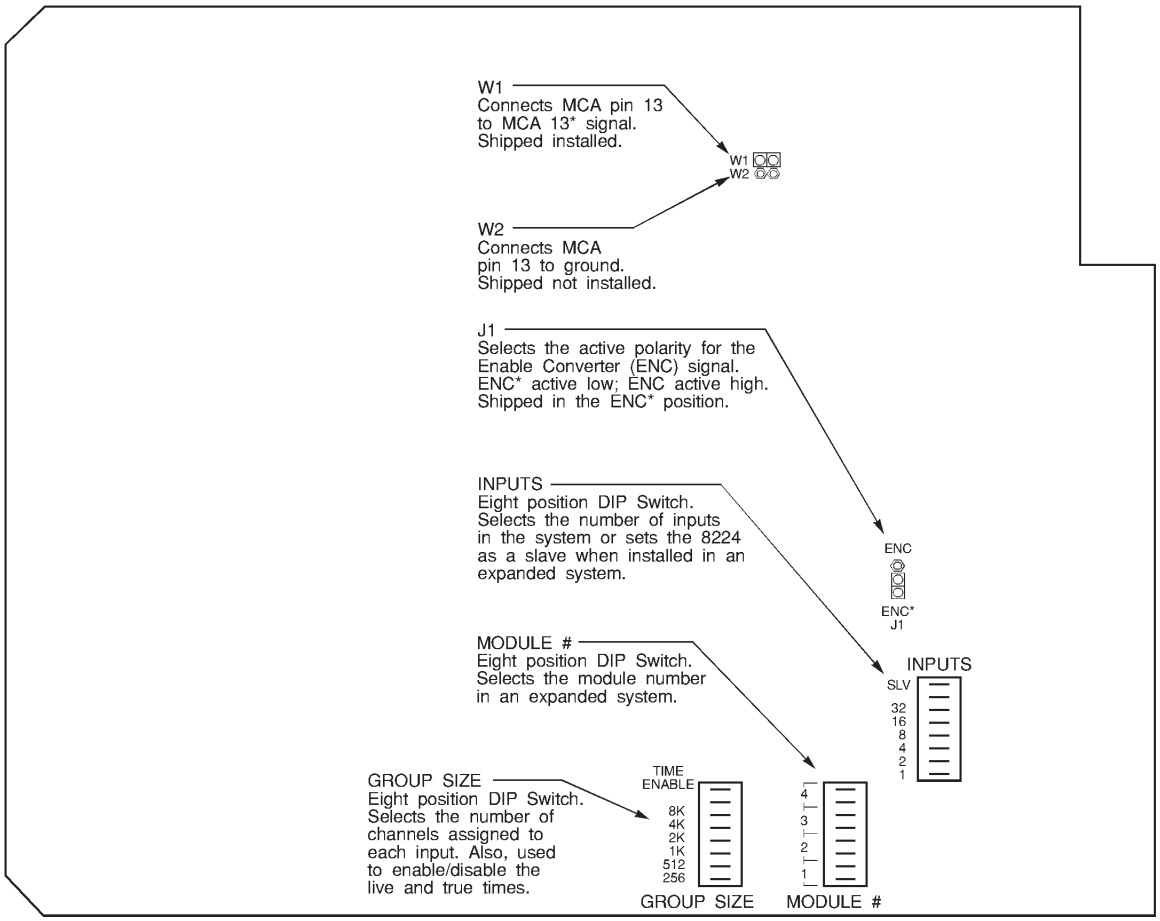

Figure 3 Internal Controls

3. Operation

The following sections discuss the use of the 8224 and its internal and external controls.

Setting up the 8224

The 8224 connects between the ADC and the MCA and multiplexes up to eight signal sources into the ADC. The 8224 stores the peak voltage of each input signal. Each peak voltage is sequentially connected to the ADC and a Gate pulse is generated by the 8224 which causes the ADC to convert that voltage. The second function of the 8224 is to append routing bits to the address from the ADC and then present the modified address to the MCA for storage.

One 8224 can accommodate up to eight inputs. If more than eight inputs are required then the system can be expanded to 32 inputs by adding additional 8224's which are configured as slaves. In an expanded system one 8224 is configured as the master and is the only 8224 connected to the ADC and the MCA. The remaining 8224's are configured as slaves and are connected to the master through the EXP connector.

The 8224 is configured by three internal DIP switches; Module Number, Group Size and Inputs. In order to determine the proper settings for these switches, two factors must be known. First, the number of inputs required. The number of inputs is set on the Inputs DIP switch (refer to "Inputs" on page 7). The second is the number of channels in the MCA memory. This value divided by the number of inputs will determine the setting for the Group Size switch (refer to "Group Size" on page 7). The Module Number switch is used in expanded systems where the Master is configured as module number 1 and each slave is configured with a unique module number, 2 through 4 (refer to "Module Number" on page 8).

The 8224 is connected to the ADC through the internal ADC connector and to the MCA through the rear panel MCA connector. The 8224 is also connected to the ADC's Signal In and Gate In BNC. The proper cables and connections are described in Appendix C.

All interface signals required between the ADC and the MCA are passed through the 8224 with the exception of the Dead Time (CDT). The 8224 provides individual Live and True timers for each input.

LLD

The Lower Level Discriminator (LLD) is a front panel potentiometer that sets the lower limit for the input signals to be accepted by the AMX for processing. The LLD setting is common to all eight of the AMX inputs. The input signal must exceed the LLD setting before it will be captured and stored by the Peak detector and hold circuit.

When operating the AMX in the External Trigger mode, the LLD must be set fully CCW.

Group Size

The Group Size switch selects the number of channels assigned to each input. The Group Size switch is an eight position DIP switch which is accessed by removing the right side cover. The allowable group sizes are 256, 512, 1K, 2K, 4K and 8K.

When selecting the group size, it is important to keep two factors in mind. The first is that the product of the group size and number of inputs (refer to “Inputs” on page 7) cannot exceed the number of channels in the MCA memory. Second, the group size should match the range of the ADC. The group size is selected by placing the corresponding switch to the ON position. Only one switch may be ON at a time.

Time Enable Switch

Included in the Group Size DIP switch is the Time Enable switch. With this switch in the OFF position all the internal live and true timers will be disabled.

Inputs

The Inputs switch selects the number of inputs being used in the system. The inputs switch is an eight position DIP switch which is accessed by removing the right side cover. The Inputs switch allows selections of 1, 2, 4, 8, 16, or 32 inputs. Choose a selection which is closest to but greater than the number of inputs being used in the system. For example, if a total of five inputs are being used then the Inputs switch would be set to 8.

When selecting the number of inputs, keep in mind that the product of the number of inputs and the group size (refer to “Group Size” on page 7) cannot exceed the number of channels in the MCA memory.

One selection on the Inputs switch is the SLAVE position. This is used when expanding a system above 8 inputs. In this type of configuration the first module, the master, would be set to the total number of inputs, 16 or 32, and the remaining modules would be set as slaves.

The number of inputs or slave selections are made by placing the corresponding switch to the ON position. Only one switch may be ON.

Module Number

The Module # switch selects the number assigned to the 8224 module. The Module Number switch is an eight position DIP switch accessed by removing the right side cover. The allowable module numbers are 1 through 4.

When using a single AMX module, its module number must be set to 1. In expanded systems where multiple AMXs are used, each module will have a unique module number, 2 through 4. It is important that the module numbers be assigned in sequence; a number cannot be skipped.

The module number is set by placing both of the corresponding switches to the ON position. Only two switches may be ON.

External Trigger Mode

The External Trigger Mode is analogous to the SVA mode of an ADC. In the External Trigger Mode, the AMX will not process any inputs until a positive pulse is received at the Trigger input BNC. This mode is useful for processing DC or slowly changing inputs or for capturing inputs simultaneously. Each peak detect and hold circuit will store the peak value of the input during the Trigger pulse time.

In expanded systems where multiple AMX modules are to be used in the External Trigger mode, the Trigger pulse must be connected to the Trigger BNC of each module.

When using the External Trigger Mode, the LLD must be set fully counterclockwise and an input provided at the rear panel BNC. The duration between trigger pulses must be long enough to allow all of the inputs to be serviced before a second event is captured. The total service time can be calculated as follows:

$S_T = I\ (A + M + 4\ \mu s)$.

Where:

S_T = Total service time

I = Total number of inputs

A = ADC conversion time in microseconds

M = MCA transfer time in microseconds

For example, in a eight input system using an Accuspec/B board and an 8713 ADC the total service time would be as follows:

$S_T = 8\ (5.9\ \mu s + 2\ \mu s + 4\ \mu s)$

$S_T = 95.2\ \mu s$

Therefore, in this example the period between trigger pulses must be greater than 95.2 µs or approximately 10.5 kHz.

In applications where the Trigger is not used the service time limits the throughput of the system.

Preventive Maintenance

Preventive maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap, side or rear panels.

4. Circuit Description

In this chapter, all negative true signals are shown with a trailing asterisk (TRIG*); all other signals are positive true. Throughout the following circuit description, please refer to the schematics found at the end of the manual.

Peak Detect and Hold

(Refer to B-27799, sheet 2)

The following circuit description refers to the Peak Detect and Hold circuit for input number one. This description is common to remaining seven Peak Detect and Hold Circuits with the exception of the reference designators for the various components.

The Peak Detect and Hold circuit is designed to track the input signal to its peak amplitude, detect that the peak has been reached, store the peak amplitude and inform the scanner logic that an input has been captured. The input signal is presented to the positive input of U60 if the linear gate is open (HOLD0 low). During the positive transition of the input, U60 supplies current through D60 and D63 pin 3 to charge the storage capacitor, C114. When the peak of the input has been reached, D60 and D63 stop conducting current and charging C114; C114 now holds the peak value of the input pulse.

U61 is a unity gain buffer which provides current isolation between the storage capacitor and the circuit output connections. The output of U61 provides feedback to the negative input of U60. When the input falls from its peak value, the output of U60 switches negative trying to force the loop to follow the input. The diodes D60 and D63 are reversed biased and prevent the storage capacitor, C114, from being discharged. When the output of U60 switches negative it also pulls the negative input of U58 negative causing the output, PHD0, to switch high.

Control Logic

(Refer to B-27799, sheet 2)

Again, this description refers to input one but is common to all inputs.

The input signal is compared to the LLD setting, VTH, by U57. When the input signal exceeds the LLD setting, the output of U57, THD0, switches high clocking flip-flop U62A. The output of U62A enables U59C and when PHD0 goes high the signal RDY0* is set true, low. RDY0* presets the hold flip-flop (U62B). HOLD0 closes the linear gate preventing any additional input signals from charging the holding capacitor until after the present input has been serviced. After the ADC has converted the input the scanner logic generates RST0*. RST0* dumps the voltage off of the holding capacitor and resets the threshold (U62A) and Hold (U62B) flip-flops.

Scanner Logic

(Refer to B-27581)

In the 8224, the AMX board (Schematic B-27799) is configured as a slave. Therefore the scanner logic found on sheet 1 of the schematic is not used. Instead the scanning function is performed by logic found on the BMX board (Schematic B-27581).

The Scanner Logic, on schematic sheets 1 and 2, continuously interrogates the Ready signal from each Peak Detect and Hold (PDH) circuit. When the scanner encounters an active Ready signal it stops scanning, connects the output of the PDH to the Signal BNC and generates a GATE pulse to the ADC. At the conclusion of the Accept signal from the MCA the PDH is reset and the scanner continues scanning from where it left off.

The scanner is configured using two 4-bit binary counters, U48 and U49. The terminal count of this counter is determined by the INPUTS DIP switch. For example, if the INPUTS switch is set to 4, the terminal count will be 16. The outputs from U48 and U49 are buffered by U31. The outputs of U31, RSC1*-RSC5*, drive the internal decoders and multiplexers as well as the decoders and multiplexers off any slave units attached to the EXP connector. For this discussion, the AMX board, should also be considered a slave. If a unit is configured as a slave the outputs of U31 (U30 on the AMX) in the slave are tri-stated eliminating any contentions on the Expansion bus.

Scan lines 1, 2 and 3, RSC1*-RSC3*, are used to select 1 of 8 inputs to the Analog Mux, U47, and the multiplexer, U28, both on the AMX. The inputs to the Analog Mux are the analog outputs from each PDH circuit. The output of the Analog Mux is buffered by U63 on the AMX which drives the Signal BNC. The inputs to the multiplexer are the Ready signals from each of the control logic circuits for the individual PDH's. The output of the multiplexer, RDYX, will be high if the Ready signal of the input being interrogated is true.

RDYX being high will set RDYD*, U58A, true on the next positive transition of CLK*. RDYD* disables the scanner until the ADC and the MCA have processed the input as directed by the ACEPT* signal. The negative transition of HOLD*, U58B, produces a negative going pulse approximately 1 µs wide at the GATE BNC (sheet 3) which is used to start the ADC conversion cycle. ACEPT* clears the RDYD and Hold flip-flops by CLRD* thereby allowing the scanner to continue to the next input.

The Reset Scanner, U29 on the AMX, generates a reset, RST0*-RST7*, to the appropriate PDH circuit as determined by SC1*-SC3*. At the end of the MCA cycle, CLRD is set true which in turn sets AMX Reset, AMXRST*, true. AMXRST* is routed to the appropriate PDH circuit by U29 on the AMX.

The Ready Scanner U28, the Reset Scanner U29 and the Analog Mux U47 on the AMX all have a common enabling input Select AMX, SLTAMX*. Scan lines 4 and 5, RSC4*-RSC5* and RSCTIM* (Remote Scan Timer), drive the three-line to eight-line decoder U59. The outputs of U59, generate the SLTAMX* and SLTAMT* signals based on the setting of the MODULE # switch.

The routing address generation and buffering is performed by U26 through U29. The setting of the GROUP SIZE switch enables one of the buffers, U26-U29. The inputs to the buffers are the address lines from the ADC and the scan lines. Based on the GROUP SIZE switch setting, the address lines presented to the MCA are a combination of the address lines from the ADC and the scan lines. For example, if the Group Size is 2K then the ADC address lines ADC00 through ADC10 are presented to the MCA. In addition RSC1* through RSC5* will generate MCA11* through MCA15* respectively. In this way the scan lines route the conversion from an input to the appropriate memory group in the MCA.

Independent Start/Stop Control

(Refer to B-27581, sheet 1)

The inputs on the PI connector are latched by U7 with the rising edge of the RSCTIM* (Remote Scan Timer) signal. The output of the latch is buffered by U5. The buffer U5 is enabled by the Enable Convertor (ENC*) signal from the MCA providing MCA control of the 8224 acquisition. The output of the latch also provides input to the data multiplexer, U6. The output of U6, ACQX*, indicates when the input being interrogated is enabled. If the input is not enabled, ACQX* high, the signals SLTAMX* and SLTAMT* are inhibited, causing the scanner to disregard that input.

True Timers

(Refer to B-27581, sheet 4)

Each input has a True Timer, consisting of a 12-bit asynchronous counter, assigned to it. The output of this counter toggles at a period of one second.

On the negative transition of the counter's output a flip-flop is set, generating the Real Time Flag (RTFG0-7) signal. The eight flags are scanned by U23 on sheet 1. When an active flag is encountered, the RDYX signal is generated and the scanner performs a storage cycle as if an input had been captured. The difference between a time storage cycle and a captured pulse storage cycle is the source of the address. For time storage cycles, the address is generated by U16, sheet 2, causing the True Time storage to occur at channel zero of the appropriate group.

Each True Timer can be enabled/disabled by the corresponding ACQ0*-ACQ7* signal from U5. When ACQ is high, the 12-bit counter is held reset inhibiting True Time storage.

Live Timers

(Refer to B-27581, sheet 5)

Each input has a Live Timer assigned to it. Each live timer consists of two 12-bit counters. The output of the second counter will set a flip-flop on its negative transition. The outputs of these flip-flops, Live Time Flag (LTFG0-7) are scanned by U42 on sheet 1. The output of U42 will generate an RDYX signal and storage will occur in channel one of the appropriate memory group as described in the True Timer description (see "True Timers" on page 13).

The input to each Live Timer is the LTCLK signal, an 8.38 MHz clock. LTCLK is gated with BSYD0-7, which is active high whenever the PHD of the input has captured a pulse and requires servicing.

As in the True Timer circuit, the Live Timers are also controlled by ACQ0*-ACQ7*.

Power Supplies

(Refer to B-27799, sheet 6)

Three 3-terminal regulators provide the voltages required by the 8224 AMX. Q101 which is mounted to the rear panel of the module, supplies the +5 volts. VR1 and VR2 supply +15 volts and –15 volts, respectively.

A. Specifications

Inputs

INPUT - Accepts positive unipolar or initially positive bipolar pulses from a spectroscopy amplifier (one amplifier per input) in the PHA Mode or dc levels or pulses in the External Trigger Mode. Amplitude 0 to +10 V, +12 V max; rise time 0.25 to 100 µs; Z_{in}=1 kΩ; front panel BNC connectors.

TRIGGER - Accepts positive TTL level pulse which causes all inputs to capture peak voltage during trigger; pulse width 2 µs, minimum; high amplitude ≥4.5 V, low amplitude ≤+0.5 V, -0.5 to +5.5 V, max; Z_{in}=2.2 kΩ; rear panel BNC connector.

PI - Provides connection for a parallel interface in the associated MCA system for individual start/stop control; TTL compatible inputs; high or open input enables; rear panel 20-pin ribbon cable connector.

ADC - Accepts binary output from the ADC; rear panel 34-pin ribbon cable connector.

Outputs

SIGNAL - Provides 0 to +10 V output pulses to ADC SIGNAL input; front panel BNC.

GATE - Provides negative-going TTL pulse; high amplitude ≥3.8 V at 4 mA, low amplitude ≤0.3 V at 4 mA; width 1 µs; front panel BNC.

MCA - Provides the ADC's binary output and appended routing bits to the MCA; TTL compatible output levels; rear panel 34-pin ribbon cable connector.

EXP - Provides connection for additional 8224 modules when the system is expanded; rear panel 20-pin ribbon cable connector. A maximum of four 8224's can be connected to provide 32 inputs.

Controls

INPUTS - Board mounted DIP switch, accessible by removing side panel, provides selection of the number of groups in binary increments from 1 to 32.

GROUP SIZE - Board mounted DIP switch, accessible by removing side panel, provides selection of group size in binary increments from 256 to 8K channels.

MODULE NUMBER - Board mounted DIP switch, accessible by removing side panel, provides selection of module number, 1 to 4, in expanded systems.

LLD - Front panel screwdriver adjusted single-turn potentiometer sets the lower level discriminator threshold for all eight inputs; range –150 mV to 800 mV.

Indicators

BUSY - Front panel LED indicators vary in intensity relative to the activity of the corresponding INPUT.

ENABLED - Front panel LED indicates when the corresponding INPUT is enabled by the individual start/stop control circuits and MCA.

Performance

NUMBER OF INPUTS - Up to eight per 8224 module; up to four 8224's may be connected for multiplexing up to 32 inputs.

PRIORITY - Equal priority for all inputs via scanning technique.

INPUT SCANNING RATE - 500 kHz.

INPUT GAIN VARIATION - <2% from any input to any other input.

INPUT ZERO VARIATION - <10 mV from any input to any other input.

PDH DROOP - 1.3 V/s, typical; 4.3 V/s, maximum.

ACQUISITION CONTROL - Each input can be individually turned on or off via signals available on a rear panel connector. These signals, which are logically ANDed with the ENC signal from the MCA, can be controlled manually or by computer interface.

LIVE TIME CLOCK - Eight counters, one for each input; 8.388 MHz gated clock drives 2^{23} prescaler; second channel of each spectral group is updated (add-one) every live second; live time for each group is defined as the total time the linear gate for that group is open.

REAL TIME CLOCK - Eight counters, one for each input; 4.096 kHz clock drives 2^{12} prescaler; first channel of each spectral group is updated (add-one) every second that its respective input is enabled.

CLOCK STABILITY - ±0.01%.

INTEGRAL NONLINEARITY - Typically <±0.025% over top 99.5% of full scale.

Power requirements

+12 V dc – 500 mA +24 V dc – 250 mA

–24 V dc – 250 mA

Accessories

C1703-2 Cable - 60 cm (2 ft) 34-pin ribbon to ribbon cable provided for connection to the 8700 series NIM ADCs.

751622 Cable - Optional 45 cm (1.5 ft) AMX expansion cable; one required for each expansion AMX.

840617 Interface Kit Option - PC slot manifold, 1.8 m (6 ft) ribbon cable and 759618 breakout cable for AccuSpec A or NaI.

840618 Interface Kit Option - PC slot manifold, 4.6 m (15 ft) ribbon cable and 759618 breakout cable for AccuSpec A or NaI.

Independent Start/Stop options

AIM Systems - Require the Model 554 Remote Parallel Interface (RPI) and the Model 751684 Interface Cable for independent start/stop. Each RPI supports two cables and each cable supports 16 inputs.

AccuSpec B and MC Systems - Require an LPT Interface and the Model 751776 Interface Cable to support a single AMX. Independent start/stop of multiple 8224's requires the Model 820763 Interface Kit, which controls up to 32 inputs, for AccuSpec B Systems or the Model 820766 Interface Kit, which controls up to 24 inputs, for AccuSpec MC Systems.

Physical

SIZE - Standard double width NIM module 6.86 X 22.12 cm (2.70 X 8.71 in.) per DOE/ER-00457T.

NET WEIGHT - 1.5 kg (3.2 lb).

SHIPPING WEIGHT - 2.4 kg (5.2 lb).

Environmental

OPERATING TEMPERATURE - 0 to 40 °C.

RELATIVE HUMIDITY - Up to 80%, non-condensing

Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution Degree 2.

B. Rear Panel Connectors

This chapter lists the details of the 8224's PC-mounted and rear panel interface connectors.

MCA Interface Connector

This 34-pin ribbon connector provides all the necessary signals for connection to the MCA. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

Pin	Signal	Pin	Signal
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	Reserved
7	GND	8	ENC* or ENC
9	GND	10	MREADY*
11	GND	12	INBX*
13	MCA13*2	14	ADC00*1
15	ADC07*1	16	ADC01*1
17	MCA08*	18	ADC02*1
19	MCA09*	20	ADC03*1
21	MCA10*	22	ADC04*1
23	MCA11*	24	ADC05*1
25	MCA12*	26	ADC06*1
27	MCA14*	28	MCA15*
29	BF*1	30	VGAIN
31	BLLD1	32	VZERO
33	BCB*1	34	MCA13X*

[1] These signals are not used by the AMX but are passed through to or from the ADC connector.

[2] This pin may be connected to ground by moving W1 to W2.

Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts

High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts

High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

Signal	Pin	Description
ADC00*	14	OUTPUT: Binary data 2^0 (LSB)
ADC01*	16	OUTPUT: Binary data 2^1
ADC02*	18	OUTPUT: Binary data 2^2
ADC03*	20	OUTPUT: Binary data 2^3
ADC04*	22	OUTPUT: Binary data 2^4
ADC05*	24	OUTPUT: Binary data 2^5
ADC06*	26	OUTPUT: Binary data 2^6
ADC07*	15	OUTPUT: Binary data 2^7
MCA08*	17	OUTPUT: Binary data 2^8
MCA09*	19	OUTPUT: Binary data 2^9
MCA10*	21	OUTPUT: Binary data 2^{10}
MCA11*	23	OUTPUT: Binary data 2^{11}
MCA12*	25	OUTPUT: Binary data 2^{12}

MCA13*	13	OUTPUT: Binary data 2^{13}
MCA13x*	34	OUTPUT: Binary data 2^{13} Alternate
MCA14*	27	OUTPUT: Binary data 2^{14}
MCA15*	28	OUTPUT: Binary data 2^{15} (MSB)
GND	1, 3, 5, 7, 9, 11	DC common for all interface signals
ENDATA*	4	INPUT (Enable Data): Used to enable the tri-state buffers driving the 16-bits of data onto the output lines ADC00* through ADC07* and MCA08* through MCA15*.
MREADY*	10	OUTPUT (Data Ready): Indicates that data is available for transfer to the MCA. MREADY* is generated by the ADC. MREADY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	INPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may be reset when READY* resets (handshake).
INBX*	12	OUTPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer cycle must be completed, the data itself should be discarded by the MCA.
ENC* or ENC	8	INPUT (Enable Converter): This signal enables or disables the ADC and AMX modules. A jumper option in the ADC and AMX allows selection of polarity. ENC = logic 1 enables ADC and AMX operation.
BF*	29	OUTPUT: This signal is set true at peak detect time and remains true until the leading edge of ACEPT*. This signal is meaningful in the NON-OVERLAP mode of the ADC only.
BCB*	33	OUTPUT: This signal is set true at peak detect time and remains true until READY* is set true. It represents the conversion time of the internal ADC.
BLLD	31	OUTPUT: this signal is set true when the input pulse rises above the ADC Threshold level and remains true until the trailing edge of ACEPT*.

VZERO (analog)	32	INPUT: This analog signal controls the ADC zero; it is normally provided by the spectrum stabilizer.
VGAIN (analog)	30	INPUT: This analog signal controls the ADC gain; it is normally provided by the spectrum stabilizer.

ADC Interface Connector

This 34-pin ribbon connector provides all the necessary signals for connection to the ADC. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

Pin	Signal	Pin	Signal
1	GND	2	ACEPT*
3	GND	4	ENDATAX*
5	GND	6	Reserved
7	GND	8	ENC* or ENC
9	GND	10	READY*
11	GND	12	INB* (INV*)
13	Reserved	14	ADC00*1
15	ADC07*1	16	ADC01*1
17	ADC08*	18	ADC02*1
19	ADC09*	20	ADC03*1
21	ADC10*	22	ADC04*1
23	ADC11*	24	ADC05*1
25	ADC12*	26	ADC06*1
27	Reserved	28	Reserved
29	BF*1	30	VGAIN1
31	BLLD1	32	VZERO1
33	BCB*1	34	Reserved

[1] These signals are not used by the AMX but are passed through to or from the MCA connector.

Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts

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And the output signal levels are:

Low = 0 to 0.5 volts

High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

Signal	Pin	Description
ADC00*	14	INPUT: Binary data 2^0 (LSB)
ADC01*	16	INPUT: Binary data 2^1
ADC02*	18	INPUT: Binary data 2^2
ADC03*	20	INPUT: Binary data 2^3
ADC04*	22	INPUT: Binary data 2^4
ADC05*	24	INPUT: Binary data 2^5
ADC06*	26	INPUT: Binary data 2^6
ADC07*	15	INPUT: Binary data 2^7
ADC08*	17	INPUT: Binary data 2^8
ADC09*	19	INPUT: Binary data 2^9
ADC10*	21	INPUT: Binary data 2^{10}
ADC11*	23	INPUT: Binary data 2^{11}
ADC12*	25	INPUT: Binary data 2^{12} (MSB)

ENDATAX*	4	OUTPUT (Enable Data): Used to enable the tri-state buffers driving the 14 bits of data onto the output lines ADC00* through ADC12*.
READY*	10	INPUT (Data Ready): Indicates that data is available for transfer to the MCA. READY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	OUTPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may reset when READY* resets (handshake).
INB*	12	INPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer cycle must be completed, the data itself should be discarded by the MCA.
ENC* or ENC	8	OUTPUT (Enable Converter): This signal enables or disables the ADC module. A jumper option in the ADC allows selection of polarity. ENC = logic 1 enables ADC operation. ENC = logic 0 prevents the ADC from reopening the linear gate thereby inhibiting further operation.
BF*	29	INPUT: This signal is set true at peak detect time and remains true until the leading edge of ACEPT*. This signal is meaningful in the NON-OVERLAP mode only.
BCB*	33	INPUT: This signal is set true at peak detect time and remains true until READY* is set true. It represents the conversion time of the internal ADC.
BLLD	31	INPUT: This signal is set true when the input pulse rises above the ADC Threshold level and remains true until the trailing edge of ACEPT*.
VZERO (analog)	32	OUTPUT: This anlog signal controls the ADC zero; it is normally provided by the spectrum stabilizer.
VGAIN (analog)	30	OUTPUT: This analog signal controls the ADC gain; it is normally provided by the spectrum stabilizer.
GND	1,3,5,7,9,11	DC common for all interface signals.

EXP Connector

This 20-pin ribbon connector provides the necessary signals to interface a master AMX to a slave AMX. Negative true signals are shown with a trailing asterisk (AMXRST*); all other signals are positive true.

Pin	Signal	Pin	Signal
1	GND	2	BAMXRST*
3	GND	4	VMA
5	GND	6	BRSCTIM*
7	GND	8	BRSC5*
9	GND	10	BRSC4*
11	GND	12	BRSC3*
13	GND	14	BRSC2*
15	GND	16	BRSC1*
17	ENC*	18	RDYX*
19	LTUDX*	20	BAMXBSY*

Signal Functions

This section describes the function of each interface signal in detail. All signals except VMA are TTL compatible. If the AMX is configured as a Master then all the signals except VMA and RDYX are outputs; VMA and RDYX are inputs. If the AMX is configured as a slave then the opposite is true, VMA and RDYX are outputs; all other signals are inputs. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts

High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts

High = 3.0 to 5.0 volts

Signal	Pin	Description
BAMXRST*	2	AMX Reset. This signal is generated by the master AMX. BAMXRST* resets the Peak Detect and Hold logic of the input being serviced.
VMA	4	This signal is the analog voltage captured by the PDH circuit of the input being service.
BRSC1*	16	Remote scan line 1 (LSB). Scanner output from the master AMX.
BRSC2*	14	Remote scan line 2
BRSC3*	12	Remote scan line 3
BRSC4*	10	Remote scan line 4
BRSC5*	8	Remote scan line 5
BRSCTIM*	6	Remote Timer Scan line.
RDYX*	18	External Ready. This signal indicates that the input presently being interrogated by the scanner has captured an input event and requires service.
BAMXBSY*	20	AMX Busy. This signal indicates that the scanner has stopped and is waiting for the input service to be completed; converted by the ADC and accepted by the MCA.
LTUDX*	19	Live Time Update External: This signal is active (low) when the time transfer being performed is Live Time data and not True Time.
ENC*	17	Enable Converter: This signal enables or disables the AMX.
GND	1, 3, 5, 7, 9, 11, 13, 15	DC common for all interface signals.

PI Connector

This 20-pin ribbon connector provides the necessary input signals to independently start/stop each input.

Pin	Signal	Pin	Signal
1	SSI1	2	SSI2
3	SSI3	4	SSI4
5	SSI5	6	SSI6
7	SSI7	8	SSI8
9	GND	10	Reserved
11	GND	12	Reserved
13	GND	14	Reserved
15	GND	16	Reserved
17	GND	18	Reserved
19	GND	20	Reserved

Signal Functions

This section describes the function of each interface signal in detail. All signals on this connector are inputs. The input signal levels are:

Low = 0 to 1.0 volts

High = 2.0 to 5.0 volts

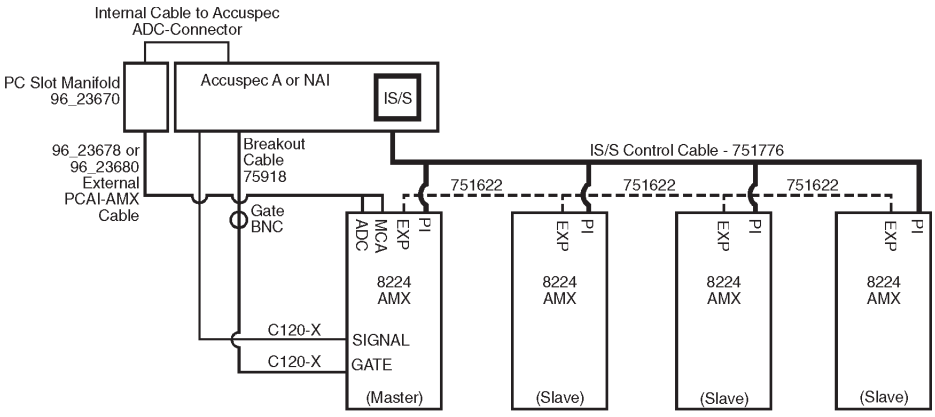
Signal	Pin	Description
SSI	1	Start Stop Input 1: This signal enables/disables the servicing of Input 1. A high or open level enables; a low level disables.
SSI2	2	Start Stop Input 2
SSI3	3	Start Stop Input 3
SSI4	4	Start Stop Input 4
SSI5	5	Start Stop Input 5
SSI6	6	Start Stop Input 6
SSI7	7	Start Stop Input 7
SSI8	8	Start Stop Input 8

GND	9, 11, 13, 15, 17, 19	DC common for all interface signals.

Trigger Connector

The Trigger BNC connector accepts a positive TTL level pulse with a minimum width of 2 sec. This signal will cause all the Peak Detect and Hold circuits to capture the peak voltage at the input during the trigger pulse.

C. Setup Diagrams



Accuspec A or NAI MCA and ADC Connections AMXs
Requires Interface Kit 840617 or 840618 to be purchased. These kits contain the 96_23678 or 96_23680 external PCAI-AMX cable, the 759618 breakout cable for the Gate Connection, and the 96_23670 PC slot manifold.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable which must be purchased separately.

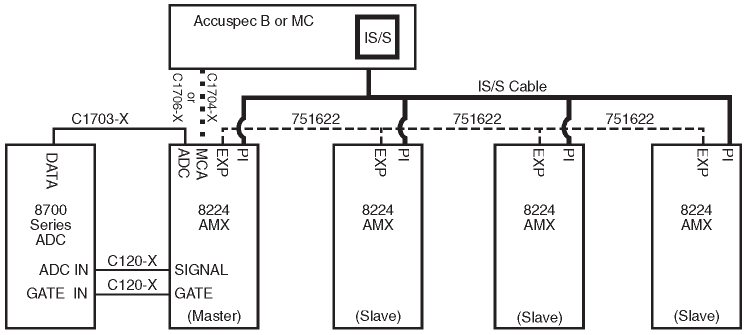
Independent Start/Stop for the 8224 AMX
Independent Start/Stop control of more than one 8224 requires Kit 820763 to be purchased. This kit contains a control board and the control cable assembly needed to control up to four 8224s. A 751776 IS/S Control Cable and a parallel port (LPT) may be used also for Independent Start/Stop control of a single 8224.

Note: The number of 8224's supported is limited by the software platform being used. Please refer to the appropriate manual for information.

Jumper Settings
8224
J1 - ENC*
W1 - Installed
W2 - Removed

Accuspec A or NaI
J1 - J8 - Removed
PHA/STB - SVB
GATE/$\overline{\text{GATE}}$ - $\overline{\text{GATE}}$

Figure 4 8224 Setup With AccuSpec A or NaI



ADC-AMX Connections
Each 8224 AMX is supplied with one C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

Accuspec B or MC Board to AMX Connection
Each Accuspec B or MC Board is supplied with one C1704-10 Interface Cables.

AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable which must be purchased separately.

Independent Start/Stop for the 8224 AMX
Kit 820763 contains the control board and the control cable assembly required for Independent Start/Stop control of one to four 8224s with an Accuspec B Board.

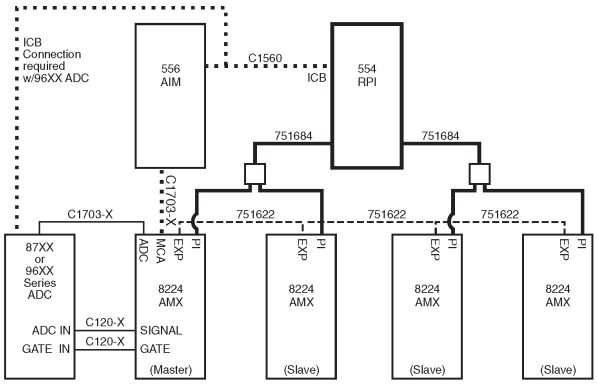
Kit 820766 contains the control board and the control cable assembly required for Independent Start/Stop control of one to three 8224s with an Accuspec MC Board.

A 751776 Control Cable may be used with a parallel port (LPT) to control a single 8224 with either the Accuspec B or MC Board.

Note: The number of 8224's supported is limited by the software platform being used. Please refer to the appropriate manual for information.

8224	8701	8706	8713/8715
J1 - ENC*	J1 - ENC*	J4 - B	W3 - B
W1 - Installed	J3 - NEG	J5 - ENC*	W6 - B
W2 - Removed	J6 - OVLP*	J7 - OVLP*	W8 - B
	J8 - B	J9 - NEG	PHA/SVA - SVA
	PHA/SVA - SVA	PHA/SVA - SVA	AUTO/DELAYED - DELAYED
	AUTO/DELAYED - DELAYED	AUTO/DELAYED - DELAYED	COINC/ANTI - COINC
	COINC/ANTI - COINC	COINC/ANTI - COINC	ADJ - Full CCW
	ADJ - Full CCW	ADJ - Full CCW	

Figure 5 8224 Setup AccuSpec B or MC



ADC-AMX Connections
Each 8224 AMX is supplied with one C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

AIM-AMX Connection
Each AIM is supplied with two C1703-2 Interface Cables and one C1560 cable.

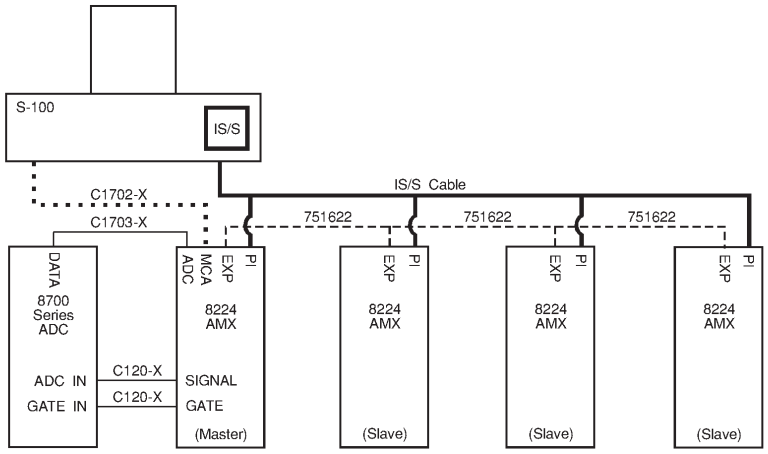
AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable that must be purchased separately.

Independent Start/Stop for the 8224 AMXs
This option requires the purchase of a Model 554 Remote Parallel Interface (RPI) and at least one 751684 cable assembly. Each 751684 Cable Assembly supports two 8224s and each RPI supports 2 such cable assemblies.

Note: The number of 8224's supported is limited by the software platform being used. Please refer to the appropriate manual for information.

8224	8701	8706	8713/8715	9633/9635
J1 - ENC*	J1 - ENC*	J4 - B	W3 - B	W3 - B
W1 - Removed	J3 - NEG	J5 - ENC*	W6 - B	W8 - B
W2 - Installed	J6 - OVLP*	J7 - OVLP*	W8 - B	PHA/SVA - SVA
	J8 - B	J9 - NEG	PHA/SVA - SVA	COINC/ANTI - COINC
	PHA/SVA - SVA	PHA/SVA - SVA	AUTO/DELAYED - DELAYED	Xfer Timing-Nonoverlap
	AUTO/DELAYED - DELAYED	AUTO/DELAYED - DELAYED	COINC/ANTI - COINC	Peak Detect-Delay
	COINC/ANTI - COINC	COINC/ANTI - COINC	ADJ - Full CCW	ADJ - Full CCW
	ADJ - Full CCW	ADJ - Full CCW		

Figure 6 8224 Setup With 556 AIM



ADC-AMX Connections
Each 8224 AMX is supplied with a C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

System 100 Board to 8224 AMX Connection
Each System 100 Board is supplied with one C1704-4 Interface Cable.

AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable, which must be purchased separately.

Independent Start/Stop for the 8224 AMX
Kit 820763 contains the control board and the control cable assembly required for Independent Start/Stop control of one to four 8224s with an Accuspec B Board.

Kit 820766 contains the control board and the control cable assembly required for Independent Start/Stop control of one to three 8224s with an Accuspec MC Board.

A 751776 Control Cable may be used with a parallel port (LPT) to control a single 8224 with either the Accuspec B or MC Board.

Note: The number of 8224's supported is limited by the software platform being used. Please refer to the appropriate manual for information.

8224	8701	8706	8713/8715
J1 - ENC	J1 - ENC	J4 - B	W3 - A
W1 - Installed	J3 - POS	J5 - ENC	W8 - A
W2 - Removed	J8 - B	J9 - POS	PHA/SVA - SVA
	PHA/SVA - SVA	PHA/SVA - SVA	AUTO/DELAYED - DELAYED
	AUTO/DELAYED - DELAYED	AUTO/DELAYED - DELAYED	COINC/ANTI - COINC
	COINC/ANTI - COINC	COINC/ANTI - COINC	ADJ - Full CCW
	ADJ - Full CCW	ADJ - Full CCW	

Figure 7 8224 Setup With System 100

D. Installation Considerations

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- A rack or tabletop enclosure fully closed on all sides with rear door access
- Single point external cable access
- Blank panels to cover open front panel Bin area
- Compliant grounding and safety precautions for any internal power distribution
- The use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance with the specified EU requirements.

Notes

Warranty

Canberra (we, us, our) warrants to the customer (you, your) that for a period of ninety (90) days from the date of shipment, software provided by us in connection with equipment manufactured by us shall operate in accordance with applicable specifications when used with equipment manufactured by us and that the media on which the software is provided shall be free from defects. We also warrant that (A) equipment manufactured by us shall be free from defects in materials and workmanship for a period of one (1) year from the date of shipment of such equipment, and (B) services performed by us in connection with such equipment, such as site supervision and installation services relating to the equipment, shall be free from defects for a period of one (1) year from the date of performance of such services.

If defects in materials or workmanship are discovered within the applicable warranty period as set forth above, we shall, at our option and cost, (A) in the case of defective software or equipment, either repair or replace the software or equipment, or (B) in the case of defective services, reperform such services.

LIMITATIONS

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EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident, neglect or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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