Model 8223
Analog Multiplexer

07/92

User's Manual

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1. Introduction

The 8223 AMX Module allows multiplexing of up to eight analog input signals through a single ADC. Multiplexing provides a cost effective method of handling a large number of low count rate input signals with one ADC and is ideal for environmental analysis and alpha spectroscopy applications. With additional 8223 modules, up to 64 input signals per ADC can be handled simultaneously. When used with a fast ADC, such as the Model 8715 800 ns Fixed Dead Time ADC, the 8223 provides a cost effective multiple input capability with good count rate performance.

The 8223 contains one PDH (Peak Detect and Hold) circuit for each of the eight input signals. These analog memory circuits hold the peak value of each input pulse as a dc voltage level. The 8223's internal logic continuously scans the status of the eight PDH circuits at a scanner rate of 1.25 MHz. When one of the PDH circuits captures a pulse, the scanner stops and connects the PDH to the ADC input. The 8223 then generates a gate pulse which initiates the ADC conversion cycle. When the conversion is complete, scanning resumes. Each event processed by the ADC is automatically routed into the associated memory group by appending routing bits to the digital ADC output word.

Each of the eight inputs to the 8223 is assigned a specific group size. For example, if the MCA is configured to provide 8192 channels of memory, data from input signal 1 is stored in the first 1024 channel group, data from input signal 2 is stored in the second 1024 channel group, and so on. This results in eight individual spectra, each representing one input signal, effectively simulating an individual ADC processing each input.

Internal DIP switches allow the user to select the group size, number of active inputs, module number assignment and master/slave designation of each 8223 in a system. These switches are accessible by removing the module's side panel.

LLD adjustment for all eight input signals is provided by a common front panel control.

Since the 8223 does not provide individual clock counters for live time control, only external real time group presetting is available.

Analog multiplexing can be performed in an external trigger mode which allows processing of dc voltage levels applied to the 8223's inputs. In this mode, each time a positive trigger signal arrives at the rear panel Trigger input, the 8223 takes a snapshot of the voltage levels in all active inputs. One event is acquired in each group with each trigger signal.

2. Controls and Connectors

2.1. Front Panel

This is a brief description of the 8223's front panel controls and connectors. For more detailed information, refer to Appendix A, Specifications.

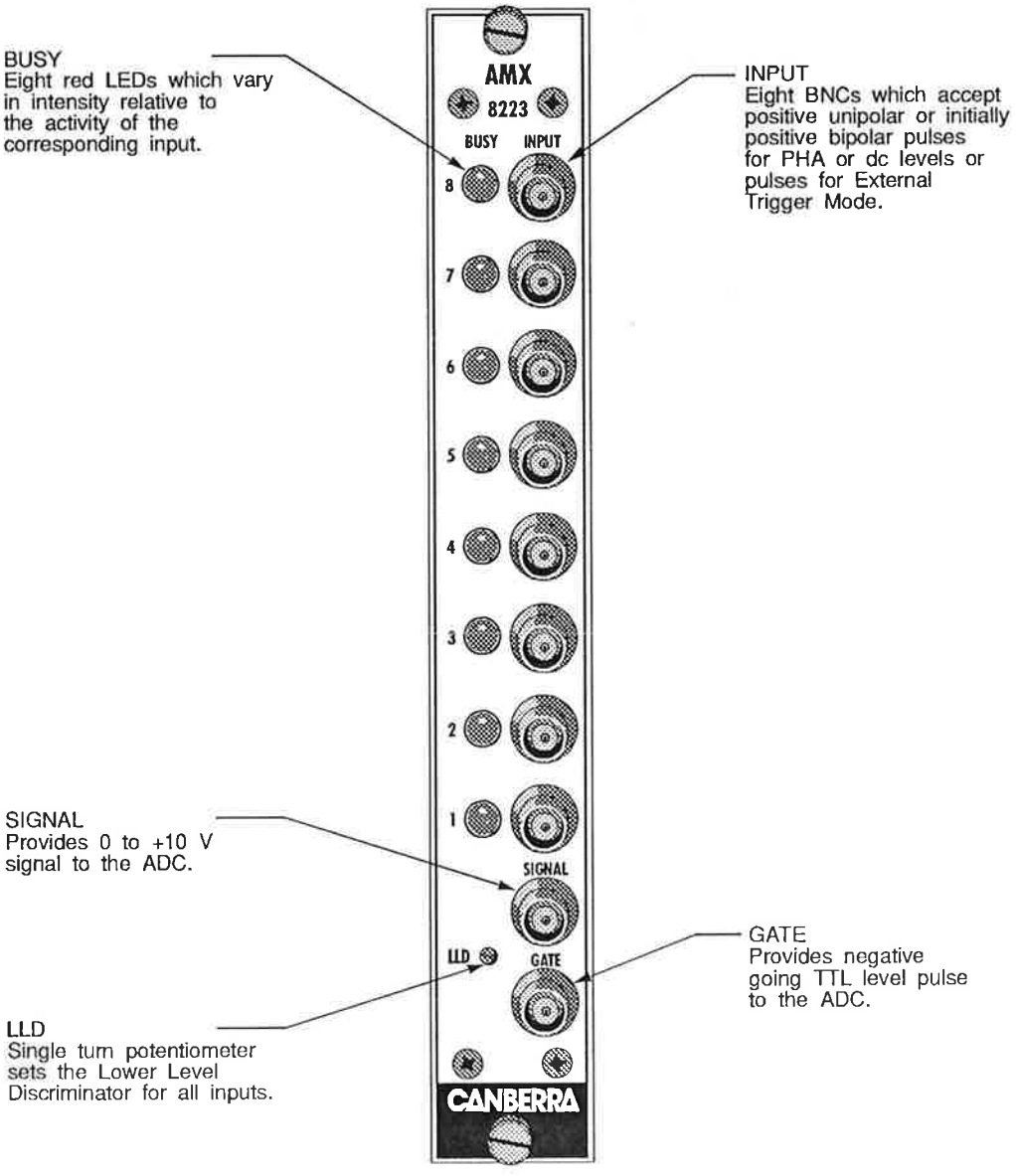


Figure 2.1 Front Panel Controls

2.2. Rear Panel

This is a brief description of the 8223's rear panel connectors. For more detailed information, refer to Appendix A, Specifications.

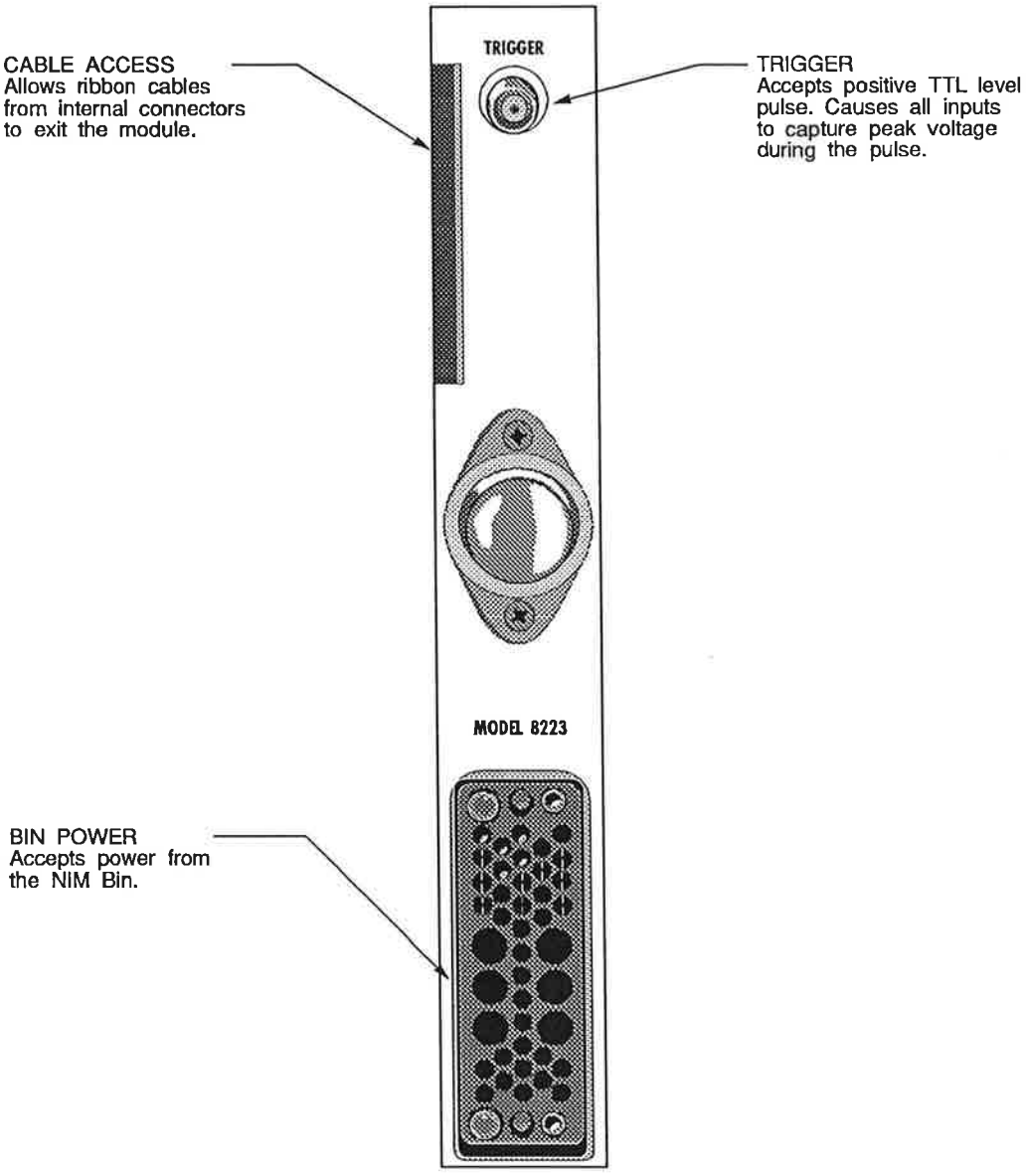


Figure 2.2 Rear Panel Controls

2.3. Internal Controls

The internal jumper plug controls should be set for your specific requirements before applying power to the module.

The factory default jumper settings are:

Inputs – 8
Module no. – 1
Group size – 512

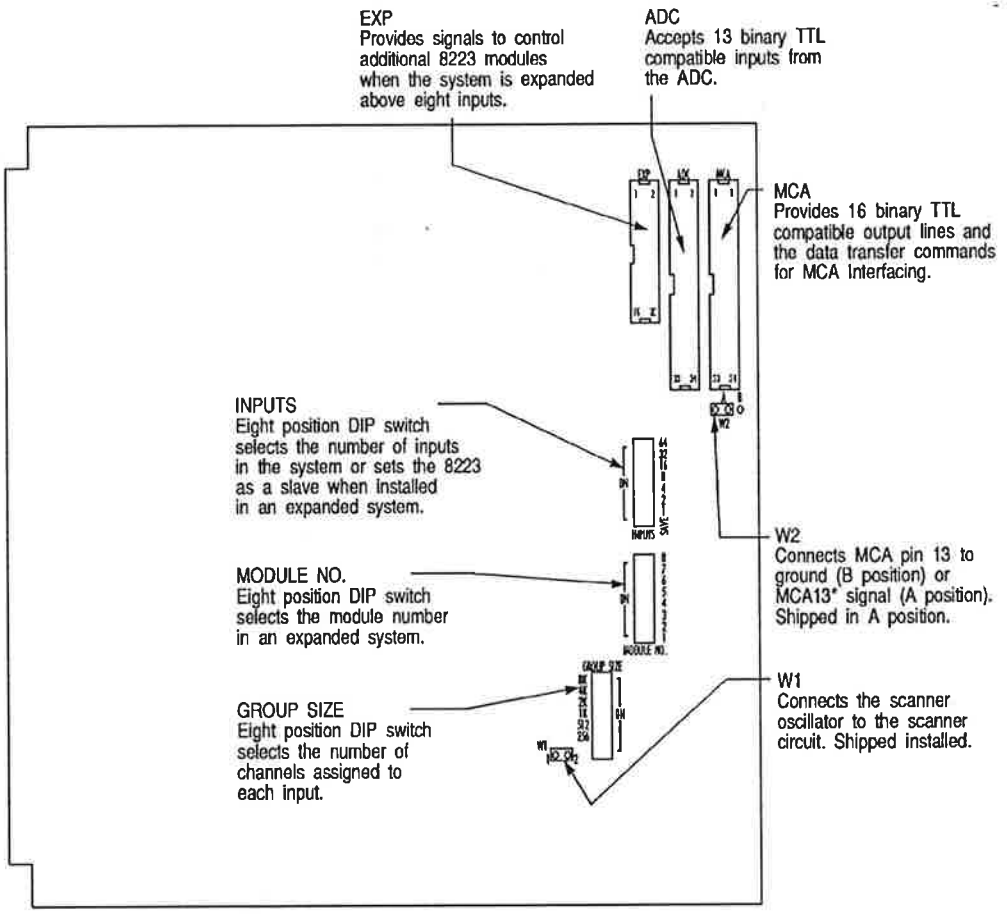


Figure 2.3 Internal Controls

3. Operation

The following sections discuss the use of the 8223 and its internal and external controls.

3.1. Setting up the 8223

The 8223 connects between the ADC and the MCA and multiplexes up to eight signal sources into the ADC. The 8223 stores the peak voltage of each input signal. Each peak voltage is sequentially connected to the ADC and a Gate pulse is generated by the 8223 which causes the ADC to convert that voltage. The second function of the 8223 is to append routing bits to the address from the ADC and then present the modified address to the MCA for storage.

One 8223 can accommodate up to eight inputs. If more than eight inputs are required then the system can be expanded to 64 inputs by adding additional 8223's which are configured as slaves. In an expanded system one 8223 is configured as the master and is the only 8223 connected to the ADC and the MCA. The remaining 8223's are configured as slaves and are connected to the master through the EXP connector.

The 8223 is configured by three internal DIP switches; Module Number, Group Size and Inputs. In order to determine the proper settings for these switches, two factors must be known. First, the number of inputs required. The number of inputs is set on the Inputs DIP switch (Section 3.4). The second is the number of channels in the MCA memory. This value divided by the number of inputs will determine the setting for the Group Size switch (Section 3.3). The Module Number switch is used in expanded systems where the Master is configured as module number 1 and each slave is configured with a unique module number, 2 through 8 (Section 3.5).

The 8223 is connected to the ADC through the internal ADC connector and to the MCA through the internal MCA connector. The 8223 is also connected to the ADC's Signal In and Gate In BNC. For details on the proper cable and connections refer to Appendix C.

All interface signals required between the ADC and the MCA are passed through the 8223 with the exception of the Dead Time (CDT). The 8223 does not support Live Time correction therefore quantitative analysis is not possible. For applications where Live Time correction is required the Model 8224 AMX is recommended. The 8224 has individual Live and True timers for each input.

3.2. LLD

The Lower Level Discriminator (LLD) is a front panel potentiometer that sets the lower limit for the input signals to be accepted by the AMX for processing. The LLD setting is common to all eight of the AMX inputs. The input signal must exceed the LLD setting before it will be captured and stored by the Peak detector and hold circuit.

When operating the AMX in the External Trigger mode, the LLD must be set fully CCW.

3.3. Group Size

The Group Size switch selects the number of channels assigned to each input. The Group Size switch is an eight position DIP switch which is accessed by removing the right side cover. The allowable group sizes are 256, 512, 1K, 2K, 4K and 8K.

When selecting the group size, it is important to keep two factors in mind. The first is that the product of the group size and number of inputs (Section 3.4) cannot exceed the number of channels in the MCA memory. Second, the group size should match the range of the ADC. The group size is selected by placing the corresponding switch to the ON position. Only one switch may be ON at a time.

3.4. Inputs

The Inputs switch selects the number of inputs being used in the system. The inputs switch is an eight position DIP switch which is accessed by removing the right side cover. The Inputs switch allows selections of 1, 2, 4, 8, 16, 32 or 64 inputs. Choose a selection which is closest to but greater than the number of inputs being used in the system. For example, if a total of five inputs are being used then the Inputs switch would be set to 8.

When selecting the number of inputs, keep in mind that the product of the number of inputs and the group size (Section 3.3) cannot exceed the number of channels in the MCA memory.

One selection on the Inputs switch is the SLAVE position. This is used when expanding a system above 8 inputs. In this type of configuration the first module, the master, would be set to the total number of inputs, 16, 32 or 64, and the remaining modules would be set as slaves.

The number of inputs or slave selections is made by placing the corresponding switch to the ON position. Only one switch may be ON.

3.5. Module No.

The Module Number switch selects the number assigned to the 8223 module. The Module Number switch is an eight position DIP switch accessed by removing the right side cover. The allowable module numbers are 1 through 8.

When using a single AMX module, its module number must be set to 1. In expanded systems where multiple AMXs are used, each module will have a unique module number, 2 through 8. It is important that the module numbers be assigned in sequence; a number cannot be skipped.

The module number is set by placing the corresponding switch to the ON position. Only one switch may be ON.

3.6. External Trigger Mode

The External Trigger Mode is analogous to the SVA mode of an ADC. In the External Trigger Mode, the AMX will not process any inputs until a positive pulse is received at the Trigger input BNC. This mode is useful for processing DC or slowly changing inputs or for capturing inputs simultaneously. Each peak detect and hold circuit will store the peak value of the input during the Trigger pulse time.

In expanded systems where multiple AMX modules are to be used in the External Trigger mode, the Trigger pulse must be connected to the Trigger BNC of each module.

When using the External Trigger Mode, the LLD must be set fully counterclockwise and an input provided at the rear panel BNC. The duration between trigger pulses must be long enough to allow all of the inputs to be serviced before a second event is captured. The total service time can be calculated as follows:

$$S_T = I\,(A + M + 2.8\,\mu s).$$

Where:

S_T = Total service time
I = Total number of inputs
A = ADC conversion time in microseconds
M = MCA transfer time in microseconds

For example, in a eight input system using an Accuspec/B board and an 8713 ADC the total service time would be as follows:

$$S_T = 8\,(5.9\,\mu s + 2\,\mu s + 2.8\,\mu s)$$
$$S_T = 85.6\,\mu s$$

Therefore, in this example the period between trigger pulses must be greater than 85.6 μs or approximately 12 kHz.

In applications where the Trigger is not used the service time limits the throughput of the system.

4. Theory of Operation

In this chapter, all negative true signals are shown with a trailing asterisk (TRIG*); all other signals are positive true. Throughout the following circuit description, please refer to the schematics found at the end of the manual.

4.1. Peak Detect and Hold

The following circuit description refers to the Peak Detect and Hold circuit for input number one. This description is common to remaining seven Peak Detect and Hold Circuits with the exception of the reference designators for the various components.

The Peak Detect and Hold circuit is designed to track the input signal to its peak amplitude, detect that the peak has been reached, store the peak amplitude and inform the scanner logic that an input has been captured. The input signal is presented to the positive input of U60 if the linear gate is open (HOLD0 low). During the positive transition of the input, U60 supplies current through D60 and D63 pin 3 to charge the storage capacitor, C114. When the peak of the input has been reached, D60 and D63 stop conducting current and charging C114; C114 now holds the peak value of the input pulse.

U61 is a unity gain buffer which provides current isolation between the storage capacitor and the circuit output connections. The output of U61 provides feedback to the negative input of U60. When the input falls from its peak value, the output of U60 switches negative trying to force the loop to follow the input. The diodes D60 and D63 are reversed biased and prevent the storage capacitor, C114, from being discharged. When the output of U60 switches negative it also pulls the negative input of U58 negative causing the output, PHD0, to switch high.

4.2. Control Logic

Again, this description refers to input one but is common to all inputs.

The input signal is compared to the LLD setting, VTH, by U57. When the input signal exceeds the LLD setting, the output of U57, THD0, switches high clocking flip-flop U62A. The output of U62A enables U59C and when PHD0 goes high the signal RDY0* is set true, low. RDY0* presets the hold flip-flop (U62B). HOLD0 closes the linear gate preventing any additional input signals from charging the holding capacitor until after the present input has been serviced. After the ADC has converted the input the scanner logic generates RST0*. RST0* dumps the voltage off of the holding capacitor and resets the threshold (U62A) and Hold (U62B) flip-flops.

4.3. Scanner Logic

The Scanner Logic, on schematic sheet 1, continuously interrogates the Ready signal from each Peak Detect and Hold (PDH) circuit. When the scanner encounters an active Ready signal it stops scanning, connects the output of the PDH to the Signal BNC and generates a GATE pulse to the ADC. At the conclusion of the Accept signal from the MCA the PDH is reset and the scanner continues scanning from where it left off.

The scanner is configured using two 4-bit binary counters, U49 and U50. The terminal count of this counter is determined by the INPUTS DIP switch. For example, if the INPUTS switch is set to 4, the terminal count will be 8. The outputs from U49 and U50 are buffered by U30. The outputs of U30, SC1*-SC6*, drive the internal decoders and multiplexers as well as the decoders and multiplexers off any slave units attached to the EXP connector. If a unit is configured as a slave the outputs of U30 in the slave are tri-stated eliminating any contentions on the Expansion bus.

Scan lines 1, 2 and 3, SC1*-SC3*, are used to select 1 of 8 inputs to the Analog Mux, U47, and the multiplexer, U28. The inputs to the Analog Mux are the analog outputs from each PDH circuit. The output of the Analog Mux is buffered by U63 which drives the Signal BNC. The inputs to the multiplexer are the Ready signals from each of the control logic circuits for the individual PDH's. The output of the multiplexer, RDYX, will be high if the Ready signal of the input being interrogated is true.

RDYX being high will set HOLD, U65, true on the next positive transition of SC0. HOLD* disables the scanner until the ADC and the MCA have processed the input as directed by the ACEPT* signal. ACEPT* clears the Hold flip-flop by CLRD* thereby allowing the scanner to continue to the next input. The positive transition of HOLD produces a negative going pulse approximately 1 μs wide at the GATE BNC which is used to start the ADC conversion cycle.

The Reset Scanner, U29, generates a reset, RST0*-RST7*, to the appropriate PDH circuit as determined by SC1*-SC3*. At the end of the MCA cycle, CLRD is set true which in turn sets AMX Reset, AMXRST*, true. AMXRST* is routed to the appropriate PDH circuit by U29.

The Ready Scanner U28, the Reset Scanner U29 and the Analog Mux U47 all have a common enabling input Select AMX, SLTAMX*. Scan lines 4, 5 and 6, SC4*-SC6*, drive the three-line to eight-line decoder U48. The outputs of U48, Select 0 through 7 (SLT0*-SLT7*), generate the SLTAMX* signal based on the setting of the MODULE NO. switch.

The routing address generation and buffering is performed by U31, U32 and U64. The setting of the GROUP SIZE Switch is converted to a 3-bit code by U64. This code is presented to the PAL U31. U31 uses the code to determine which address bits from the ADC, ADC8*-ADC12*, are passed along to the MCA. U31 also appends routing bits to the ADC address as determined by the input being serviced. The input information is a function of the scan lines SC1-SC6. The output of U31 provides the MCA address line, MCA8-MCA15. These address lines are buffered by U32.

4.4. Power Supplies

Three 3-terminal regulators provide the voltages required by the 8223 AMX. Q101 which is mounted to the rear panel of the module, supplies the +5 volts. VR1 and VR2 supply +15 volts and –15 volts, respectively.

A. Specifications

A.1. Inputs

INPUT - Accepts positive unipolar or initially positive bipolar pulses from a spectroscopy amplifier (one amplifier per input) in the PHA Mode or dc levels or pulses in the External Trigger Mode. Amplitude 0 to +10 V, +12 V max; rise time 0.25 to 100 μs; Z_{in} = 1 kΩ; front panel BNC connectors.

TRIGGER - Accepts positive TTL level pulse which causes all inputs to capture peak voltage during trigger; pulse width 2 μs, minimum; high amplitude $\geq$4.5 V, low amplitude $\leq$ +0.5 V, -0.5 to +5.5 V, max; Z_{in} = 2.2 kΩ; rear panel BNC connector.

ADC - Accepts binary output from the ADC; pc mounted 34-pin ribbon cable connector.

A.2. Outputs

SIGNAL - Provides 0 to +10 V output pulses to ADC SIGNAL input; front panel BNC.

GATE - Provides negative-going TTL pulse; high amplitude $\geq$3.8 V at 4 mA, low amplitude $\leq$0.3 V at 4 mA; width 1 μs; front panel BNC.

MCA - Provides the ADC's binary output and appended routing bits to the MCA; TTL compatible output levels; pc mounted 34-pin ribbon cable connector.

EXP - Provides connection for additional 8223 modules when the system is expanded; pc mounted 20-pin ribbon cable connector. A maximum of eight 8223's can be connected to provide 64 inputs.

A.3. Controls

INPUTS - Board mounted DIP switch, accessible by removing side panel, provides selection of the number of groups in binary increments from 1 to 64.

GROUP SIZE - Board mounted DIP switch, accessible by removing side panel, provides selection of group size in binary increments from 256 to 8K channels.

MODULE NUMBER - Board mounted DIP switch, accessible by removing side panel, provides selection of module number, 1 to 8, in expanded systems.

LLD - Front panel screwdriver adjusted single-turn potentiometer sets the lower level discriminator threshold for all eight inputs; range –150 mV to 800 mV.

A.4. Indicators

BUSY - Front panel red LED indicators vary in intensity relative to the activity of the corresponding INPUT.

A.5. Performance

NUMBER OF INPUTS - Up to eight per 8223 module; up to eight 8223's may be connected for multiplexing up to 64 inputs.

PRIORITY - Equal priority for all inputs via scanning technique.

INPUT SCANNING RATE - 1.25 MHz.

INPUT GAIN VARIATION - < 2% from any input to any other input.

INPUT ZERO VARIATION - < 10 mV from any input to any other input.

PDH DROOP - 1.3 V/s, typical; 4.3 V/s, maximum.

ACQUISITION CONTROL - All inputs are started and stopped together.

INTEGRAL NONLINEARITY - Typically < ±0.025% over top 99.5% of full scale.

OPERATING TEMPERATURE RANGE - 0 TO 40 °C.

A.6. Power Requirements

+12 V dc – 100 mA +24 V dc – 250 mA
–24 V dc – 250 mA

A.7. Accessories

C1703-2 Cable - 60 cm (2 ft) 34-pin ribbon to ribbon cable provided for connection to the 8700 series NIM ADCs.

751622 Cable - Optional 45 cm (1.5 ft) AMX expansion cable; one required for each expansion AMX.

840617 Interface Kit Option - PC slot manifold and 1.8 m (6 ft) 759618 breakout cable for AccuSpec A or NaI.

840618 Interface Kit Option - PC slot manifold and 4.6 m (15 ft) 759618 breakout cable for AccuSpec A or NaI.

A.8. Physical

SIZE - Standard single width NIM module 3.43 X 22.12 cm (1.35 X 8.71 in) per DOE/ER-00457T.

NET WEIGHT - 0.9 kg (1.9 lb).

SHIPPING WEIGHT - 1.8 kg (4.0 lb).

B. Rear Panel Connectors

This chapter lists the details of the 8223's PC-mounted and rear panel interface connectors.

B.1. MCA Interface Connector

This 34-pin ribbon connector provides all the necessary signals for connection to the MCA. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	Reserved
7	GND	8	ENC* or ENC[1]
9	GND	10	READY*[1]
11	GND	12	INB* (INV*)[1]
13	MCA13*[2]	14	ADC00*[1]
15	ADC07*[1]	16	ADC01*[1]
17	MCA08*	18	ADC02*[1]
19	MCA09*	20	ADC03*[1]
21	MCA10*	22	ADC04*[1]
23	MCA11*	24	ADC05*[1]
25	MCA12*	26	ADC06*[1]
27	MCA14*	28	MCA15*
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	Reserved*	34	MCA13X*

[1]These signals are not used by the AMX but are passed through to or from the ADC connector.

[2]This pin may be connected to ground by moving W2 to the B position.

B.1.1 Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

SIGNAL	PIN	DESCRIPTION
ADC00*	14	OUTPUT: Binary data 2^0 (LSB)
ADC01*	16	OUTPUT: Binary data 2^1
ADC02*	18	OUTPUT: Binary data 2^2
ADC03*	20	OUTPUT: Binary data 2^3
ADC04*	22	OUTPUT: Binary data 2^4
ADC05*	24	OUTPUT: Binary data 2^5
ADC06*	26	OUTPUT: Binary data 2^6
ADC07*	15	OUTPUT: Binary data 2^7
MCA08*	17	OUTPUT: Binary data 2^8
MCA09*	19	OUTPUT: Binary data 2^9
MCA10*	21	OUTPUT: Binary data 2^{10}
MCA11*	23	OUTPUT: Binary data 2^{11}
MCA12*	25	OUTPUT: Binary data 2^{12}
MCA13*	13	OUTPUT: Binary data 2^{13}
MCA13X*	34	OUTPUT: Binary data 2^{13}, alternate
MCA14*	27	OUTPUT: Binary data 2^{14}
MCA15*	28	OUTPUT: Binary data 2^{15} (MSB)
GND	1, 3, 5, 7, 9, 11	DC common for all interface signals
ENDATA*	4	INPUT (Enable Data): Used to enable the tri-state buffers driving the 16-bits of data onto the output lines ADC00* through ADC07* and MCA08* through MCA15*.
READY*	10	OUTPUT (Data Ready): Indicates that data is available for transfer to the MCA. READY* is generated by the ADC. READY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	INPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may be reset when READY* resets (handshake).
INB*	12	OUTPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer cycle must be completed, the data itself should be discarded by the MCA.

ENC* or ENC	8	INPUT (Enable Converter): This signal enables or disables the ADC module. A jumper option in the ADC allows selection of polarity. ENC = logic 1 enables ADC operation. ENC = logic 0 prevents the ADC from reopening the linear gate thereby inhibiting further operation.

B.2. ADC Interface Connector

This 34-pin ribbon connector provides all the necessary signals for connection to the ADC. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	Reserved
7	GND	8	ENC* or ENC[1]
9	GND	10	READY*[1]
11	GND	12	INB* (INV*)[1]
13	Reserved	14	ADC00*[1]
15	ADC07*[1]	16	ADC01*[1]
17	MCA08*	18	ADC02*[1]
19	MCA09*	20	ADC03*[1]
21	MCA10*	22	ADC04*[1]
23	MCA11*	24	ADC05*[1]
25	MCA12*	26	ADC06*[1]
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	Reserved*	34	Reserved

[1]These signals are not used by the AMX but are passed through to or from the MCA connector.

B.2.1 Signal Functions

This section describes the function of each interface signal in detail. All input and output signals are TTL compatible. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

All input and output signals considered to be a logic 1 for a high voltage level unless the signal name is followed by an asterisk (*), in which case the signal is considered to be a logic 1 for a low voltage level.

SIGNAL	PIN	DESCRIPTION
ADC00*	14	INPUT: Binary data 2^0 (LSB)
ADC01*	16	INPUT: Binary data 2^1
ADC02*	18	INPUT: Binary data 2^2
ADC03*	20	INPUT: Binary data 2^3
ADC04*	22	INPUT: Binary data 2^4
ADC05*	24	INPUT: Binary data 2^5
ADC06*	26	INPUT: Binary data 2^6
ADC07*	15	INPUT: Binary data 2^7
ADC08*	17	INPUT: Binary data 2^8
ADC09*	19	INPUT: Binary data 2^9
ADC10*	21	INPUT: Binary data 2^{10}
ADC11*	23	INPUT: Binary data 2^{11}
ADC12*	25	INPUT: Binary data 2^{12} (MSB)
ENDATA*	4	OUTPUT (Enable Data): Used to enable the tri-state buffers driving the 13 bits of data onto the input lines ADC00* through ADC12*.
READY*	10	INPUT (Data Ready): Indicates that data is available for transfer to the MCA. READY* will be reset after receipt of signal ACEPT*.
ACEPT*	2	INPUT (Data Accepted): Signals the ADC that the data has been accepted by the MCA. ACEPT* may reset when READY* resets (handshake).
INB*	12	INPUT (Inhibit): This signal indicates that the data available for transfer to the MCA is invalid and, although the data transfer cycle must be completed, the data itself should be discarded by the MCA.
ENC* or ENC	8	OUTPUT (Enable Converter): This signal enables or disables the ADC module. A jumper option in the ADC allows selection of polarity. ENC = logic 1 enables ADC operation. ENC = logic 0 prevents the ADC from reopening the linear gate thereby inhibiting further operation.
GND	1,3,5,7,9,11	DC common for all interface signals.

B.3. EXP Connector

This 20-pin ribbon connector provides the necessary signals to interface a master AMX to a slave AMX. Negative true signals are shown with a trailing asterisk (AMXRST*); all other signals are positive true.

Pin	Signal	Pin	Signal
1	GND	2	AMXRST*
3	GND	4	VMA
5	GND	6	RSC6*
7	GND	8	RSC5*
9	GND	10	RSC4*
11	GND	12	RSC3*
13	GND	14	RSC2*
15	GND	16	RSC1*
17	Reserved	18	RDYX
19	Reserved	20	AMXBSY*

B.3.1 Signal Functions

This section describes the function of each interface signal in detail. All signals except VMA are TTL compatible. If the AMX is configured as a Master then all the signals except VMA and RDYX are outputs; VMA and RDYX are inputs. The AMX is configured as a slave then the opposite is true, VMA and RDYX are outputs; all other signals are inputs. Unless otherwise noted, the input signal levels are:

Low = 0 to 1.0 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

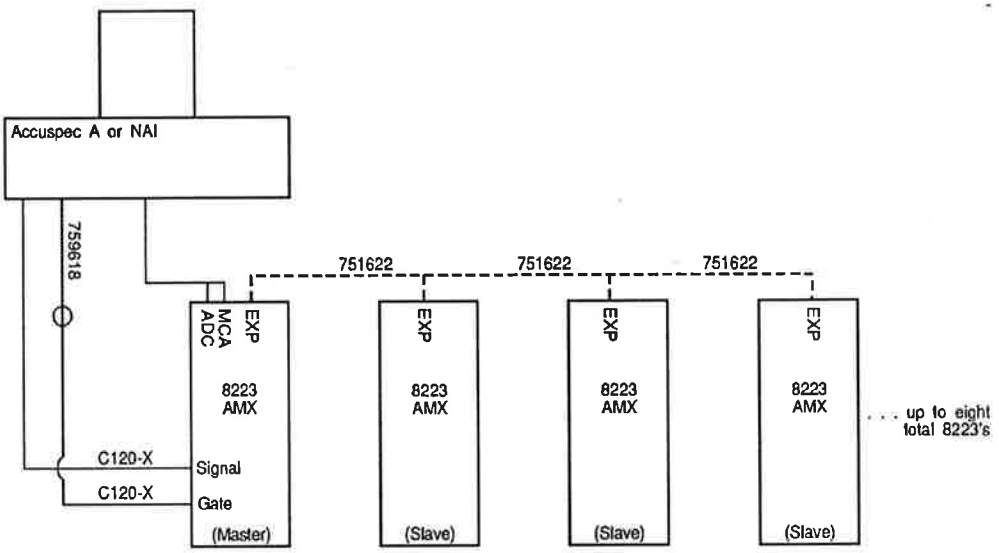
SIGNAL	PIN	DESCRIPTION
AMXRST*	2	AMX Reset. This signal is generated by the master AMX. AMXRST* resets the Peak Detect and Hold logic of the input being serviced.
VMA	4	This signal is the analog voltage captured by the PDH circuit of the input being service.
RSC1*	16	Remote scan line 1 (LSB). Scanner output from the master AMX.
RSC2*	14	Remote scan line 2
RSC3*	12	Remote scan line 3
RSC4*	10	Remote scan line 4

RSC5*	8	Remote scan line 5
RSC6*	6	Remote scan line 6
RDYX	18	External Ready. This signal indicates that the input presently being interrogated by the scanner has captured an input event and requires service.
AMXBSY*	20	AMX Busy. This signal indicates that the scanner has stopped and is waiting for the input service to be completed; converted by the ADC and accepted by the MCA.
GND	1, 3, 5, 7, 9, 11, 13, 15	DC common for all interface signals.

B.4. TRIGGER Connector

The Trigger BNC connector accepts a positive TTL level pulse with a minimum width of 2 sec. This signal will cause all the Peak Detect and Hold circuits to capture the peak voltage at the input during the trigger pulse.

C. Setup Diagrams



——— **Accuspec A or NAI MCA and ADC Connections AMXs**
Requires Interface Kit 840617 or 840618 to be purchased. These kits contain the MCA-ADC to AMX interface cable assembly and the 759818 breakout cable for the Gate Connection.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

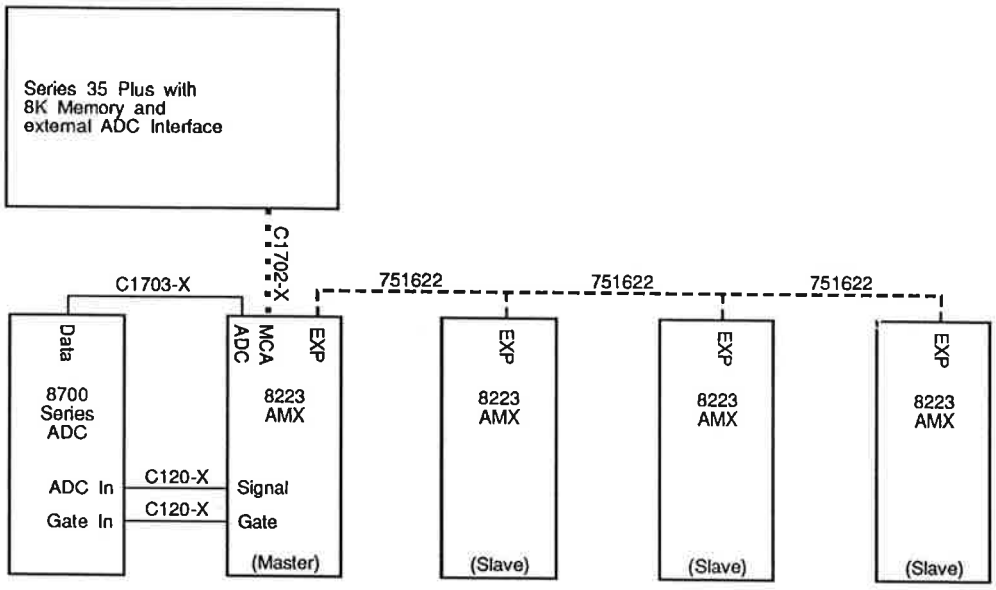
----- **AMX Master-Slave Connection**
Each slave requires a 751622 Expansion Cable that must be purchased separately.

Jumper Settings
8223
w1 - installed
w2 - A

Accuspec A or Nal
J1 - J8 - Removal
PHA/STB - STB
GATE/$\overline{\text{GATE}}$ - $\overline{\text{GATE}}$

Figure C.1

Figure C.1 8223 Setup With AccuSpec A or Nal



ADC-AMX Connections
Each 8223 AMX is supplied with a C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

Series 35 Plus MCA to 8223 AMX Connection
Each Series 35 Plus MCA with an external ADC Interface is supplied with one or more C1702-4 Interface Cables.

AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable, which must be purchased separately.

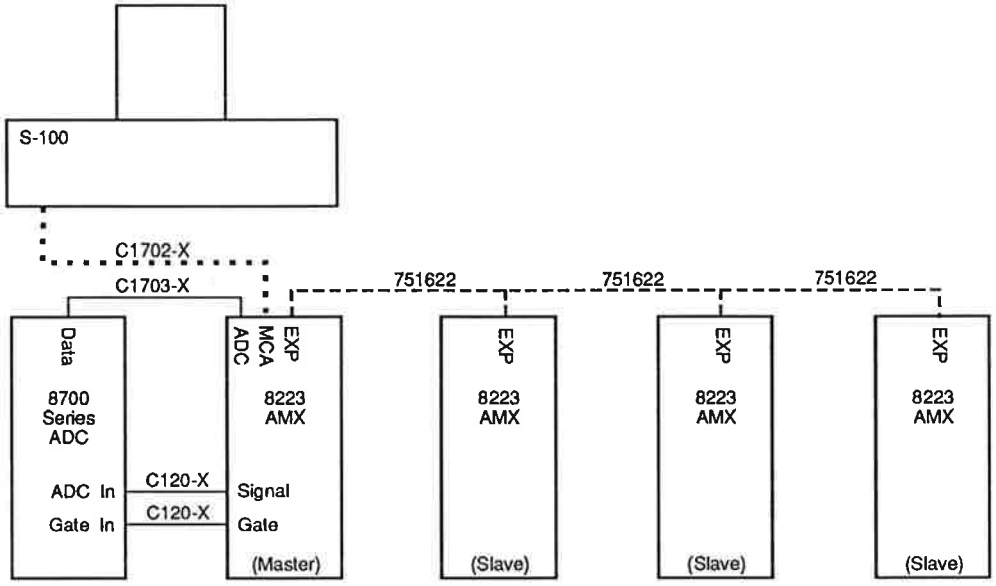
8223 Jumpers
- W1 - installed
- W2 - A

8701
- J1 - ENC
- J3 - POS
- J8 - B
- PHA/SVA - SVA
- AUTO/DELAYED - DELAYED
- COINC/ANTI - COINC
- ADJ - Full CCW

8706
- J4 - B
- J5 - ENC
- J9 - POS
- PHA/SVA - SVA
- AUTO/DELAYED - DELAYED
- COINC/ANTI - COINC
- ADJ - Full CCW

8713/8715
- W3 - A
- W8 - A
- PHA/SVA - SVA
- AUTO/DELAYED - DELAYED
- COINC/ANTI - COINC
- ADJ - Full CCW

Figure C.2 8223 Setup With Series 35 Plus



——— **ADC-AMX Connections**
Each 8223 AMX is supplied with a C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

• • • • • **System 100 Board to 8223 AMX Connection**
Each System 100 Board is supplied with one C1702-4 Interface Cable.

– – – – – **AMX Master-Slave Connection**
Each slave requires a 751622 Expansion Cable, which must be purchased separately.

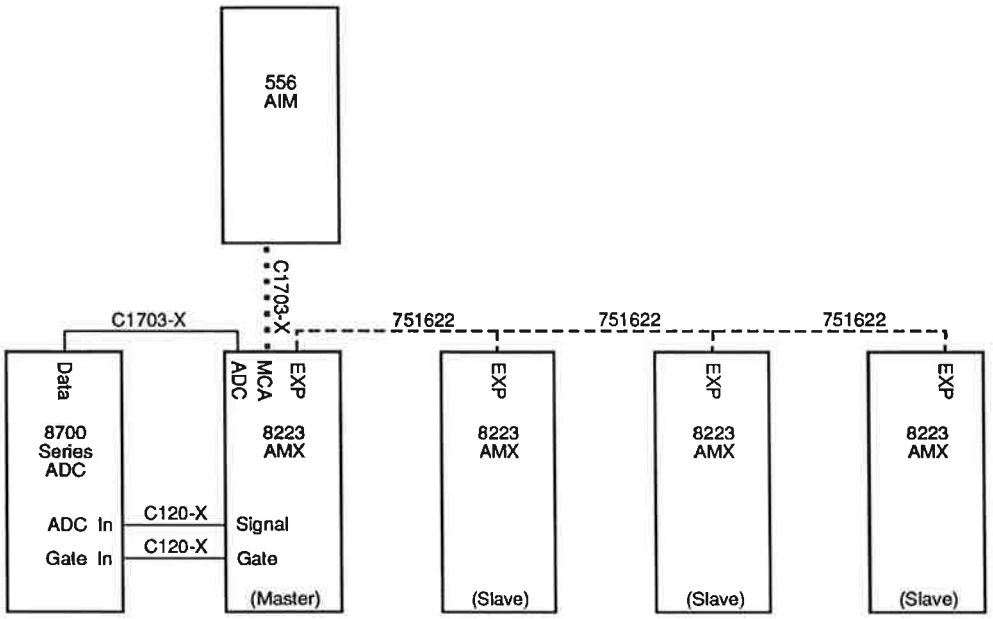
8223 Jumpers
W1 - installed
W2 - At

8701
J1 - ENC
J3 - POS
J8 - B
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

8706
J4 - B
J5 - ENC
J9 - POS
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

8713/8715
W3 - A
W8 - A
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

Figure C.3 8223 Setup With System 100



ADC-AMX Connections
Each 8223 AMX is supplied with one C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

AIM-AMX Connection
Each AIM is supplied with two C1703-2 Interface Cables.

AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable, which must be purchased separately.

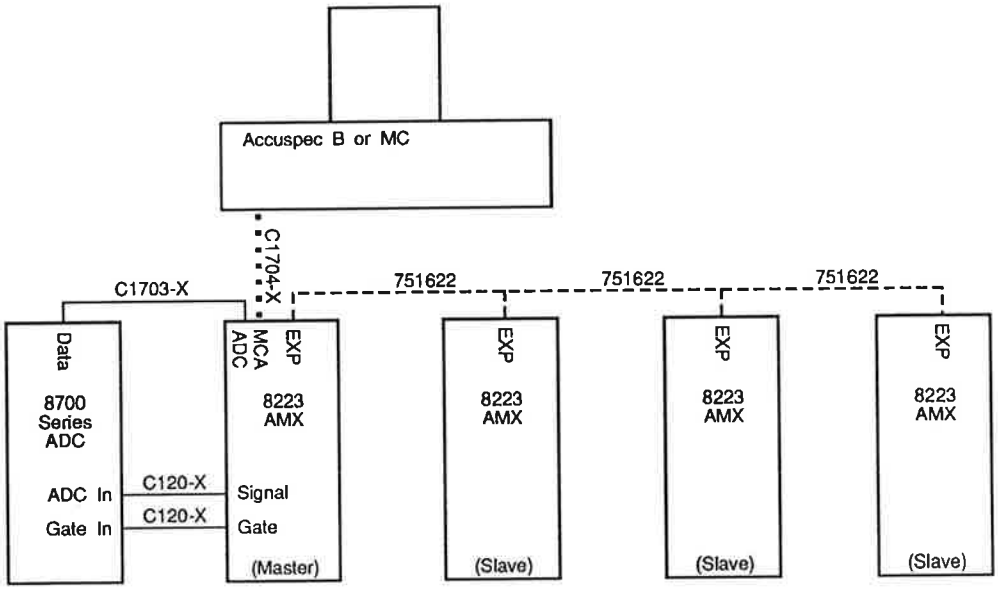
8223 Jumpers
W1 - Installed
W2 - B

8701
J1 - ENC*
J3 - POS
J8 - B
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

8706
J4 - B
J5 - ENC*
J9 - NEG
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

8713/8715
W3 - B
W8 - B
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

Figure C.4 8223 Setup With 556 AIM



——— **ADC-AMX Connection**
Each 8223 AMX is supplied with a C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

▪ ▪ ▪ ▪ ▪ **Accuspec B or MC Board to AMX Connection**
Each Accuspec B or MC Board is supplied with one C1704-10 Interface Cable.

– – – – – AMX Master-Slave **Connection**
Each slave requires a 751622 Expansion Cable, which must be purchased separately.

8223 Jumpers
W1 - installed
W2 - B

8701
J1 - ENC*
J3 - POS
J8 - B
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

8706
J4 - B
J5 - ENC*
J9 - NEG
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

8713/8715
W3 - B
W8 - B
PHA/SVA - SVA
AUTO/DELAYED - DELAYED
COINC/ANTI - COINC
ADJ - Full CCW

Figure C.5 8223 Setup With AccuSpec B or MC

CANBERRA

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