FAST ANALOG-TO-DIGITAL CONVERTER
Model 8077

0885

Operator's Manual

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

M183R2 8/85 Printed in U.S.A.

Table of Contents

FIGURE LISTING

Section 1. Introduction

1.1 DESCRIPTION

The Canberra Model 8077 is a single-width NIM analog-to-digital converter for applications in nuclear and X-ray spectroscopy. This unit incorporates a Wilkinson type, 450 MHz clock rate, counter/ramp-converter optimized for high count rates, high resolution and low differential nonlinearity performance. The ADC also includes an internal data buffer which allows the ADC to begin a second conversion prior to MCA acceptance of the first. For 8K conversion gain, the ADC will digitize a 10 volt input in less than 18.1 μsec and in statistical applications such as spectroscopy, the average conversion time is less than 6.1 μsec. When compared to conventional 100 MHz ADCs, the 8077 has a throughput advantage of over 4.5 times.

A direct-coupled input of 0 to +10 V is digitized according to the front panel GAIN control into binary code spans of 9 through 14 bits (512 through 16 384 channels). The concentric RANGE control may be used to limit the maximum digital output count to less than the full scale set by the GAIN control. This is useful when data is to be transferred to a memory unit with a smaller capacity than the overflow limit of the selected gain range. The user may expand an analog input region for finer gain analysis by using a high GAIN setting and selecting appropriate digital OFFSET in any desired combination of the 6 front-panel toggle switches.

The Model 8077 includes a 10-turn locking-dial precision potentiometer for the Lower Level Discriminator (LLD) with a range of 0.02 to 10 V dc, and a screwdriver-adjusted 22-turn Upper Level Discriminator (ULD) with a range of 0.02 to 10.5 V dc nominal. The front panel ZERO adjustment is also a 22-turn screwdriver-adjusted potentiometer; its setting can be monitored on the adjacent CAL test point and covers ±5% of full scale input range.

Conversion for the Pulse Height Analysis (PHA) mode can be initiated AUTOmatically using an internal constant-fraction peak detector operating on the trailing edge of the input pulse, or can be delayed up to 100 μsec using the DELAYED mode. A front panel INSPect test point is provided so that the user can monitor the Linear Gate (LG), time between LLD crossing and the beginning of conversion for either mode. Conversions may be enabled/disabled by the COINCidence/ ANTIcoincidence gating applied at any time during the Linear Gate interval.

Conversion for the Sample Voltage Analysis (SVA) mode is initiated by the falling edge of a GATE pulse applied in the COINCidence mode. The same LLD and ULD limits are used for acceptance of an input level for conversion in this mode.

The Model 8077 is compatible with all Canberra MCAs using the external ADC options designated for each unit. This instrument is also compatible with the Canberra Model 8222 Mixer/Router and, with the exception of 16K conversion gain, with the Model 8634 for multiple parameter studies. A separate 25-pin STABILIZER output connector on the rear panel interfaces with the Model 8232 Digital Stabilizer for use in system setups requiring gain stabilization. An additional 3-pin pileup rejector (PUR) connector is provided on the rear panel for direct interface to the Canberra Model 2020 Amplifier which includes pileup rejection circuitry.

Section 2. Specifications

2.1 INPUTS

ADC IN - Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 μsec maximum; width 0.5 μsec minimum; input impedance 1k ohm, direct coupled; front panel BNC and test point.

GATE IN - Accepts positive logic pulse or dc level; amplitude $\geq$ 2.5 to 7 V maximum; dc coupled; with COINCidence or SVA selected loading $\leq$ -100 μA at +3 V and $\leq$ +800 μA for ANTIcoincidence; width $\geq$ 250 nsec; PHA analysis does not require a gate input. For SVA, pulse width $\geq$ 1 μsec.

2.2 OUTPUTS

DATA - Provides 14 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 26-pin Ansley connector and 1.2 meter (4 foot) mating cable with Amphenol type (17-10250) connector. Data lines are negative true as standard.

STABILIZER - Provides 14 binary TTL-compatible lines and the trigger commands required for the Model 8232 Digital Stabilizer; rear panel 26-pin Ansley connector. Data lines are negative true. Stabilizer Control range for ±5 V input and 1k source impedance; zero: ±2%; gain: ±5%.

PILEUP REJECTOR/LIVE TIME CORRECTOR - Accepts REJECT and Live Time signals from Canberra Model 2020 Amplifier, also provides Linear Gate to that unit for full interactive operation; rear panel 3-pin Molex connector for use with Molex Cable, Model C1514.

REJect - Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur and remain stable until the ADC Linear Gate (LG) Signal concludes; amplitude ≥ 2.5 to 7 V; width ≥ 50 nsec; loading ≤ +800 μA at +3 V. Accessible through pin 2 of rear panel PUR connector.

LG - Provides a negative true logic signal; logic low when ADC accepts input, returns to a logic high at the ADC acquisition cycle conclusion. TTL compatible totem pole output (LS) through 47 ohm series resistor. Accessible through pin 1 of rear panel PUR connector.

DEAD TIME - Rear panel BNC connector having a dual-function capability; external dead time INPUT or ADC dead time OUTPUT; one of these modes is internally selected with jumper plug J9; shipped in the NEG INput position. When used as:

NEG INput - Accepts a negative logic signal which is ORed with the ADC dead time, the composite dead time signal may be accessed through pin 21 of the rear panel J102 DATA connector; negative true; amplitude ≤ 400 mV, 0 to +7 volts maximum; loading ≤ -1.4 mA at 400 mV.

OUT - Provides logic signal representation of the ADC acquisition and conversion times; internal jumper plug J10 provides the option of positive true or negative true logic pulses; shipped in the POS position; TTL compatible, totem pole output (LS) with 4.7k pull-up resistor.

2.3 FRONT PANEL CONTROLS

GAIN - Six-position rotary switch to select full scale resolution of input signal; selection of 512, 1024, 2048, 4096, 8192, or 16 384 channels for a 10 V input pulse or level.

RANGE - Six-position rotary switch to select 512, 1024, 2048, 4096, 8192 or 16 384 channels as the overflow limit and the limit of the address output lines to be driven.

OFFSET - Six toggle switches to provide suppression of the digital zero; 0 to 16 128 channels in binary multiples of 256 channels.

LLD - Ten-turn locking-dial precision potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range 0.02 to +10 V dc.

ULD - Screwdriver adjusted 22-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range 0.02 to +10.5 V dc.

ZERO - Screwdriver adjusted 22-turn potentiometer sets the input analog zero level; range ± 5% of input range; resolution 0.005% of full scale. Adjacent CALibration test point monitors adjustment voltage.

PEAK DETECT - Toggle switch to select either AUTOmatic or DELAYED initiation of conversion cycle. In AUTOmatic an internal constant-fraction trigger operates on the falling edge of the input pulse. In DELAYED mode, the Linear Gate ends and conversion begins at a selected time after the constant-fraction trigger point. An ADJustment potentiometer permits selection of from 2 to 100 μsec delay. An INSPect test point is provided to monitor the Linear Gate time delay adjustment, or for time sync of an applied GATE pulse input.

COINC/ANTI - Toggle switch to select either the COINCidence or the ANTIcoincidence mode of the GATE input pulse to enable or disable respectively a given conversion cycle. Pulse must be present during the Linear Gate time as monitored on the INSPect test point.

PHA/SVA - Toggle switch to select either Pulse Height Analysis or Sample Voltage Analysis modes of conversion. In PHA the input pulse must cross the LLD threshold to be accepted for conversion. In SVA a varying input dc level or pulse can be acquired (Peak detected) while the GATE input is high, and captured for conversion on the negative (falling) edge of the GATE input.

2.4 INDICATORS

DEAD TIME - Ten-segment LED indicator displays the average dead time of the converter. Jumper plug selectable for 0 to 100% or 0 to 20% full scale. Shipped in 0 to 100%.

2.5 PERFORMANCE

INTEGRAL NONLINEARITY - Less than ±0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY - Less than ± 0.7% over the top 99.5% of range including effects from tilt.

DRIFT - Gain - Less than ±0.009% of full scale/°C
Zero - Less than ±0.0025% of full scale/°C
Long Term - Less than ±0.005% of full scale/24 hours at a constant temperature.

PEAK SHIFT - Less than ±0.025% of full scale at rates up to 100 kHz

ADC DEAD TIME - Linear Gate Time + Conversion Time

Note: Since the 8077 ADC includes a data buffer, the MCA memory cycle time is not part of the ADC dead time for most applications. However, for high data collection rates or excessive MCA memory cycle time, the MCA cycle time may extend the ADC dead time proportionately.

CONVERSION TIME - 0.7 μsec + 0.0022 (N + X) μsec where N = address count, and X = effective digital OFFSET.

CHANNEL PROFILE - Typically flat over 90% of channel width.

2.6 POWER REQUIREMENTS

+24 V — 65 mA +12 V — 190 mA*
-24 V — 55 mA -12 V — 200 mA*

*This power exceeds the normal bin power allotment of 167 mA for a single width module.

2.7 PHYSICAL

SIZE - Standard single width NIM module 3.42 × 22.12 cm (1.35 × 8.71 inches) per TID-20893 (rev.)

OPERATING TEMPERATURE RANGE - 0° to 45° with adequate air flow.

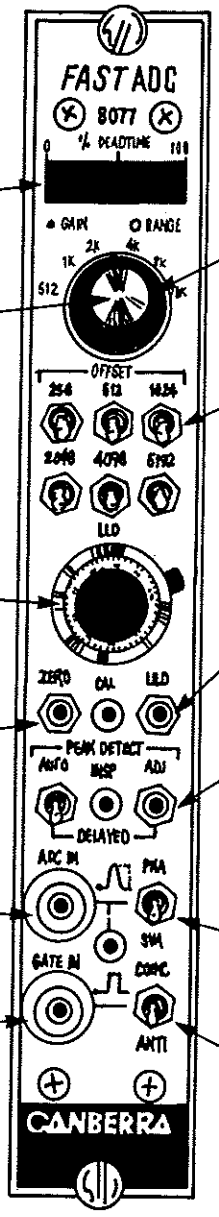
NET WEIGHT - 0.9 kg (1.9 lbs)

SHIPPING WEIGHT - 1.8 kg (4.0 lbs)

Section 3.
Controls and Connectors

3.1 FRONT PANEL

Refer to Section 2 for additional information and signal specifications.



% DEAD TIME
Ten-segment LED indicator displays the converter's average dead time in increments of 2% or 10%.

GAIN
Six-position rotary switch to select full scale resolution of input signal.

LLD
Ten-turn locking dial precision potentiometer; sets the Lower Level Discriminator for the minimum input acceptance voltage.

ZERO
Screwdriver-adjusted 22-turn potentiometer; sets the input analog zero level; adjacent CALibration test point monitors adjustment voltage.

ADC IN
Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, dc level or pulses for SVA, mode.

GATE IN
Accepts positive logic pulse or dc level for COINCidence and ANTIcoincidence gating.

RANGE
Six-position rotary switch to select the upper limit of digital overflow and address output lines to be driven.

OFFSET
Six toggle switches to provide suppression of the digital zero.

ULD
Screwdriver-adjusted 22-turn potentiometer; sets the Upper Level Discriminator for the maximum input acceptance voltage.

PEAK DETECT
Toggle switch to select either AUTOmatic or DELAYED peak detection to initiate conversion cycle; an ADJustment potentiometer permits selection of delay; an INSPect test point is provided to monitor the Linear Gate time.

PHA/SVA
Toggle switch to select either Pulse Height Analysis or Sample Voltage Analysis modes of conversion.

COINC/ANTI
Toggle switch to select COINCidence or ANTIcoincidence GATE input modes.

Figure 3.1
Front Panel

3.2 REAR PANEL

Refer to Section 2 for additional information and PUR signal specifications and to Appendix A for Data and Stabilizer signal specifications.

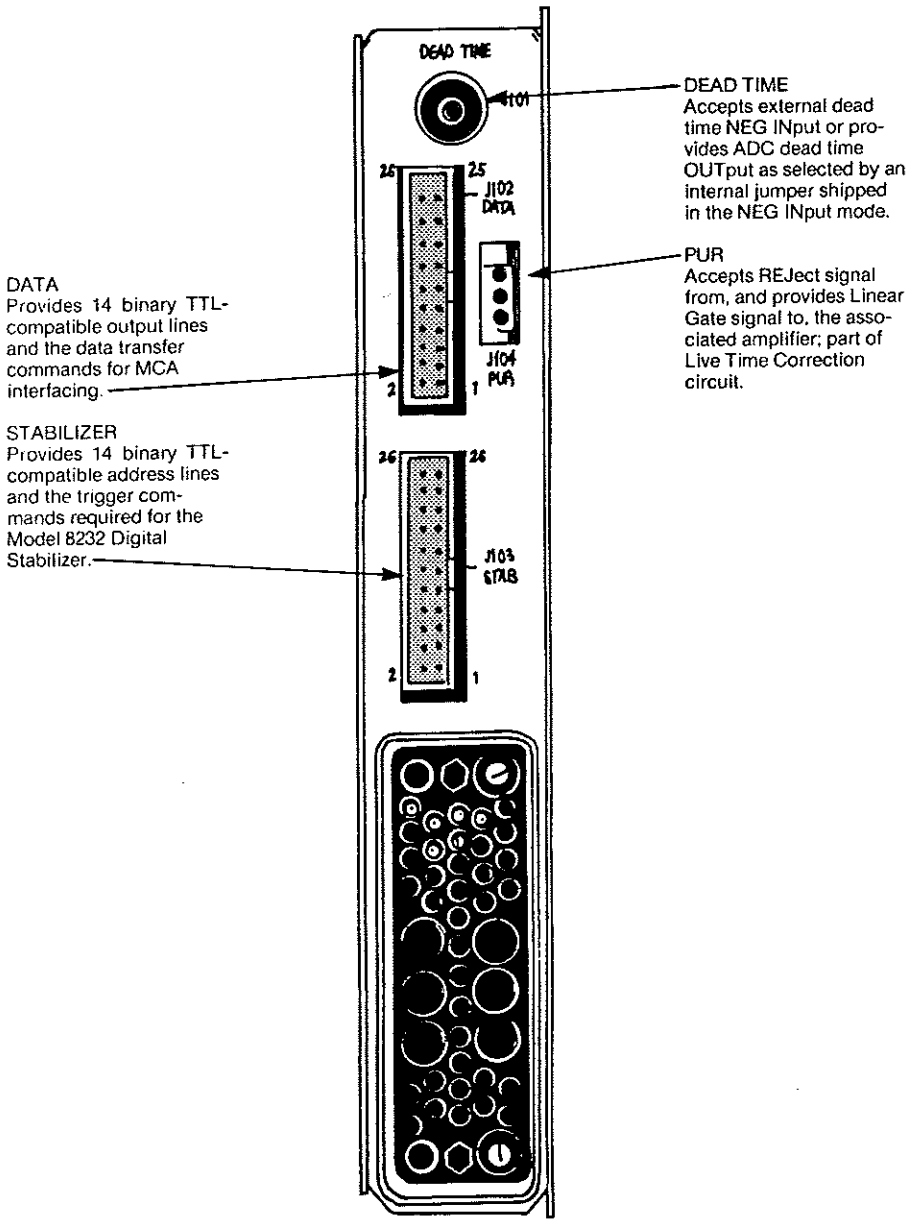


Figure 3.2
Rear Panel

3.3 INTERNAL CONTROLS

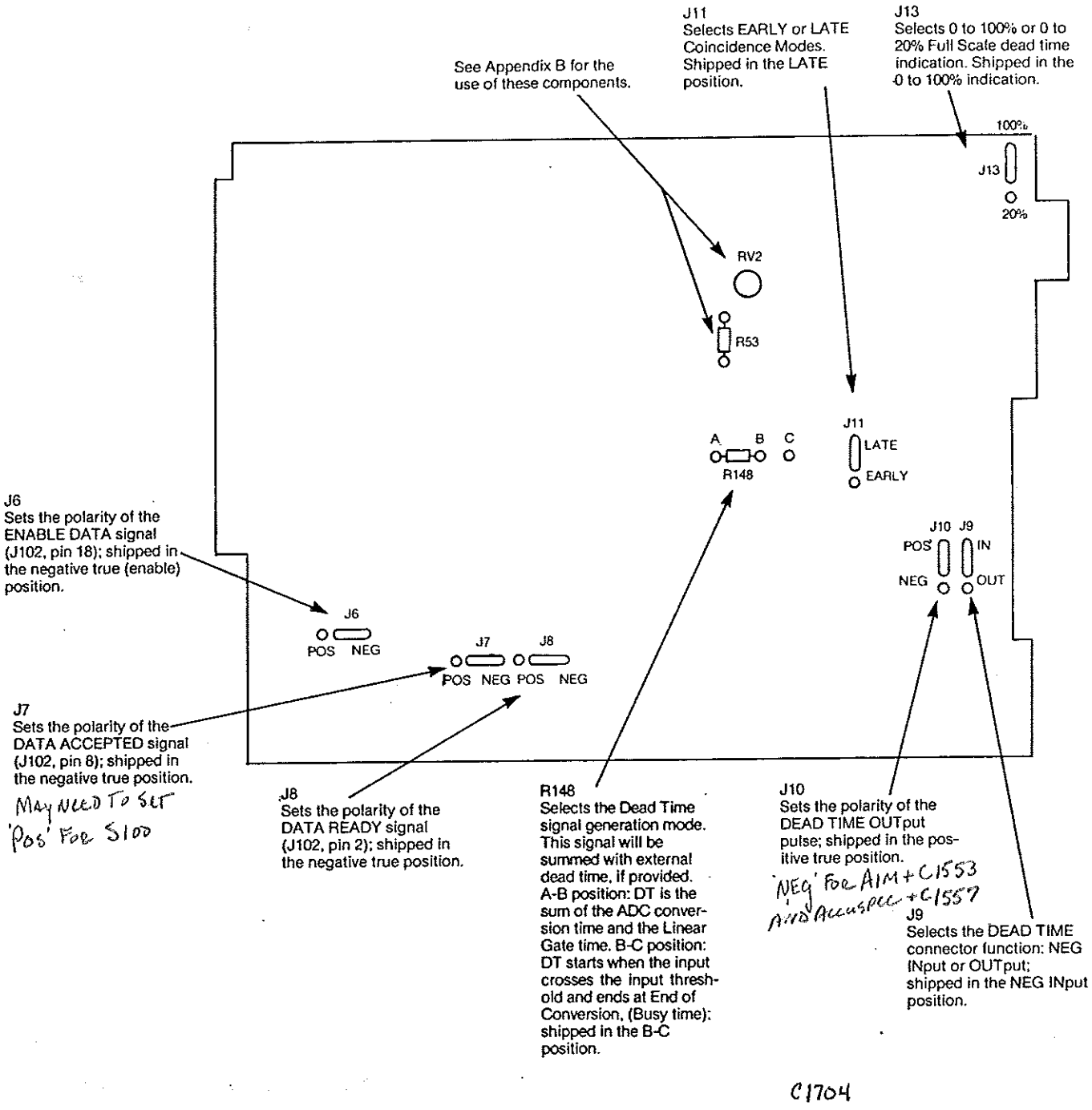


Figure 3.3
Internal Controls

Section 4. Operation

4.1 % DEAD TIME

The DEAD TIME indicator is a ten-segment LED display which shows the average dead time in increments of ten or two percent, jumper selectable, for 0 to 100% or 0 to 20% full scale indications respectively. Shipped for 0 to 100%. Refer to J13 in Figure 3.3.

Dead time is the time that the ADC is busy converting an input and increases proportionately with increases in gain and/or conversions per unit time.

4.2 GAIN

The GAIN controls the ADC's resolution; that is, the number of parts into which the full-scale (10 V) inputs can be divided. The larger the selected gain, the finer the divisions and the greater the resolution.

Higher gains take longer to make a conversion from analog to digital form, which increases the dead time. With GAIN set to 8192 and no OFFSET, the maximum conversion time is 18.7 μsec. With GAIN set to 512 and no OFFSET, the maximum conversion time is 1.84 μsec.

4.3 RANGE

The RANGE switch is commonly set to equal the size of the memory group assigned to the ADC. For instance a memory assignment of 4096 channels would require a RANGE of 4096.

Inputs which convert to a number greater than the selected RANGE will not be stored in memory. Since the range check is made after the input has been converted, an overflow conversion will add to the ADC's dead time.

4.4 OFFSET

The OFFSET is used to precisely shift the memory assignment of the ADC's conversions. With no OFFSET (all switches down), the ADC's channel numbers are the same as the memory's channel numbers.

For example, if the GAIN is set to 8192 and the memory assignment is only 4096, an OFFSET of zero will allow only the lower half of the full-scale conversions to be stored. That is, pulses up to five volts will be stored, pulses greater than five volts will not be stored.

If, in this example, the OFFSET were set to 4096 (the 4096 switch up), channel zero of the memory would be shifted to correspond to channel 4096 of the ADC. This offset would allow the upper half of the full-scale conversions, those above five volts, to be stored in the assigned memory.

4.5 LLD AND ULD

The Lower Level Discriminator (LLD) and the Upper Level Discriminator (ULD) controls set the limits for the input signals to be accepted by the ADC for conversion. If an input pulse falls within the selected window (higher than the LLD setting but lower than the ULD setting) the input will be converted. If the input does not fall within the window, the input will not be converted. The window check is made at the conclusion of the linear gate time; an input pulse not within the window will add to the ADC's dead time.

4.6 ZERO

The ZERO control varies the zero intercept of the ADC conversion function so that zero energy is stored in channel zero of the memory. The Model 8077 is shipped with the ZERO set for a GAIN of 8192. For other gains, a slight adjustment of the control may be necessary for precise energy calibration.

For accurate setting of the ZERO control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. Connect the Pulser's SIGNAL OUT to the ADC INput.
2. Set the Pulser to HI, 0^0, +, and 0.5 μsec Rise Time.
3. Set the ADC's GAIN control as desired.
4. Set all binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY on, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.
5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be switched in on the ADC. For instance, if the memory is 4096 channels and the GAIN is set for 8192, an OFFSET of 4096 must be added so that conversion can take place in the highest channel of the memory.
6. Turn all binary switches on the Model 8210 OFF, except the 1/128 switch, which should be left ON.
7. Set all OFFSET switches on the ADC to the off (down) position.
8. Adjust the ZERO control so that counts are being collected in the proper channel, as follows:

Gain	Channel
16 384	128
8192	64
4096	32
2048	16
1024	8
512	4

9. Repeat steps 4 through 8 until no further adjustments are necessary.
10. The voltage which can be seen at the CAL test point may be recorded and used in the future for quickly setting the ZERO control.

4.7 PEAK DETECT

In the AUTO mode, the linear gate, which allows a valid input pulse to be acquired, opens when the input rises above the input threshold. The input threshold level tracks the LLD setting up to 100 mV, maximum; therefore, the input signal's baseline must be less than 100 mV for proper ADC operation.

The linear gate closes when the input pulse falls below 90% of its peak amplitude. Wide input pulses may make the AUTOmatic detection of the 90% point less certain. To overcome this uncertainty, the DELAYED peak detect feature may be used. This feature allows input pulses up to 100 μsec wide to be converted. In this mode the linear gate closes at the end of the selected delay time. The delay time can be selected with the ADJ control while monitoring the INSP test point next to the ADJ control.

In either peak detect mode, the INSP test point provides a positive logic pulse; the pulse width represents the ADC linear gate time.

4.8 GATE

Input pulse conversions may be enabled or disabled by using the GATE function. This function is not the same as the linear gate, which is an internal circuit.

In the COINC mode, a positive logic pulse at least 250 nsec wide or a positive dc level must be present at the GATE connector during the linear gate time. The opening and closing of the linear gate can be seen at the peak detect INSP test point.

If the GATE input is low during the linear gate time, conversion will not take place.

An internal jumper (EARLY/LATE) is shipped in the LATE coincidence position, which means that the GATE pulse must be present sometime during the linear gate time to be effective. Since a common gating signal is the output of an independent SCA module, this late-arriving pulse can be accommodated by using the DELAYED peak detect mode and adjusting the linear gate time, as seen at the INSP test point, so that the linear gate closes after the SCA's output arrives. Thus the need for delaying the ADC INput signal can be eliminated.

If the jumper is changed to the EARLY coincidence position, the GATE signal must be present before the linear gate opens and remain for at least another 250 nsec. Refer to J11 in Figure 3.3.

EARLY coincidence is preferable when a high count rate is being gated because of the appreciable dead time introduced in the LATE coincidence mode. However, LATE coincidence gating is easier to do since a delay amplifier is not needed.

In the ANTI mode, the logic sense of the GATE signal is inverted. That is, a logic low will enable the linear gate and a logic high will disable it.

Note that in the ANTIcoincidence mode, the gating logic must be set for LATE coincidence for proper operation.

In any gating mode, an open GATE (nothing connected to the GATE connector) acts as if an enabling level were present.

4.9 SAMPLED VOLTAGE ANALYSIS

The ADC is usually used in the Pulse Height Analysis (PHA) mode, but by changing the PHA/SVA switch to the SVA position, analog voltages can be sampled by the ADC. The result will be an amplitude distribution curve of the input signal. The input signal must be between 20 mV and 10 V in amplitude to be sampled. If desired, an amplitude window may be set with the LLD and ULD controls.

The GATE input supplies the sampling signal, which must be equal to or greater than one microsecond in width. However, for pulse inputs (rather than dc levels or slowly changing ac signals), the GATE input signal must be narrower than the input pulse width.

The sampling rate should be at least twice the frequency of the input signal for accurate sampling.

4.10 REAR PANEL CONNECTORS

J101 DEAD TIME - A dual-function connector which can be used as either an external dead time input from the Model 2020 amplifier or an internal dead time output. The mode is selected by an internal jumper (J9). Shipped in the NEGative INput mode.

J102 DATA - Used to connect the ADC, with the supplied cable, to the Analyzer or to a Mixer/Router.

J103 STAB - Used to connect a Digital Stabilizer to the ADC.

J104 PUR - Accepts the REJect signal from, and provides the Linear Gate (LG) signal to, the Model 2020 amplifier.

Further information and signal specifications for J101 and J104 can be found in Section 2 and for J102 and J103 in Appendix A.

4.11 ADC INTERFACING

This ADC improves its throughput by using a data buffer, which allows it to accept another analog input and start converting it while the previous conversion is being transferred from the buffer to the memory unit. In the unlikely event that the conversion finishes before the previous data has been transferred from the buffer, the new data is momentarily held in the counter and no new conversion can start until the DATA ACCEPTED signal is received.

The result of the ADC's conversion is a 14-bit binary-coded number. At the end of the Wilkinson ramp time, this number is transferred into a holding register (buffer) and signal DATA READY is set true. The address data is then valid and can be used by the MCA or CPU. At this point, the ADC is free to begin another conversion.

The DATA lines are driven by tri-state drivers that are controlled by the ENABLE DATA input. The DATA ACCEPTED input signals the ADC that the current output data has been transferred and the result of the next conversion can be loaded into the buffer.

For revision B and earlier ADCs, the maximum time is 1 ms. This should not be a problem since normal MCA data transfer times are 1 to 20 μs. For longer hold times, consult the factory. There are no restrictions for C revision and higher ADCs. The revision level is indicated by the letter following the identification number at the top of the printed circuit board.

It may sometimes be necessary to record all inputs whether valid or not. Secion 4.12 describes the conditions which will set the INVALID flag output (signal INV at J102, pin 14). Because of the ADC buffer operation, the ADC can begin a second conversion even though the first event was not yet accepted by the memory storage device. If a second conversion is completed and invalid prior to the transfer of the first conversion, there is no way to determine which event, the first or the second, is invalid. Thus, without using the GATE or ENABLE CONVERTER inputs, there is no INVALID/DATA synchronization.

The ENABLE CONVERTER input (J102, pin 10) or the front panel GATE input can be used to inhibit a later conversion and thus synchronize multiple ADCs. These inputs must be used because the ADC does not buffer INVALID events. That is, the ADC is not normally inhibited from processing later inputs if the current conversion is INVALID.

The DEAD TIME output is the sum of the ADC Conversion Time and the Linear Gate Time and begins with the Linear Gate. It does not include the time that it may take the input to go below the threshold. An internal jumper (A-B) can change the DEAD TIME output to begin when the input signal exceeds the input threshold (20 to 100 mV) and end when the ADC can accept a new input and the input level is below the threshold. In this mode, the DEAD TIME output is the sum of the Conversion Time and the time that the input is above the threshold.

If an external Live Time Corrector (for example, the Model 2020 Amp) is used, its BUSY signal is summed with the ADC DEAD TIME. The ENABLE CONVERTER and GATE signals make no contribution to the dead time, although when false, they do inhibit conversion.

4.12 INVALID FLAG CONDITIONS

For a conversion to be accepted, it must meet all of the following criteria. When violated, the INVALID flag (J102, pin 14) will be set.

SCA Window - Pulses not in the SCA's analog window will be rejected, initiating a dump cycle. An LLD or a ULD violation will generate the INVALID flag. Both states are interrogated at the 90% point.

Baseline - Input pulses exceeding the ADC ZERO baseline will be rejected, initiating a dump cycle. The condition is interrogated at the 90% point, setting the INVALID flag when violated.

Digital Underflow - Input pulses resulting in a numeric conversion less than the counter back-bias or less than the digital offset, or both, will be rejected by inhibiting ADC READY. The INVALID flag will be set at EOC (end of conversion).

Digital Overflow - Input pulses resulting in a numeric conversion greater than the ADC RANGE will be rejected by inhibiting ADC READY. The INVALID flag will be set at EOC (end of conversion).

Late Coincidence/Anticoincidence - The GATE pulse width must be at least 250 ns wide and be true (high for coincidence, low for anticoincidence) for at least 100 ns prior to the 90% point or the end of Linear Gate. Otherwise the conversion is aborted by initiating a dump cycle. The INVALID flag will be set at the 90% point.

Early Coincidence/Anticoincidence - The GATE pulse width must be at least 250 ns wide and be true (high for coincidence, low for anticoincidence) for at least 100 ns prior to the initiation of ADC BUSY as determined by an ADC input pulse crossing the ADC input threshold. Otherwise the INVALID flag will be set at the trailing edge of the GATE pulse.

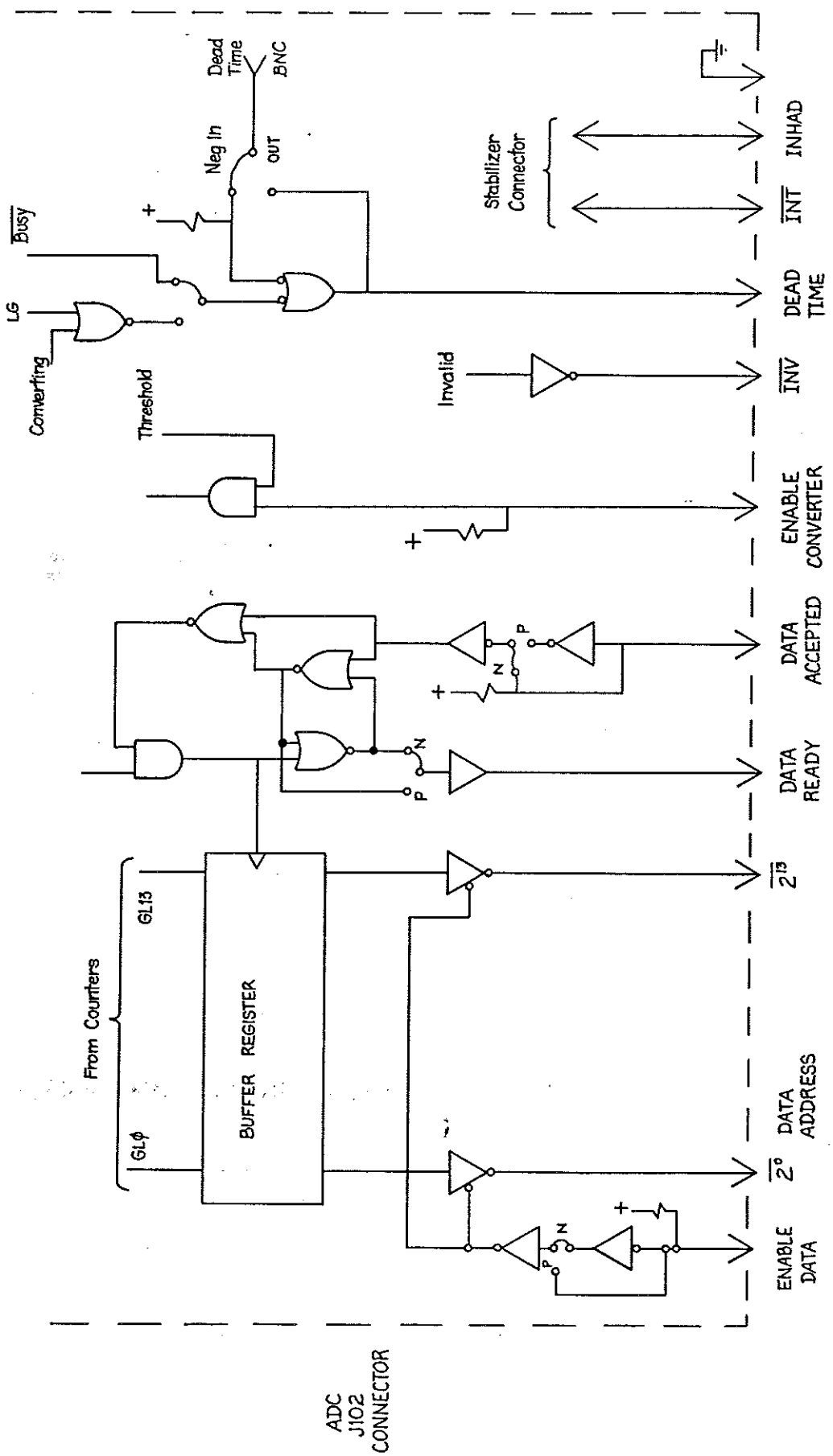


Figure 4.1
8077 Interfacing Logic (Logic shown is representative. Refer to Logic Schematic B19864 for details.)

Section 5.
Theory of Operation

5.1 GENERAL
The following is a description of the circuitry used in the 8077 FAST ADC. Components are referred to reference designations such as Q2, C5, and R10. Throughout the following circuit description, please refer to the circuit block diagram, schematics, and timing diagram.

5.2 BLOCK DIAGRAM DESCRIPTION
The 8077 ADC is a Wilkinson-type ADC; the input signal is captured on a holding capacitor and discharged at a constant rate while counting clock pulses into an address register.

Prior to the acquisition mode, the ADC stretcher is normally active and will track and follow input signals. If no conversions are in progress and the input signal threshold is exceeded, Busy flip-flop A48b will get set. Linear Gate (LG) is enabled, indicating the ADC is acquiring a signal. The stretcher will now peak detect the corresponding input signal. When the input signal falls to 90% of its peak value, comparator A12 changes state, starting a conversion.

At this time a decision is made: If the voltage on the stretcher (peak value of the input signal) is greater than the LLD and less than the ULD, and the GATE criterion is satisfied, the Start Convert (SC) flip-flop (A29a) will get set. The Linear Gate closes and the ADC conversion begins. The voltage on the stretcher capacitor (C31) is ramped down until the zero comparator A7 detects the crossover point, which ends the conversion. SYNC/ is reset, and the trailing edge initiates the timing chain driven by A39c. The outputs from these one shots load the converted address into the bus driver latches (A14, A15), set the DATA READY request, and generate EOC, which resets the ADC and interrogates for invalid flags.

In response to the DATA READY request, the MCA or computer sets ENABLE DATA true, which activates and enables tri-state bus drivers, A14 and A15, allowing the ADC address data to be presented on the data bus. At the conclusion of the Data Storage Cycle, DATA ACCEPTED is set, clearing the DMA READY request flip-flop.

If the pulse was not within the LLD-ULD window or the GATE criterion was not met, the stretcher capacitor will be reset (dumped) quickly to prepare for a new input.

5.3 ADC THEORY OF OPERATION
5.3.1 Stretcher (Sheet 1 of the schematics)
The Stretcher is a discrete op-amp configured as a positive peak detector/holder including a calibrated precision ramp-down circuit. The peak holder has negative feedback via R28 and C9, providing a gain of +1. The Stretcher comprises transistors Q1 through Q6, Q8 through Q14, Q15, Q16, Q18, and IC A8. Transistor array A8 is connected as a Darlington differential amplifier and allows a larger dynamic range at its input. Thus, the input signal is connected directly without attenuation for improved signal-to-noise ratio characteristic. FET Q8 and transistor Q6 are connected to form a buffer providing low output and high input impedances. R21 and C8 form a low-pass filter limiting the input rise time and high-frequency noise. Diode D3 provides a negative input clamp. RV3 can vary Q9's collector current by approximately ±2%, enabling the differential amplifier to be precisely balanced, establishing the Stretcher Output dc offset.

Pin 8 of the differential amplifier drives the base of Q5. When the differential amplifier receives a signal, more positive with respect to the peak holder output, A8 steers current, turning Q5 on. Q5 supplies current limited by R14 and charges capacitor C13 through Cascode Q33. The resultant voltage generated on C13 is buffered to the Stretcher Output by FET follower Q8/Q6 and follows the positive transition of the input signal. When the input signal slope reduces to zero, or goes negative, A8 steers all current through pin 12. Q14 now pulls the base of Q5 positive, turning it off. With the ramp and Q15 OFF, the voltage developed on C13 remains until the ramp-down cycle begins. The output buffer supplies a buffered signal to the differential-amplifier negative input (A8 pin 9) via feedback resistor R28, zero-crossing comparator, and Stretcher/Input interrogation comparators. During the ramp-down cycle, the peak holder is gated OFF by Q1, Q2 and Q3.

5.3.2 Ramp-Down Generator (Sheet 1)
The ramp-down generator is a gated precision-current source. A constant sink-current is developed and switched between ground (ramp off) and the peak holder storage cap (ramp on). The ramp-down circuit comprises Diodes D6, D7, transistors Q10 through A14, Q15, Q16, Q18, and op-amp A6. D6 and D7 are 6.2 volt Zener diodes, referenced to the -24 volt supply, producing a temperature stable reference-voltage source of -11.6 volts referenced to ground and op-amp A6. Transistor Q18 performs a voltage-to-current transformation. The op-amp input reference voltage (A6 pin 3) also appears at the emitter of Q18 establishing a constant voltage across the current set (conversion gain) resistors (R54 through R60), producing a precision current. The ramp current is precisely calibrated using RV2. The precision ramp current is steered to ground or the peak-holder storage capacitor by current steering transistors Q13 and Q14.

For an invalid conversion, the Control Logic sets DUMP true. Q15 and Q16 are biased on, a current (significantly higher), independent of the precision current generator now dominates, producing a much faster RAMP DOWN or DUMP cycle.

5.3.3 Stretcher/Input Interrogation Logic (Sheet 1)
The Stretcher/Input interrogation logic is made up of comparators A12, A13, and op-amp A9. A13 pin 7 generates a logic "0" (ITHR/) whenever the ADC input signal

exceeds the threshold reference voltage. Normally the output of A9 follows the LLD voltage. However, if the LLD reference voltage is set higher than +100 mV, determined by R67 and R68, diode D8 reverse biases and the threshold reference voltage is limited to +100 mV. For LLD voltages of +100 mV and less, diode D8 forward biases, forcing the threshold reference voltage to track the LLD down to 0 volts.

The 90% comparator (A12) monitors both the Stretcher Output (pin 3) and ADC input (pin 2). The Stretcher Output is attenuated 10%, determined by R31 and R79. Thus for a given ADC input, pin 2 is more positive than pin 3 (Stretcher Output) setting A12 pin 7 to a logic "1". When the ADC input reduces by approximately 10%, compared to the captured Stretcher signal, A12 pin 7 is set to a logic "0" (90% indication).

5.3.4 SCA (Sheet 1)
Comparators A10 and All compare the Stretcher Output signal with the LLD and ULD reference voltages respectively. If the Stretcher Output is above the LLD threshold, A10 pin 7 is set to a logic "0" (LLD/). If the Stretcher Output is above the ULD threshold, A11 pin 7 is set to a logic "0" (ULD/). The LLD and ULD reference voltages are calibrated to +9.0 and +9.6 volts respectively, using RV5. The LLD and ULD reference voltages are scaled in proportion to the front panel LLD (RV1) and ULD (RV2) settings, covering a range of 0 to +10.0 and 0 to +10.7 volts respectively, when referenced to the ADC Input.

5.3.5 Zero-Crossing Discriminator (Sheet 1)
The zero-crossing discriminator comprises FET Q19 and comparators A7 and A4. The zero-crossing comparators interrogate the Stretcher Output (TP4), ending the ramp-down and synchronizer/counter cycles when the negative ramp reaches the baseline (zero) reference voltage. Two comparators are used in cascade for improved comparator gain and analog-to-digital buffering.

FET Q19 serves as a limiter. For Stretcher Output signals 2 to 3 volts more positive than the comparator reference input (A7 pin 3), the FET pinches off and becomes a high impedance. For smaller signals, Q19 remains a low impedance, providing a low impedance signal to comparator input A7 pin 2). Resistor R82 and diode D9 serve as a load when the FET is pinched off, maintaining a voltage more positive than that of the reference voltage.

For Stretcher signals more positive with respect to the baseline (zero) reference voltage, A7 pin 7 is set to a logic "1". A4 pin 7 is set to a logic "1" while A4 pin 8 is set to a logic "0", enabling the synchronizer and address counters. When the Stretcher ramps down such that the Stretcher signal equals or becomes more negative than the baseline (zero) reference voltage, A7 pin 7 is set to a logic "0". A4's outputs (7 and 8) are set to a logic "0" and "1" respectively, ending the ramp-down and synchronizer/counter cycles.

The baseline (zero) reference voltage is set by the front panel ADC zero control RV3. The control covers a range of ±5%. The baseline (zero) reference voltage can be remotely set to ±2% for ±5 volt signal at the STAB zero input, pin 16 of J103.

5.3.6 450 MHz Oscillator (Sheet 2)
The oscillator consists of a Colpitts crystal-controlled, 150 MHz oscillator which drives a subsequent resonant frequency tripler circuit.

Capacitors C46 and C47 in parallel with inductance L9 form the resonant tank circuit of the basic 150 MHz oscillator. These tank capacitors also form a capacitor attenuator which provides voltage feedback through the 150 MHz crystal. Inductance L10 in parallel with the crystal resonates with the crystal capacitance increasing its apparent series impedance and lowering its series current.

Differential amplifier Q21/Q22 is biased to operate Class C driving resonant load L13 and C52, tuned to the third harmonic (450 MHz). Differential amplifier Q23/Q24 provides voltage gain and drives the output filter and impedance matching network (L15 through L17, C58 and C59) which is also tuned to 450 MHz.

5.3.7 Synchronizer (Sheet 2)
A2 and A3 are configured as a synchronizer that serves to synchronize the ADC Ramp and counter functions with the 450 MHz clock. When "START" signal is initiated, SCD/ (Start Convert Delayed Not) is set to a logic "0", removing the synchronizer clear, a ramp-down sequence is initiated. On the next positive clock transition Q/ and Q of A3 are clocked true. On the positive transition of the second clock, Q and Q/ of A2 are clocked true. The setting of A2 causes two things to happen simultaneously: the address counter is armed to begin counting with the next 450 MHz clock, and the control logic initiates the ramp by setting RAMP ON/ to a logic "0". The ramp current is steered to the peak-holder storage cap and linearly discharges the cap at a rate proportional to the conversion gain setting. When a zero crossing is detected by the zero-crossing discriminator, the D proposition of A3 is set false. On the positive transition of the next clock Q of A3 is set false, setting the D proposition of A2 to a logic "0". On the positive transition of the 2nd clock, Q and Q/ of A2 are set false. This action simultaneously disables the address counters and sets SYNC/ to go to a logic 1, ending the ramp down cycle and initiating the EOC (End of Conversion) sequence.

5.3.8 Counter Logic (Sheet 2)
The address counters (A1, A5, A19, and A20) are configured as a 15-bit ripple counter. The 15th bit is used for under and overflow detection. During the ramp-down sequence, the ramp counter and ramp current are enabled and synchronized to the 450 MHz clock. When the zero-crossing reference point is reached, the zero-crossing discriminator and synchronizer gates the address counter off, again synchronously with the 450 MHz clock. The resultant digital address in the address counter represents the magnitude of the ADC analog input.

Since the beginning of the ramp may be non-linear, the address counter is offset or back biased by 64 counts for all conversion gains. This allows the counter to be referenced to the more linear region of the ramp-down signal. Circuit propagation delays reduce the effective number of digital back bias channels to approximately ten, which are compensated for at the zero crossing comparator with the introduction of an analog offset. The effective ten channels of digital back bias represent a fixed amount of time, i.e., ten clock cycles or 22 nsec. However, as the conversion gain changes, so do the volts per channel, and thus the required analog back bias, which is performed automatically with the selection of ADC Conversion Gain.

Digital offsets are selected using front panel switches to set the respective counter preset lines to a logic "0". ADC digital offset presets the address counter in increments of

512 and include 512, 1024, 2048, 4096, and 8192. All counter offsets are loaded into the counter prior to the start convert command.

Tri-state latched bus drivers A14 and A15 interface to the data bus. A18 and A22 are assigned for operation with external stabilization. The address data is presented to the tri-state latches while T1 is true and is clocked in at its trailing edge. Data becomes active on the bus when ENABLE DATA is set true.

5.3.9 Range/Overflow Logic (Sheet 2)
The address range data is selected by the Range switch S1C for digital comparison. The range data and corresponding address bits QL0 through QL13 are compared by digital comparators A16 and A17. If the address counter does not count past the digital pre-bias, or if it exceeds the range selected, the comparator <R signal instructs the control logic to inhibit the ADC Ready signal for that conversion. Thus the under/overranged data is not stored in the MCA memory. When the address counter offset is loaded, the 2^{14} (A29-9) bit is set to a logic 1. The counter must count past the digital pre-bias before this bit is set back to a logic 0. Thus the 2^{14} bit is also used as an underflow indication. If at the end of a ramp-down sequence the 2^{14} bit remains high, the <R flag would again be set, inhibiting the ADC Ready for that underflow conversion.

5.3.10 Control Logic (Sheet 3)
Prior to an input signal, the ADC Linear Gate (LG) is open. The ADC stretcher is in the track (TRK) mode and will track and acquire an impending input signal. The arrival of an ADC input signal sets ITHR/ (A13 pin 7) true, setting Busy A48b true and TRK false. The precision ramp is switched off, allowing the stretcher to acquire and peak detect the input signal. When the stretcher has charged to the peak value of the ADC input signal and reduces by approximately 10%, the 90% comparator, A12-7 is set true. If the ADC input signal is within the SCA window and the coincidence criterion is met, the 90% signal sets the Start Convert (SC) flip-flop true. The stretcher is gated OFF, LG is set false, and after a short latency time, the ramp down cycle begins.

The counters and stretcher ramp are initiated synchronously. When the ramp down cycle is completed, resulting from a zero crossing detection from A7 pin 7 an End of Conversion (EOC) cycle is initiated. Monostable A49 is set generating a counter stabilization time period T1. At the end of the T1 counter stabilization period A49a is set, generating EOC, which clocks the Ready (RDY) flip-flop (A45b) and generates an ADC reset, setting flip-flop A39b. If the ADC RANGE criteria was not violated, DATA READY (A45b) is set true, initiating a data storage cycle. The MCA or computer generates a DATA ACCEPTED signal, setting ADCR/ (ADC Release) true, which clears the RDY and INVALID Logic. When the input signal falls below the ITHR/ reference, the reset signal clears the SC flip-flop and releases the Busy flip-flop.

A. Delayed Peak Detect
If the DELAYED PEAK DETECT mode has been selected, the 90% interrogation comparator is replaced by a 555 timer via A42 and switch S8a. Thus the TOP (Time of Peak) signal that starts the ADC conversion is now initiated by the trailing edge of A42 pin 3. A42 is configured as a monostable, which is front-panel programmable, covering a range of approximately 2 to 100 μsec. The leading edge of LG (Linear Gate) is differentiated by leading edge discriminator A41 and A47, initiating the monostable time-out period.

B. Coincident Logic
LATE Coincidence, ANTI Coincidence and EARLY Coincidence may be selected and performed.

With LATE Coincidence selected, switch S10a connects R166 to +5 volts biasing the GATE input to the enable mode. If GATE remains positive during Linear Gate (LG) the coincidence flip-flop, A47a/A47b, will be set and if the LLD, ULD, and REJ criteria are satisfied, the Start Convert (SC) flip-flop VALID proposition will be true, allowing the conversion to proceed.

With ANTI Coincidence selected, switch S10b connects R166 to -12 volts, biases the GATE input to the enable mode, and selects the coincident flip-flop output complement. The SC flip-flop VALID proposition will be set true, and the conversion will be allowed again, provided the LLD, ULD, and REJ criteria remain satisfied. However, if the GATE input is set positive during LG, the Coincidence flip-flop A44 will be set, disabling the start convert flip-flop. At the conclusion of LG, the ADC will abort the attempted conversion.

C. Dump
If the ADC input signal did not satisfy the LLD/ULD, ADC baseline (GZR), and Coincidence criteria, or if a REJ was initiated, the pending conversion is aborted. For this case, both the 90 flip-flop (A39d) and SC flip-flop (A29a) are clocked as before. However, the SC flip-flop proposition is false, and the flip-flop will not get set. For this condition, DUMP is set true which rapidly discharges (approximately 6.7 V/ μsec) the Stretcher holding capacitor C13. When ITHR/ and GZR/ or LLD/ return to a logic "1", the 90 flip-flop (A39d) is cleared, ending the Dump cycle and arming the ADC for the next conversion attempt. An INV (invalid) flag will be set, RDY (ready) will not be set, and an MCA Storage cycle will not occur. REJ (reject) is gated with LG, therefore, to perform a reject/dump; reject must occur during the LG time window. PR (power reset) also initiates a dump sequence.

D. SVA (Sampled Voltage Analysis) Mode
With SVA selected, PHA is set false and the A inputs of multiplexer A34 are connected to the Y outputs. Busy flip-flop A48b is disabled and TRK is set to a logic "0". Prior to a Positive Gate signal the SC flip-flop A29a is held cleared, and the 90 flip-flop A39d is held preset. Both RAMP ON and DUMP are set true while STR OFF is held false. Thus the Stretcher is in the fast-track mode and follows the ADC Input signal. When the Gate signal is set positive, the 90 flip-flop is cleared. RAMP ON and DUMP are set false, placing the Stretcher in the hold mode. If the Stretcher Output signal is within the SCA Window, the SC flip-flop proposition will be set true, enabling the flip-flop. Coincident with the trailing edge of Gate, the SC and 90 flip-flops are set, and the ADC conversion commences.

5.3.11 Invalid Logic (Sheet 4)
For events that do not satisfy the LLD, ULD, Baseline, and COINC criteria, INV/ (invalid) is set and the ADC defaults to the Dump mode at the Linear Gate conclusion. For

events which result in a digital under or overflow, Invalid is set at the End of Conversion (EOC), Ready is not set, and the data is discarded.

The Dump signal is leading edge discriminated and clocks A51a (INV) to a logic 1, generating INV/. The only instance when this is not the case is in the occurrence of REJ. During Linear Gate, if REJ occurs, A51b is set, disabling the INV flip-flop and inhibiting the generation of INV/.

Events that result in digital underflow or overflow set INV/ where<R is interrogated during the time of EOC/. If<R is low at this time, a logic 0 presets A51a setting INV/.

Invalid for Early Coincidence is detected via A48a. With the EARLY/LATE jumper in the EARLY mode, signal GATE B/ becomes active. PHA BUSY/ is the D proposition of A48a. GATE B/ is the clock. If PHA BUSY/ is not low at the trailing (rising) edge of GATE B/ (A48a) is clocked true 1, which presets INV/.

The Invalid flip-flop (A51a) is reset by the next ADCR/ (DATA ACCEPTED) to the ADC. The Invalid flip-flop (A51b) is reset by 90CLR/.

5.3.12 Dead Time Display (Sheet 4)
A1 (Board 2) is an integrated circuit that senses analog voltage levels and drives the 10-segment bar-graph (Board 2), providing a linear analog display of the ADC dead-time. The analog voltage is integrated from the ADC dead-time signal provided from A28c. Full scale ranges of 20% or 100% may be selected with jumper plug J13. Variable resistor RV4 sets full scale calibration.

5.3.13 5 Volt Power Supply (Sheet 5)
The +5 and -5 volt power supplies are synthesized by a push-pull switching inverter which operates off the +12 V and -12 V NIM voltages. Q29 and Q30 are operated as saturating switches in a relaxation oscillator through the power transformer. The operating frequency is set by the transformer primary inductance and C120 at about 70 kHz. The feedback winding of the transformer alternates drive between Q29 and Q30 to generate a push-pull voltage to the primary. Rectifiers D21 through D24 convert the push-pull ac to a full-wave output. XFMR-1 in the +12 V line, driving the center tap of the power transformer, couples an ac waveform to the secondary at the output of the rectifiers in a phase and level which effectively cancels the ripple voltage in the dc output. C123 and C125 are used to integrate the small residual ripple and reduce noise in the voltage output.

Q32 and Q31 provide short-circuit protection of the output by sensing the input dc current to the inverter and switch off the drive to Q26/Q27 if a fault is detected.

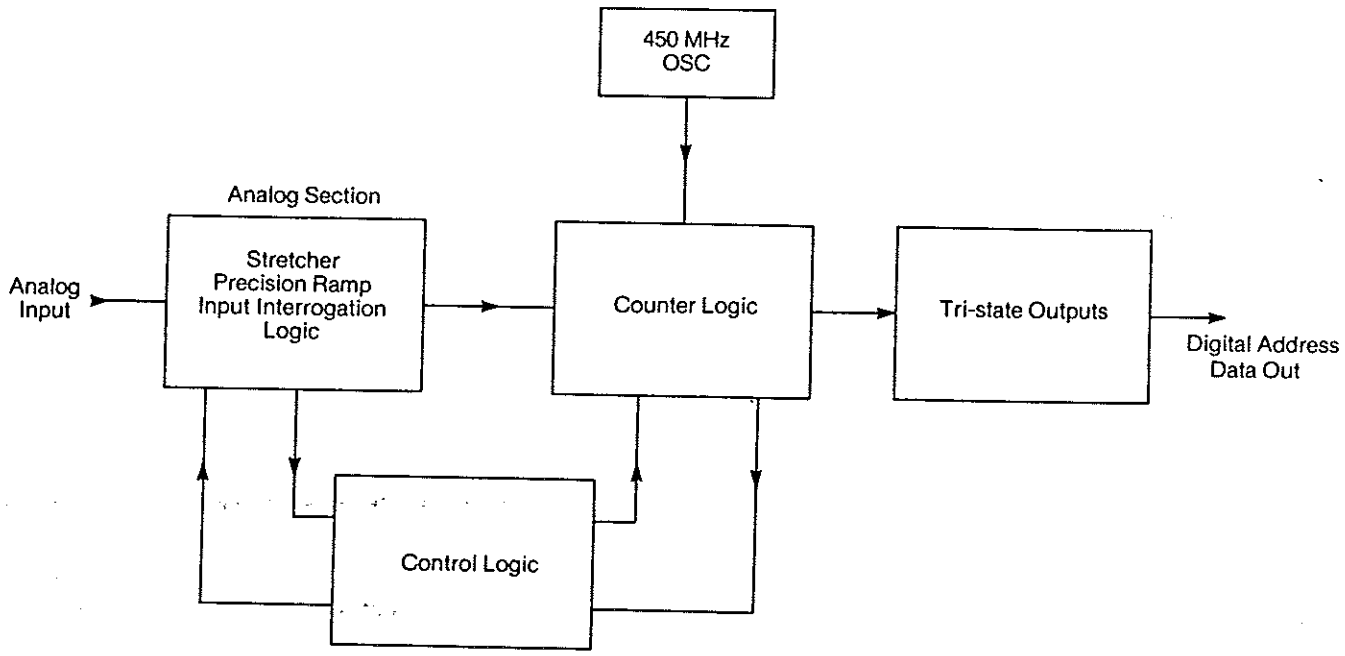


Figure 5.1
8077 ADC Block Diagram

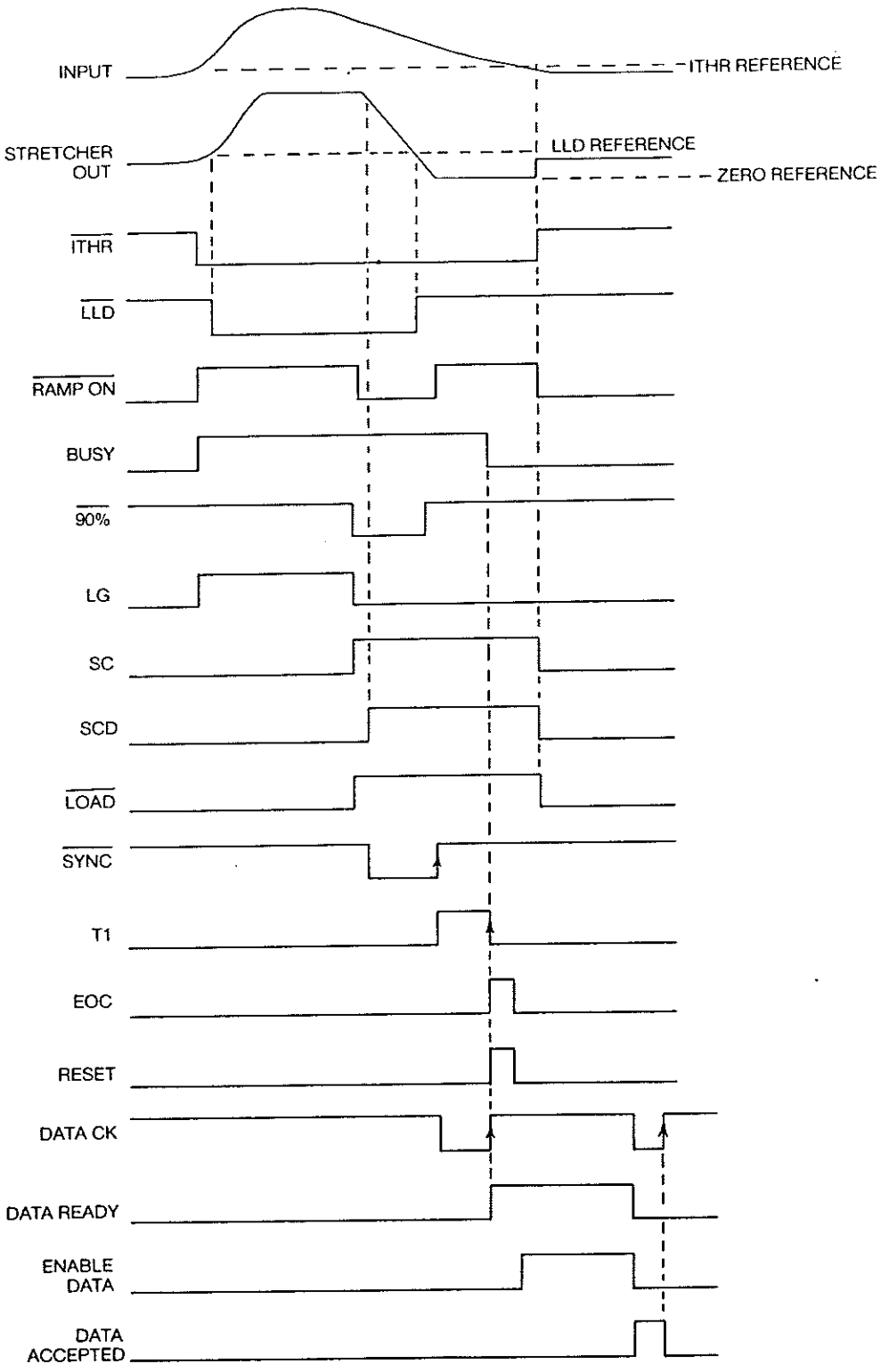


Figure 5.2
8077 Timing Diagram

Appendix A
Connector Signals

A.1 J102 - DATA

Pin	Signal	In/Out	Description
1	$\overline{2^0}$	Output	
3	$\overline{2^1}$	Output	
5	$\overline{2^2}$	Output	
7	$\overline{2^3}$	Output	
9	$\overline{2^4}$	Output	Gated binary address data, negative true (0 V) as standard: TTL Tri-state outputs; outputs are enabled by setting ENABLE DATA to a logic 0. $V_o > 3$ V @ 20 mA (High) $V_o < 0.9$ V @ 20 mA (Low)
11	$\overline{2^5}$	Output	
13	$\overline{2^6}$	Output	
15	$\overline{2^7}$	Output	
17	$\overline{2^8}$	Output	
19	$\overline{2^9}$	Output	
21	$\overline{2^{10}}$	Output	
23	$\overline{2^{11}}$	Output	
25	$\overline{2^{12}}$	Output	
4	$\overline{2^{13}}$	Output	

Pin	Signal	In/Out	Description
2	DATA READY	Output	Signals external memory storage unit that a conversion is complete; positive true or negative true logic, set by internal jumper J8; shipped in negative true.
6	$\overline{\text{INHAD}}$	Pass-through	Inhibit Add; this signal comes from a Digital Stabilizer and is passed directly to the memory storage unit. The $\overline{\text{INHAD}}$ signal is used to prevent storage of a reference peak from a pulser. Active negative true logic.
8	DATA ACCEPTED	Output	Feedback signal from the memory storage unit which acknowledges data acceptance. This pulse resets the ADC and clears the INValid flag, if set. Positive true or negative true logic set by internal jumper J7; shipped in negative true. TTL hysteresis input with a 4.7k ohm pull-up resistor to 5 V.

Pin	Signal	In/Out	Description
10	ENABLE CONVERTER	Input	Used to gate the ADC on or off. Pulses in progress prior to initiation of this signal will be allowed to finish the output sequence; further inputs will be ignored. Positive true logic. TTL hysteresis input with a 4.7k ohm pull-up resistor to 5 V.
14	$\overline{\text{INV}}$	Output	Invalid; set by digital under or overflow (OVF) if the ADC input is not within the SCA window or does not exceed the ZERO intercept setting. Invalid may also be set if the linear input with a COINC Gate signal is not large enough to cause conversion. The $\overline{\text{INV}}$ signal is reset by the DATA ACCEPTED signal. Negative true logic. TTL output with a 4.7k ohm pull-up resistor to 5 V.
16	DEAD TIME	Output	Used to enable live time circuitry to control storage periods. Positive true or negative true logic, set by internal jumper J10; shipped in negative true. TTL output with a 4.7k ohm pull-up resistor to 5 V.
18	ENABLE DATA	Input	Used to gate the 14-bit data onto the output lines. Positive true or negative true logic, set by internal jumper J6; shipped in negative true; hysteresis input with a 4.7 k ohm pull-up resistor to 5 V.
20	$\overline{\text{INT}}$	Pass-through	Intensify; originates in a Digital Stabilizer and passed directly to the memory storage unit. This signal is used to aid in determining the proper settings of the peak and window controls of the Stabilizer. Negative true logic.
22	GND		Ground.
26	-12 V	Output	

A.2 J103 - STABILIZER

Pin	Signal	In/Out	Description
1	$\overline{SA2^0}$	Output	
3	$\overline{SA2^1}$	Output	
5	$\overline{SA2^2}$	Output	
7	$\overline{SA2^3}$	Output	
9	$\overline{SA2^4}$	Output	
11	$\overline{SA2^5}$	Output	Binary address data; negative true logic; data is valid when STAB TRIG is true (low); TTL - LS outputs. $V_o > 3$ V @ 20 mA (High) $V_o < 0.9$ V @ 20 mA (Low)
13	$\overline{SA2^6}$	Output	
15	$\overline{SA2^7}$	Output	
17	$\overline{SA2^8}$	Output	
19	$\overline{SA2^9}$	Output	
21	$\overline{SA2^{10}}$	Output	
23	$\overline{SA2^{11}}$	Output	
24	$\overline{SA2^{12}}$	Output	
4	$\overline{SA2^{13}}$	Output	
6	$\overline{INHAD}$	Pass-through	Inhibit Add; this signal comes from the Digital Stabilizer and is passed directly to the memory storage unit. It is used to prevent storage of a reference peak from a pulser. Negative true logic.
12	INT	Pass-through	Intensify; originates in the Digital Stabilizer and passes directly to the memory storage unit. This signal is used to aid in determining the proper settings of the peak and window controls of the Stabilizer. Negative true logic.
14	STAB GAIN	Input	Gain correction; an analog voltage from the Stabilizer. It is used to correct ADC Gain drifts. $Z_{in} \approx 5$k ohms; ± 5 V input yields a gain change of $\approx \pm 5\%$ of full scale.
16	STAB ZERO	Input	Zero correction; an analog voltage from the Stabilizer. It is used to correct ADC Zero drifts. $Z_{in} \approx 9.5$k ohms; ± 5 V input yields a zero change of $\approx 6 \pm 2\%$ of full scale.
20	STAB TRIGGER	Output	Stabilizer Trigger; positive true logic pulse; provides stabilizer data sample window. About 1 μsec wide.
22	GND		Ground
26	-12 V	Output	

A.3 J104 - PUR

Pin	Signal	In/Out	Description
1	$\overline{LG}$	Output	Linear Gate; provides a negative true logic signal; logic low when the ADC accepts an input. Initiated when the input signal exceeds the input reference threshold; returns to a logic high at the end of the ADC acquisition cycle. TTL output through a 47 ohm series resistor. 4.7k ohm pull-up resistor to 5 V.
2	REJ	Input	Reject; receives a positive true logic signal which is used to initiate an ADC reject sequence. It must occur during and remain active until the end of the ADC's LG signal. At this point, the conversion attempt will be aborted. Amplitude: 2.5 to 7 V; width $\geq$ 50 nsec; loading $\leq +800$ mA at +3 V.
3	GND	Input	Ground

A.4 J101 - DEAD TIME

A rear panel BNC dual-function connector: external dead time INPUT or ADC dead time OUTPUT. Either of these modes can be internally selected with a jumper plug (J9). Shipped in the INPUT mode.

INPUT - Accepts a negative true logic signal which is ORed with the ADC dead time. This composite dead time signal may be seen at pin 16 of the rear panel DATA connector. Logic low when true; amplitude $\leq$ 400 mV; 0 to +7 V maximum; loading $<$ -1.4 mA at 400 mV.

OUTPUT - Provides a logic signal representing the ADC acquisition and conversion times; an internal jumper plug (J10) provides the option of POSitive true or NEGative true logic pulse signal; shipped in the POSitive true position. TTL compatible totem-pole output (LS) with a 4.7 k ohm pull-up resistor to 5 V.

Appendix B
Setup for use with a Model 8220 Mixer/Router

The Model 8220 Mixer/Router has a full-scale range of 8 V, but the Model 8077 ADC is shipped calibrated for a 10 V full-scale range. To make the Model 8077 compatible with the Model 8220:

1. Remove the Model 8077's left side-cover.
2. Locate resistor R53 (see Figure 3.3).
3. Remove this socketed 4.12 k ohm resistor.
4. Replace it with a 3.12 k ohm 1% (RN60C) resistor.

To adjust the full-scale range, a Model 8210, or equivalent, Precision Pulser will be needed.

5. Connect the Pulser's OUTPUT to the ADC's INPUT paralleled to an oscilloscope with a "tee" connector.
6. Connect the ADC's DATA output to an Analyzer.
7. Set the Pulser for 2 μsec Rise Time, Positive (+) output, and adjust the GAIN controls for an 8 V output, as seen on the scope.
8. Set the ADC's GAIN control to equal the Analyzer's full memory size.
9. Enable COLLECT on the Analyzer and adjust RV2 on the ADC so that the 8 V input is collecting in the Analyzer's highest channel. It will be helpful to place the Analyzer's cursor in the highest channel and enable EXPAND.
10. Remove the ADC from the calibration setup and replace the side cover.

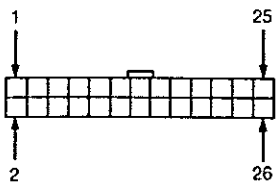
Appendix C
Cable Connections

C-8075-A
CABLE INTERFACE FOR J102

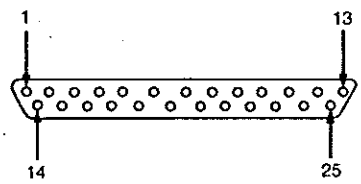
J102 END		EXTERNAL USER END
1	$\overline{2^0}$	1
2	DATA READY	14
3	$\overline{2^1}$	2
4	$\overline{2^{13}}$	15
5	$\overline{2^2}$	3
6	$\overline{\text{INHAD}}$	16
7	$\overline{2^3}$	4
8	DATA ACCEPTED	17
9	$\overline{2^4}$	5
10	ENABLE CONVERTER	18
11	$\overline{2^5}$	6
12	NOT USED	19
13	$\overline{2^6}$	7
14	$\overline{\text{INV}}$	20
15	$\overline{2^7}$	8
16	DEAD TIME	21
17	$\overline{2^8}$	9
18	ENABLE DATA	22
19	$\overline{2^9}$	10
20	$\overline{\text{INT}}$	23
21	$\overline{2^{10}}$	11
22	GND	24
23	$\overline{2^{11}}$	12
24	NOT USED	25
25	$\overline{2^{12}}$	13
26	- 12 V	NOT USED

C-8075-B
CABLE INTERFACE FOR J102

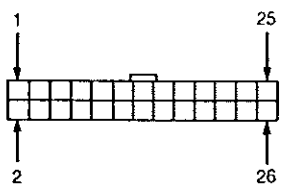
J102 END		EXTERNAL USER END
1	$\overline{2^0}$	1
2	DATA READY	2
3	$\overline{2^1}$	3
4	$\overline{2^{13}}$	4
5	$\overline{2^2}$	5
6	$\overline{\text{INHAD}}$	6
7	$\overline{2^3}$	7
8	DATA ACCEPTED	8
9	$\overline{2^4}$	9
10	ENABLE CONVERTER	10
11	$\overline{2^5}$	11
12	NOT USED	12
13	$\overline{2^6}$	13
14	$\overline{\text{INV}}$	14
15	$\overline{2^7}$	15
16	DEAD TIME	16
17	$\overline{2^8}$	17
18	ENABLE DATA	18
19	$\overline{2^9}$	19
20	$\overline{\text{INT}}$	20
21	$\overline{2^{10}}$	21
22	GND	22
23	$\overline{2^{11}}$	23
24	NOT USED	24
25	$\overline{2^{12}}$	25
26	- 12 V	NOT USED



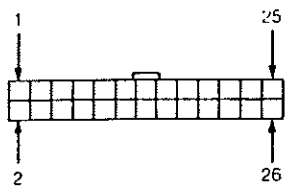
26 Pin Ansley Connector
CI 45-30-0033
Ansley 609-2600M



25 Pin D Connector
CI 45-21-1512
Ansley 609-25P



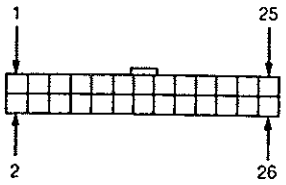
26-Pin Socket Connector
CI 45-30-0033
Ansley 609-2600M



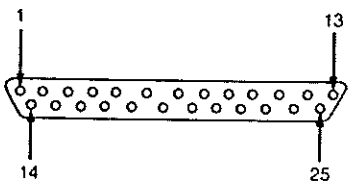
26-Pin Socket Connector
CI 45-30-0033
Ansley 609-2600M

C-8075-A
CABLE INTERFACE FOR J103

J103 END		EXTERNAL USER END
1	$\overline{SA2^0}$	1
2	NOT USED	14
3	$\overline{SA2^1}$	2
4	$\overline{SA2^{13}}$	15
5	$\overline{SA2^2}$	3
6	$\overline{INHAD}$	16
7	$\overline{SA2^3}$	4
8	NOT USED	17
9	$\overline{SA2^4}$	5
10	NOT USED	18
11	$\overline{SA2^5}$	6
12	$\overline{INT}$	19
13	$\overline{SA2^6}$	7
14	STAB GAIN	20
15	$\overline{SA2^7}$	8
16	STAB ZERO	21
17	$\overline{SA2^8}$	9
18	$\overline{RST}$	22
19	$\overline{SA2^9}$	10
20	STAB TRIGGER	23
21	$\overline{SA2^{10}}$	11
22	GND	24
23	$\overline{SA2^{11}}$	12
24	NOT USED	25
25	$\overline{SA2^{12}}$	13
26	- 12 V	NOT USED



26-Pin Socket Connector
CI 45-30-0033
Ansley 609-2600M



25-Pin D Connector
CI 45-21-1512
Ansley 609-25P

Request for Schematics

Schematics for this unit are available directly from Canberra. Write, call or FAX:

Training and Technical Services Department
Canberra Industries, Inc.
800 Research Parkway, Meriden, CT 06450
Telephone: (800) 255-6370 or (203) 639-2467
FAX: (203) 235-1347

If you would like a set of schematics for this unit, please provide us with the following information.

Your Name _____

Your Address _____

_____

_____

_____

_____

Unit's model number _____

Unit's serial number _____

Note: Schematics are provided for information only; if you service or repair or try to service or repair this unit without Canberra's written permission you may void your warranty.

WARRANTY

This warranty covers Canberra hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Equipment manufactured by Canberra's Instruments Division, Detector Products Division, and Nuclear Systems Division is warranted against defects in materials and workmanship for one year from the date of shipment.

Canberra warrants proper operation of its software only when used with software and hardware supplied by Canberra and warrants software media to be free from defects for 90 days from the date of shipment.

If defects are discovered within 30 days of the time you receive your order, Canberra will pay transportation costs both ways. After the first 30 days, you will have to pay the transportation costs.

This is the only warranty provided by Canberra; there are no other warranties, expressed or implied. All warranties of merchantability and fitness for an intended purpose are excluded. Canberra shall have no liability for any special, indirect or consequential damages caused by failure of any equipment manufactured by Canberra.

EXCLUSIONS

This warranty does not cover equipment which has been modified without Canberra's written permission or which has been subjected to unusual physical or electrical stress as determined by Canberra's Service Personnel.

Canberra is under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by abuse, neutrons, or heavy charged particles.

SHIPPING DAMAGE

Examine shipments carefully when you receive them for evidence of damage caused in transit. If damage is found, notify Canberra and the carrier immediately. Keep all packages, materials and documents, including your freight bill, invoice and packing list. Although Canberra is not responsible for damage sustained in transit, we will be glad to help you in processing your claim.

OUT OF WARRANTY REPAIRS

Any Canberra equipment which is no longer covered by warranty may be returned to Canberra freight prepaid for repair. After the equipment is repaired, it will pass through our normal pre-shipment checkout procedure.

RETURNING EQUIPMENT

Before returning equipment for repair you must contact your Regional Service Center or one of our factories for instructions. For detector repair, contact the Canberra Detector Division in our Meriden, Connecticut, factory for instructions. If you are going to return the equipment to the factory, you must call first to get an Authorized Return Number (ARN).

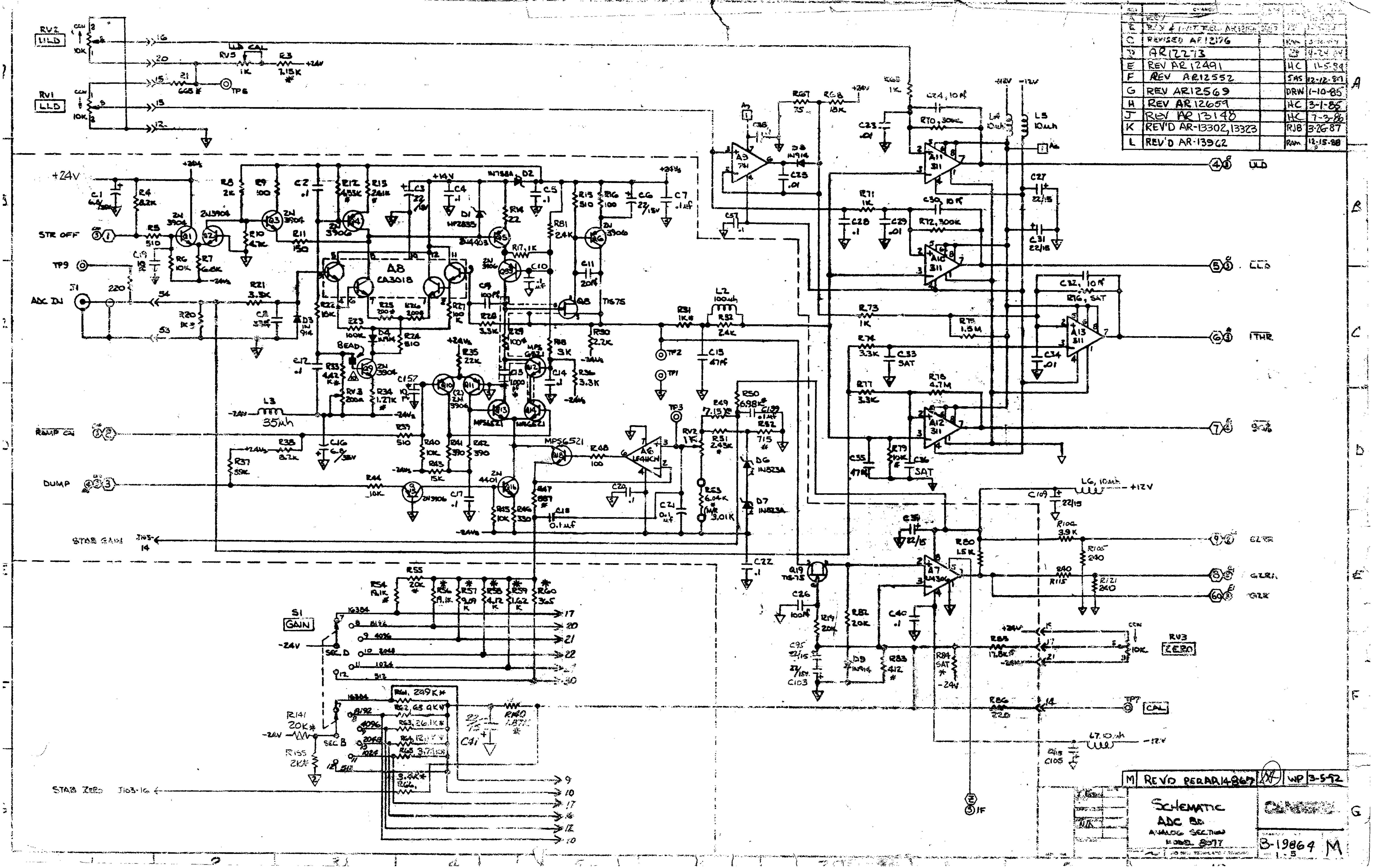
When you call us, we will be glad to suggest the best way for you to ship the equipment and will expedite the shipment in case it is delayed or lost in transit. Giving you shipping advice does not make us responsible for the equipment while it is in transit.

SOFTWARE LICENSE

You have purchased the license to use Canberra software, not the software itself. Since title to this software remains with Canberra, you may not sell or transfer this software. This license allows you to use this software on only one compatible computer at a time. You must get Canberra's written permission for any exception to this license.

BACKUP COPIES

Canberra's software is protected by United States Copyright Law and by International Copyright Treaties. You have Canberra's express permission to make one archival copy of this software for backup protection. You may not copy Canberra software or any part of it for any other purpose.



C	REVISED AR12176	
D	AR12273	4-24-84
E	REV AR12491	HC 11-5-84
F	REV AR12552	SAS 12-12-84
G	REV AR12569	DRW 1-10-85
H	REV AR12659	HC 3-1-85
J	REV AR13148	HC 7-3-86
K	REV'D AR-13302, 13323	RJB 3-26-87
L	REV'D AR-13962	RAM 12-15-88
M	REVD PER AR14867	WP 3-5-92

SCHEMATIC
ADC BD.
ANALOG SECTION
MODEL 8077

B-19864 M

REV	CHANGE			
A				
B	INIT. REL AR12156	3687	LP	11-23-84
C	REVISED PER 12715		RAM	1-12-84
D	AR12273		LP	4-24-84
E	REV AR12491		MC	11-15-84
F	REV AR12552		SFS	11-12-84
G	REV AR12569		DRW	1-10-85
H	REV AR12659		MC	3-1-85
J	REV AR13148		MC	7-3-85
K	REV'D AR13302, 13325		RP	3-26-87
L	REV'D AR13962		RA	12-15-88
M	REV'D AR14867	(X)	WP	3-5-92

SCHEMATIC
A.D.C. BD
JOINT UNIT

MODEL

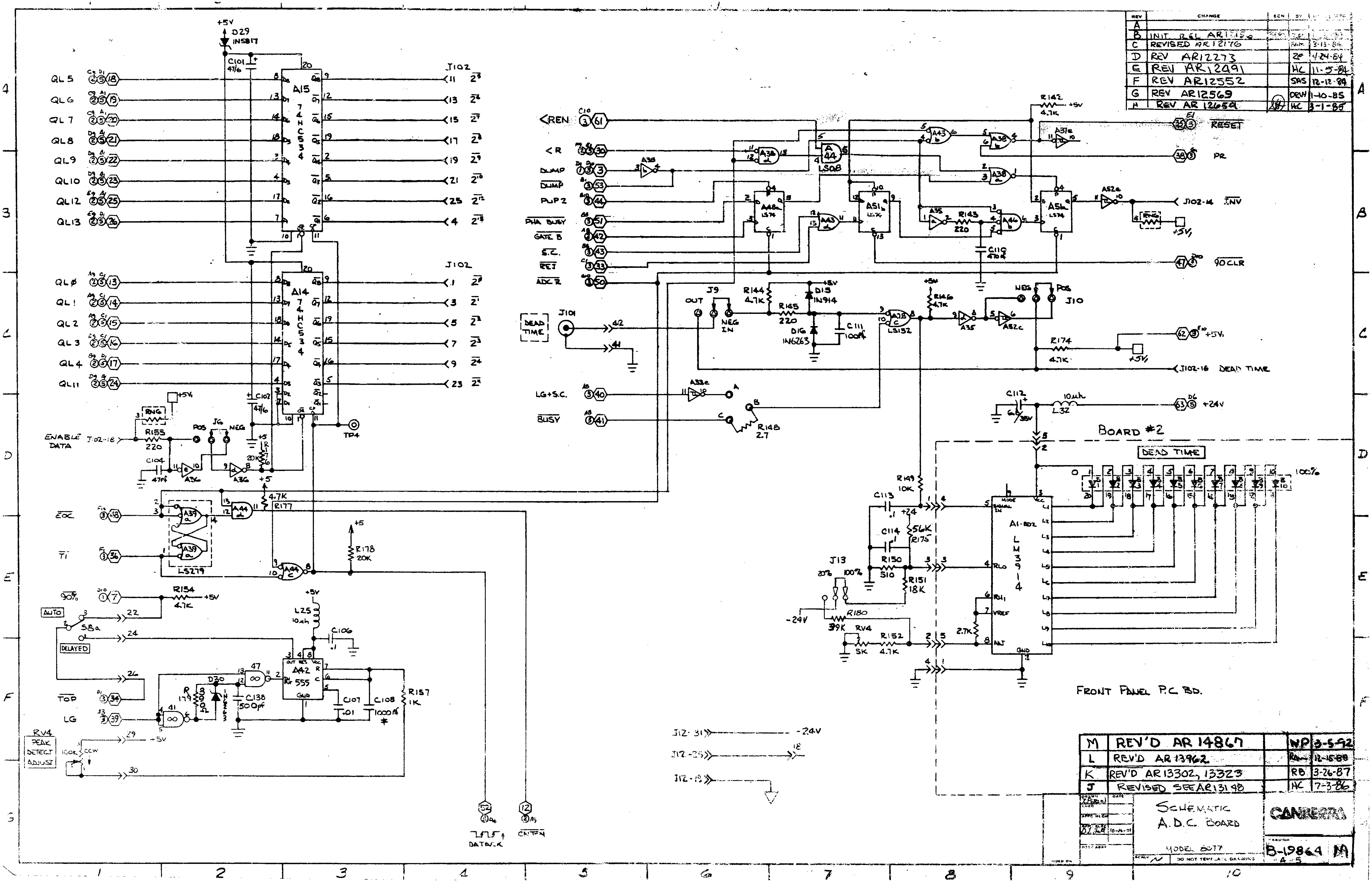
B 19864 M
2 5

REV	CHANGE	ECN	BY	DATE
A				
B	INIT. REL AR12236			
C	REVISED AR12176		RAM	2-13-84
D	AR12273		SP	4-24-84
E	REV AR12491		HC	11-5-84
F	REV AR12552		SPS	12-12-84
G	REV AR12569		DRW	1-10-85
H	REV AR12659		HC	3-1-85
J	REV AR13148		HC	7-3-86
K	REV.D AR 13302, 13323		RB	3-26-87
L	REV'D AR 13962		RAM	12-15-88
M	REV'D AR 14867	M	NP	3-5-92

SCHEMATIC
A.D.C. BOARD
CONTROL LOGIC
MODEL 8077

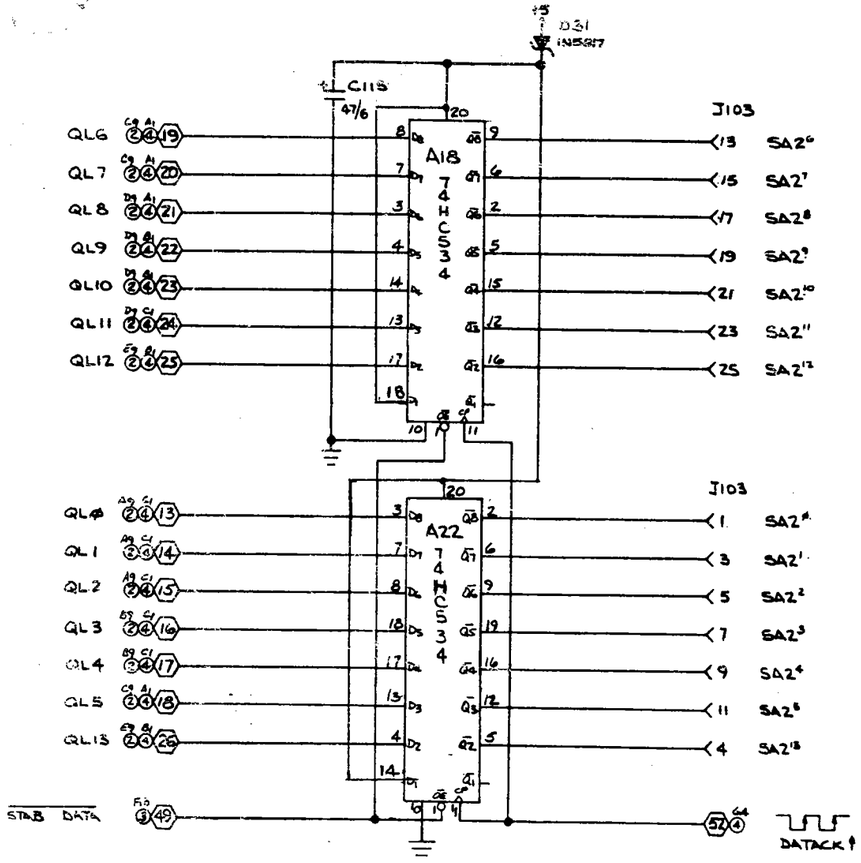
CAMBRIA

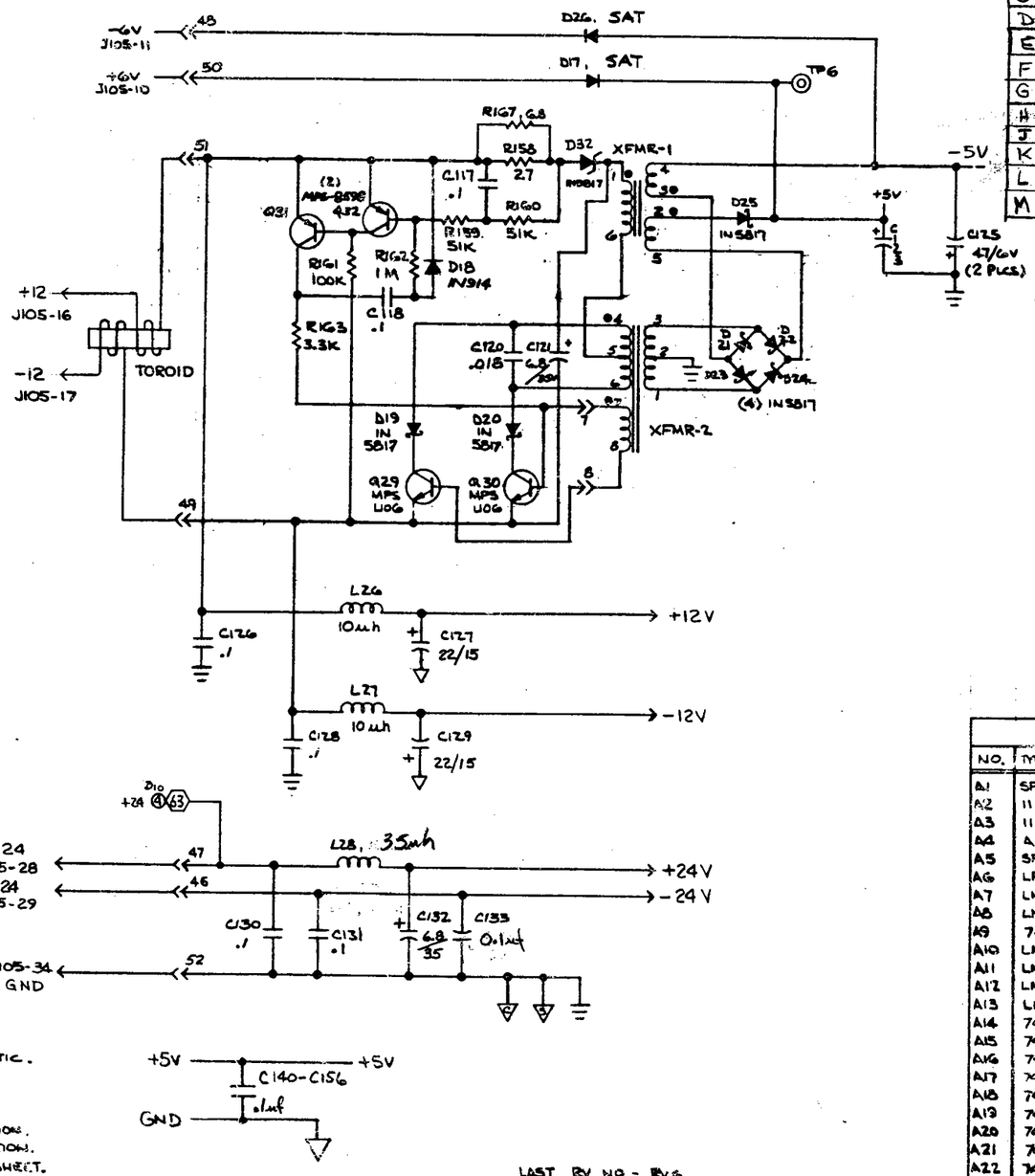
B-19864 M
3 of 5

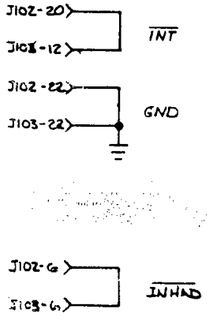


SCHEMATIC A.D.C. BOARD
CANBERRA
MODEL 8077
B-19864 M
DO NOT REPLACE DRAWING
FRONT PANEL P.C. BD.
BOARD #2
DEAD TIME
A INIT REL AR...
C REVISED AR12176 3-15-84
D REV AR12273 4-24-84
E REV AR12491 11-5-84
F REV AR12552 12-12-84
G REV AR12569 1-10-85
H REV AR12659 3-1-85
M REV'D AR 14867 WP 3-5-92
L REV'D AR 13962 12-15-88
K REV'D AR 13302, 13323 RB 3-26-87
J REVISED SEE AR13148 HC 7-3-86
A15 74HC534
A14 74HC534
J102
QL5 QL6 QL7 QL8 QL9 QL10 QL12 QL13
QLØ QL1 QL2 QL3 QL4 QL11
D29 IN5817
C101 47/6
C102 47/6
ENABLE DATA
R155 220
C104 47pf
A36
TP4
EOC
TI
LS279
A39
A44
R177 4.7K
R178 20K
90% R154 4.7K +5V
AUTO
DELAYED
S8a
L25 10uh
C106 .1
A42 555
R157 1K
C107 .01
C108 1000uf
C138 500pf
D30
TOP
LG
RV4 PEAK DETECT ADJUST
DATACLK
CNTEN
REN
R
DUMP
PUP2
PHA BUSY
GATE B
S.C.
REJ
ADC R
RESET
PR
90CLR
INV
J101
DEAD TIME
J9 OUT NEG IN
R144 4.7K
R145 220
D15 1N914
D16 1N6263
C111 100pf
R146 4.7K
R143 220
C110 470pf
R142 4.7K
R174 4.7K
J10 NEG POS
J102-16 DEAD TIME
LG+S.C.
BUSY
R148 2.7
C112 6.8/35V
L32 10uh
+24V
A1-802 LM3914
C113
C114
R175 56K
R150 510
R151 18K
R149 10K
J13 20% 100%
R180 39K
RV4 5K
R152 4.7K
-24V

REV	CHANGE	FOR	BY	DATE
A				
B	INIT. REL AR12156	3687	JF	2-29-84
C	REVISED AR12176		RAM	3-13-84
D	AR12273		JF	4-24-84
E	REV AR12491		HC	11-5-84
F	REV AR12552		SAS	12-12-84
G	REV AR12569		DRW	1-10-85
H	REV AR12659		HC	3-1-85
J	REV AR13148		HC	7-3-86
K	REV AR13302, 13323		RJB	9-26-87
L	REV AR13962		RA	12-15-88
M	REV'D AR14867	W	WP	5-5-92







NOTES:

1. THERE ARE NO 4-WAY TIES ON THIS SCHEMATIC.
2. UNLESS NOTED ALL CAPACITORS ARE IN μf.
3. ✱ INDICATES MONO COG CAPACITORS.
4. ✱ INDICATES RN55 RESISTORS.
5. ▭ INDICATES FRONT PANEL COMPONENT LOCATION.
6. ▭ INDICATES REAR PANEL COMPONENT LOCATION.
7. A1 1 SQUARE INDICATES CONNECTION SAME SHEET.
   REF. NO.
   COORDINATES SQUARE IS FOUND AT.
8. A1 01 HEX INDICATES INTER-SHEET CONNECTIONS.
   REF. NO.
   INDICATES WHAT SHEET HEX APPEARS ON
   COORDINATES HEX IS FOUND AT.
9. S INDICATES WIRE POINT
   REF NO.
10. FERRITE BEAD ICN 2030008

LAST RV NO. - RV6
LAST R NO. - R182
LAST C NO. - C156
LAST D NO. - D32
LAST L NO. - L32
LAST Q NO. - Q34

INTEGRATED CIRCUITS

NO.	TYPE I.C.	OPEN GATES	NO.	TYPE I.C.	OPEN GATES
A1	SP8T35A		A21	74LS02	
A2	11C70		A22	74LS00	c,d
A3	11C70		A23	74LS14	
A4	AMG85		A24	74LS157	
A5	SP8T35B		A25	74LS04	
A6	LF411CN		A26	74LS14	a
A7	LM306		A27	74LS14	
A8	LM311		A28	74LS02	
A9	741		A29	74LS279	
A10	LM311		A30	74LS27	
A11	LM311		A31	74LS00	
A12	LM311		A32	NE555	
A13	LM311		A33	74LS00	a
A14	74HC534		A34	74LS08	b
A15	74HC534		A35	74LS74	
A16	74HC86		A36	74LS27	
A17	74HC86		A37	74LS00	d
A18	74HC534		A38	74LS74	
A19	74LS197		A39	74LS221	
A20	74LS197		A50	74LS221	
A21	74LS08	d	A51	74LS74	
A22	74HC534		A52	74LS14	
A23	74LS04	e,f			
A24	74LS27	b			
A25	74LS02				
A26	74LS08	c,ap			
A27	74LS02	d			
A28	74LS152	b			
A29	74LS74				
A30	74LS02	c			

DRAWN JF 4-24-84
CHK'D
ENG APPR
MFG APPR
QUAL CK
USED ON

SCHEMATIC
A.D.C. BOARD
MODEL 8077

DO NOT TRANSLATE DRAWING

B19864 M
5-5