PROGRAMMABLE ANALOG-TO-DIGITAL CONVERTER Model 8076

1185

Operator's Manual

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

M184R3 11/85 Printed in U.S.A.

Addition to the 8076 Manual

No more than four (4) 8076 ADCs can be supported by the Series 90's NIM Bin power supply.

Additional 8076s will require a separate Model 2100 NIM Bin, or equivalent.

Table of Contents

Section 1. Introduction

The Canberra Model 8076 is a single-width NIM style analog-to-digital converter for applications in nuclear and X-ray spectroscopy. This unit incorporates a Wilkinson-type counter/ramp-converter with a clock rate of 100 MHz for fast operation.

The Model 8076 is compatible with the Canberra Acquisition Bus (CAB) which allows up to eight compatible modules to be connected to a Series 90 MCA via the 9132 Collect Interface. Gain, Range, Offset, ULD and LLD are programmable by way of the CAB. The Canberra Acquisition Bus is capable of interfacing to Modules up to 6.0 meters away.

A direct-coupled input of 0 to +10 V is digitized according to the programmed GAIN into binary code spans of 8 through 13 bits (256 through 8192 channels). The RANGE is set by the Series 90 to equal the number of channels assigned to the associated memory group. The GAIN can be programmed to be less than the assigned RANGE. This is useful when data is to be transferred to a memory group with a smaller capacity than the overflow limit of the selected RANGE. The user may use a small memory group and with high GAIN and digital OFFSET analyze a part of the spectrum.

GAIN, OFFSET, LLD, and ULD are set via the Series 90's dialogue.

The front panel ZERO adjustment is a 22-turn screwdriver-adjusted potentiometer; its setting can be monitored at the adjacent CAL test point and covers ± 5% of full scale input range.

Conversion for the Pulse Height Analysis (PHA) mode can be initiated AUTOmatically using an internal constant-fraction peak detector operating on the trailing edge of the input pulse, or can be DELAYED up to 100 μsec after the leading edge of the input pulse passes the LLD. A front panel INSPect test point is provided so that the user can monitor the Linear Gate (LG) time between LLD crossing and the beginning of conversion for either mode. Conversions may be enabled/disabled by the COINCidence/ANTIcoincidence gating applied at any time during the Linear Gate interval.

Conversion for the Sample Voltage Analysis (SVA) mode is initiated by the falling edge of a GATE pulse applied in the COINCidence mode. The same LLD and ULD limits are used for acceptance of an input level for conversion in this mode.

The Model 8076 is compatible with the Model 8222A Mixer/Router and with the Model 8232 Digital Stabilizer. An additional 3-pin pileup rejector (PUR) connector is provided on the rear panel for direct interface to the Canberra Model 2020 Amplifier which includes pileup rejection circuitry.

Section 2. Specifications

2.1 INPUTS

ADC IN - Accepts positive unipolar or bipolar (positive lobe leading) pulses for PHA, and dc level or pulses for SVA mode; amplitude 0 to +10 V, +12 V maximum; rise time 0.25 to 100 μsec maximum; width 0.5 μsec minimum; input impedance 1 kilohm, direct coupled; front panel BNC and test point.

GATE IN - Accepts positive logic pulse or dc level; amplitude ≥ 2.5 to 7 V maximum; dc coupled; with COINCidence or SVA selected loading ≤ -100 μA at +3 V and ≤ +800 μA for ANTIcoincidence; width ≥ 250 nsec; PHA analysis does not require a gate input. For SVA, pulse width ≥ 1 μsec.

2.2 OUTPUTS

DATA - Provide Data, Address and Control lines compatible with Canberra Acquisition Bus. Rear panel 34-pin block connector.

MIXER/ROUTER - Provides routing bits and control signals which allow the 8076 to function with 8222A Mixer/Router. Control signals permit independent acquisition-enable of 1 to 4 inputs with single 8222A or 1 to 4 groups with multiple 8222As. Rear panel 26-pin block connector.

STABILIZER - Provides 13 binary TTL-compatible lines and the trigger commands required for the Model 8232 Digital Stabilizer; rear panel 26-pin block connector. Data

lines are negative true. Stabilizer Control range for ± 5 V input and 1 kilohm source impedance; zero: ± 2%; gain: ± 5%.

PILEUP REJECTOR/LIVE TIME CORRECTOR - Accepts REJECT and Live Time signals from Canberra Model 2020 Amplifier; also provides Linear Gate to that unit for full interactive operation; rear panel 3-pin Molex connector for use with Molex Cable, Model C1514.

REJect - Receives a positive true logic pulse used to initiate an ADC reject sequence; must occur and remain stable until the ADC Linear Gate (LG) Signal concludes; amplitude ≥ 2.5 to 7 V; width ≥ 50 nsec; loading ≤ +800 μA at +3 V. Accessible through pin 1 of rear panel PUR connector.

LG - Provides a negative true logic signal; logic low when ADC accepts input, returns to a logic high at the ADC acquisition cycle conclusion. TTL compatible totem pole output (LS) through 47 ohm series resistor. Accessible through pin 2 of rear panel PUR connector.

DEAD TIME - Rear panel LEMO connector having a dual-function capability; external dead time INPUT or ADC dead time OUTPUT; one of these modes is internally selected with jumper plug J9; shipped in the NEG INput position. When used as:

NEG INput - Accepts a negative logical signal which is ORed with the ADC dead time.

OUT - Provides logic signal representation of the ADC acquisition and conversion times; internal jumper plug J10 provides the option of positive true or negative true logic pulses; shipped in the POS position. TTL compatible, totem pole output (LS) with 4.7 k pull-up resistor.

2.3 PROGRAMMABLE CONTROLS - VIA SERIES 90

GAIN - Programmable settings of 256, 512, 1024, 2048, 4096 or 8192 channels for a 10 V pulse or level.

RANGE - Programmed settings of 256, 512, 1024, 2048, 4096 or 8192 channels as the overflow limit and the limit of the address information sent to the interface.

OFFSET - Programmable from 0 to 8064 channels in increments of 128 channels.

LLD - Programmable from 0 to 110% (0 to 11 V) in 1024 equal increments. (Approximately 10 millivolts per increment)

ULD - Programmable from 0 to 110% (0 to 11 V) in 256 equal increments. (Approximately 40 millivolts per increment)

2.4 FRONT PANEL CONTROLS

ZERO - Screwdriver adjusted 22-turn potentiometer sets the input analog zero level; range ± 5% of input range; resolution 0.005% of full scale. Adjacent CALibration test point monitors adjustment voltage.

PEAK DETECT - Toggle switch to select either AUTOmatic or DELAYED initiation of conversion cycle. In AUTOmatic an internal constant-fraction trigger operates on the falling edge of the input pulse. In DELAYED mode the conversion begins at a selected time after the rising edge of the input passes the selected LLD. An ADJustment potentiometer permits selection of from 2 to 100 μsec delay. An INSPect test point is provided to monitor the Linear Gate time delay adjustment, or for time sync of an applied GATE pulse input.

COINC/ANTI - Toggle switch to select either the COINCidence or the ANTIcoincidence mode of the GATE input pulse to enable or to disable respectively a given conversion cycle. Pulse must be present during the Linear Gate time as monitored on the INSPect test point.

PHA/SVA - Toggle switch to select either Pulse Height Analysis or Sample Voltage Analysis modes of conversion. In PHA the input pulse must start below the threshold level to be accepted for conversion. In SVA a varying input dc level or pulse can be acquired while the GATE input is high, and captured for conversion on the negative (falling) edge of the GATE input.

2.5 INDICATORS

DEAD TIME - Ten-segment LED indicator displays the average dead time of the converter.

ACTIVE - LED Indicator is lighted if collect has been enabled

2.6 PERFORMANCE

INTEGRAL NONLINEARITY - Less than ± 0.025% of full scale over the top 99.5% of selected range.

DIFFERENTIAL NONLINEARITY - Less than ± 0.7% over the top 99.5% of range including effects from tilt.

DRIFT - Gain - less than ± 0.009% of full scale/°C
Zero - less than ± 0.0025% of full scale/°C
Long Term - less than ± 0.005% of full scale/24 hours at a constant temperature.

PEAK SHIFT - Less than ± 0.025% of full scale at rates up to 50 kHz.

ADC DEAD TIME - Linear Gate Time + Conversion Time + Transfer Time.

CONVERSION TIME - 1.5 μsec + 0.01 (N + X) μsec where N = address count, and X = effective digital OFFSET.

TRANSFER TIME is the time required to store the ADC value in a small buffer memory. If this memory is not full the transfer takes 2.4 μsec.

CHANNEL PROFILE - Typically flat over 90% of channel width.

OPERATING TEMPERATURE RANGE - 0° to 50° C.

2.7 POWER REQUIREMENTS

+24 V - 80 mA	+12 V - 180 mA*
-24 V - 80 mA	-12 V - 180 mA*
+6 V - 1.0 A	

*Exceeds the NIM power allotment for a single-width module.

2.8 PHYSICAL

SIZE - Standard single width NIM module 3.43 × 22.12 cm (1.35 × 8.71 inches) per TID-20893 (rev.)

OPERATING TEMPERATURE RANGE - 0° to 45° C with adequate air flow.

NET WEIGHT - 0.9 kg (1.9 lbs).

SHIPPING WEIGHT - 1.8 kg (4.0 lbs).

Section 3.
Controls and Connectors

3.1 FRONT PANEL

Refer to Section 2 for additional information and signal specifications.

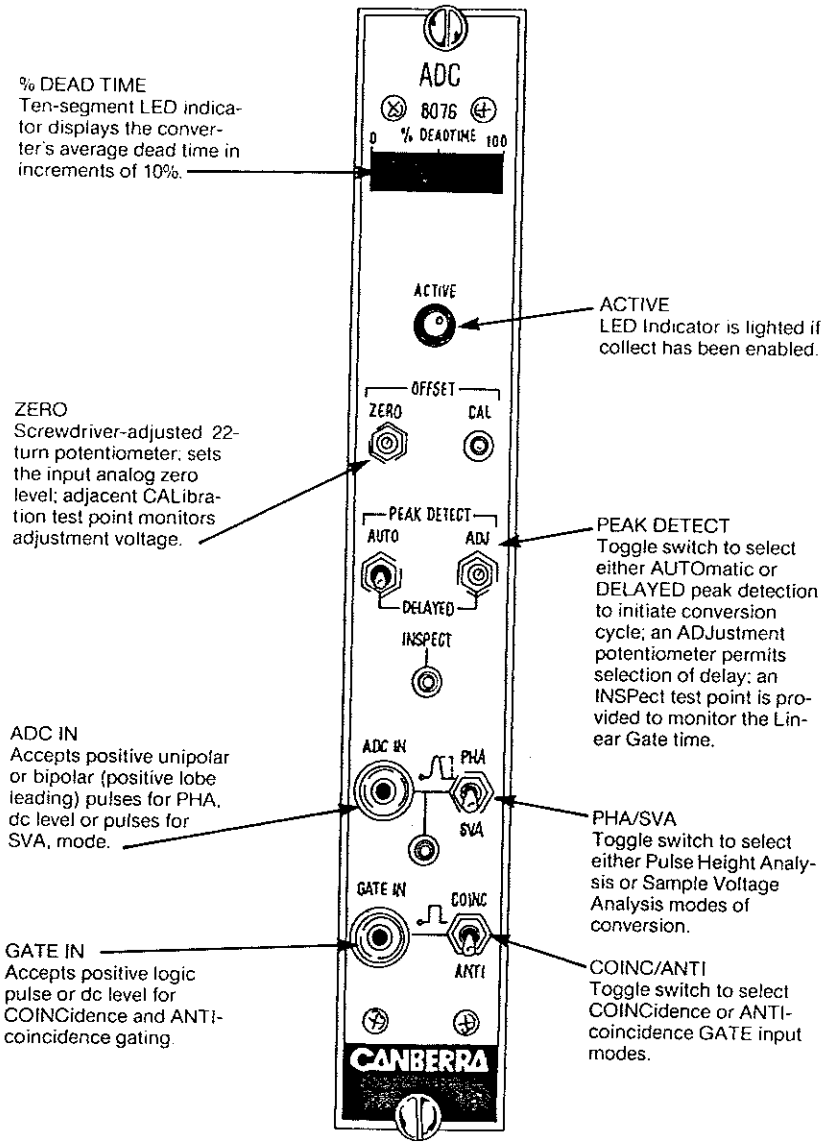

Figure 3.1
Front Panel

3.2 REAR PANEL

Refer to Section 2 for additional information and PUR signal specifications and to Appendix B for Data and Stabilizer signal specifications.

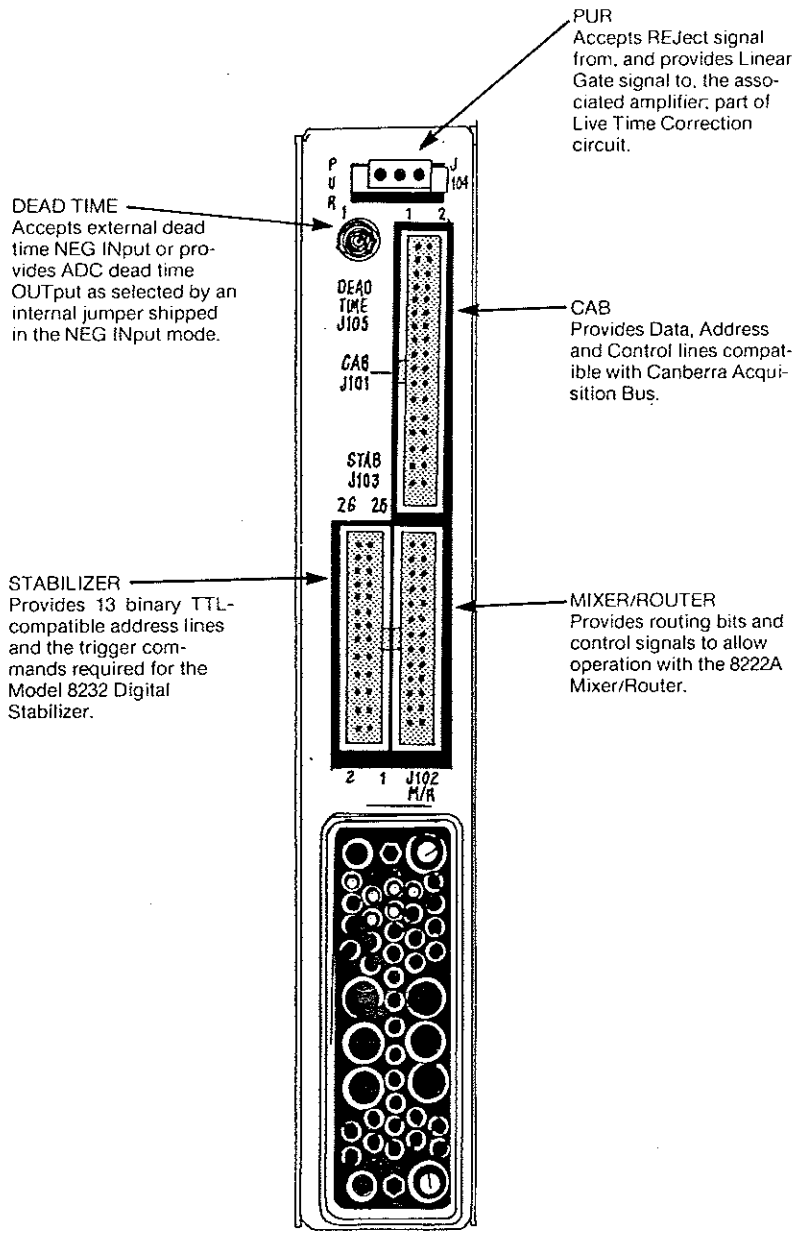

Figure 3.2
Rear Panel

3.3 INTERNAL CONTROLS

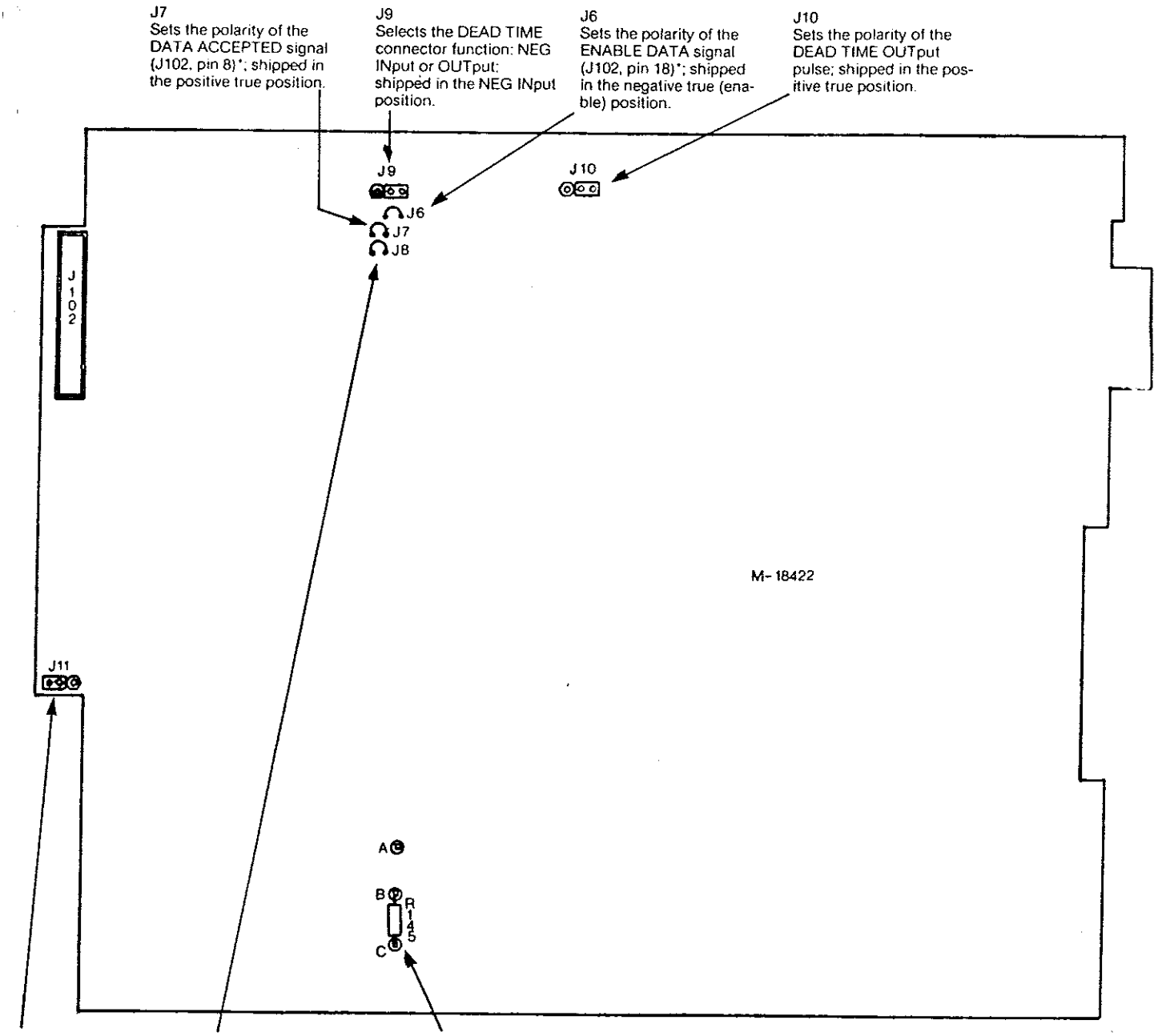

Figure 3.3
ADC Board

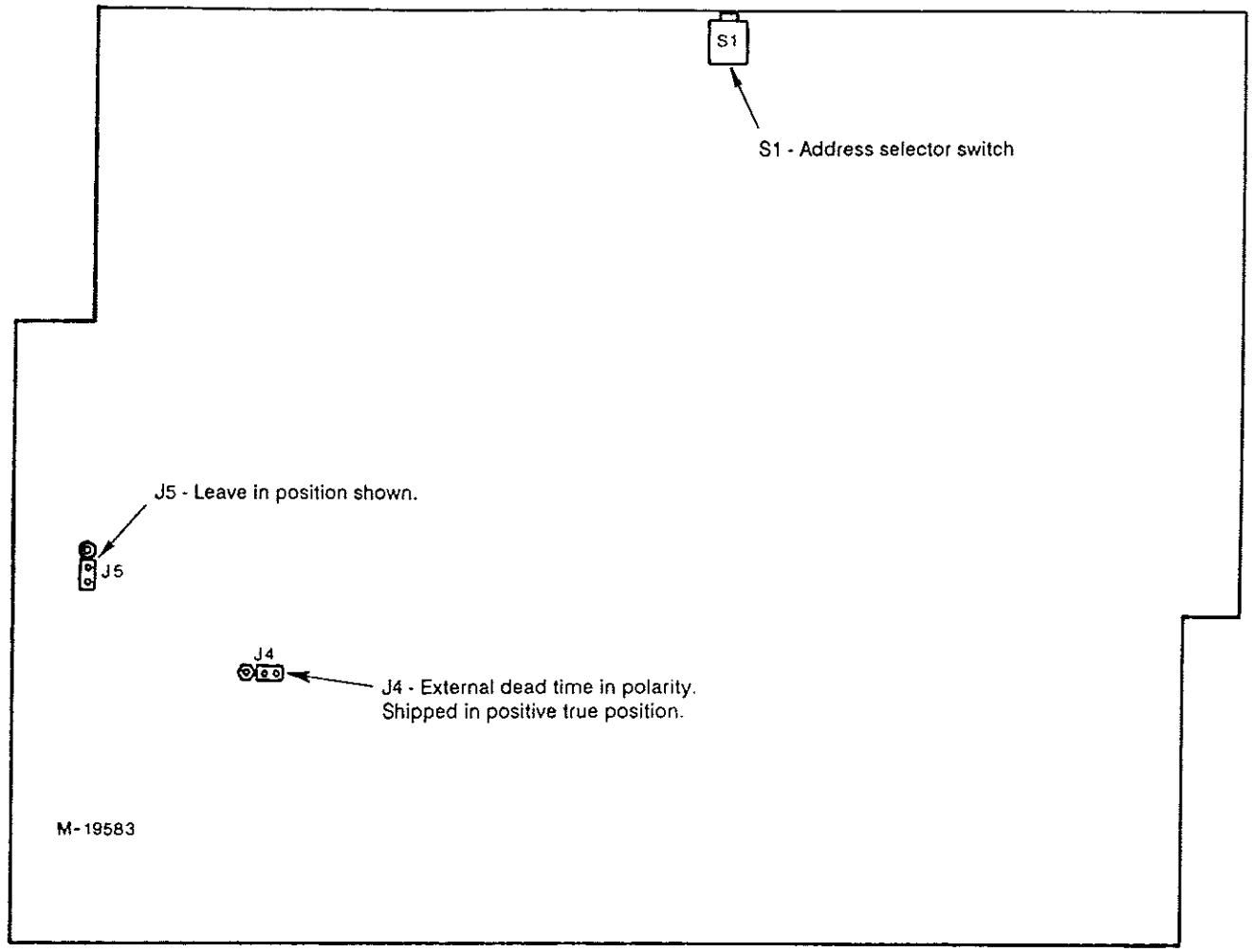

Figure 3.4
Remote Interface Board

Section 4. Operation

The Model 8076's ADC Gain, Offset, LLD, and ULD are set remotely via the Series 90's Current User-Configure Group dialogue. Each of these functions is described in the following sections.

4.1 % DEAD TIME

The DEAD TIME indicator is a ten-segment LED display which shows the average dead time in increments of ten percent. Dead time is the time that the ADC is busy converting an input and increases proportionately with increases in gain and/or conversions per unit time.

4.2 GAIN

The GAIN controls the ADC's resolution; that is, the number of parts into which the full-scale (10 V) inputs can be divided. The larger the selected gain, the finer the divisions and the greater the resolution.

Higher gains take longer to make a conversion from analog to digital form, which increases the dead time. With GAIN set to 8192 and no OFFSET, the maximum conversion time is 83.5 μsec. With GAIN set to 256 and no OFFSET, the maximum conversion time is 4.1 μsec.

4.3 OFFSET

The OFFSET is used to precisely shift the memory assignment of the ADC's conversions. With no OFFSET the ADC's channel numbers are the same as the memory's channel numbers.

For example, if the GAIN is set to 8192 and the memory assignment is only 4096, an OFFSET of zero will allow only the lower half of the full-scale conversions to be stored. That is, pulses up to five volts will be stored, pulses greater than five volts will not be stored.

If, in this example, the OFFSET were set to 4096, channel zero of the memory would be shifted to correspond to channel 4096 of the ADC. This offset would allow the upper half of the full-scale conversions, those above five volts, to be stored in the assigned memory.

4.4 LLD AND ULD

The Lower Level Discriminator (LLD) and the Upper Level Discriminator (ULD) controls set the limits for the input signals to be accepted by the ADC for conversion. If an input pulse falls within the selected window (higher than the LLD setting but lower than the ULD setting) the input will be converted. If the input does not fall within the window, the input will not be converted. The window check is made at the conclusion of the linear gate time; an input pulse not within the window will add to the ADC's dead time.

4.5 RANGE

The ADC RANGE is set by the Series 90's program to equal the size of the memory assigned to the ADC's Group.

Inputs which convert to a number greater than the allowed RANGE will not be stored in memory. Since the range check is made after the input has been converted, an overflow conversion will add to the ADC's dead time.

4.6 ZERO

The ZERO control varies the zero intercept of the ADC conversion function so that zero energy is stored in channel zero of the memory. The Model 8076 is shipped with the ZERO set for a GAIN of 8192. For other gains, a slight adjustment of the control may be necessary for precise energy calibration.

When the ADC is properly calibrated, the ADC zero reference voltage will normally be slightly negative. Some experiments may require the ADC to be uncalibrated using a positive value. On D revision ADCs, it may be necessary to raise the LLD to be equal to or more positive than the ADC zero to insure proper operation. This should not be a problem since signals below the ADC zero reference voltage are not processed, regardless of the LLD setting. The ADC zero reference voltage may be monitored at the front panel CAL test point. There are no restrictions for E revision and higher ADCs. The revision level is indicated by the letter following the identification number at the top of the printed circuit board.

For accurate setting of the ZERO control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. Connect the Pulser's SIGNAL OUT to the ADC INput.
2. Set the Pulser to HI, 0°, +, and 0.5 μsec Rise Time.
3. Set the ADC's GAIN control as desired.
4. Set all binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY on, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.
5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be set for the ADC. For instance, if the memory is 4096 channels and the GAIN is set for 8192, an OFFSET of 4096 must be added so that conversion can take place in the highest channel of the memory.
6. Turn all binary switches on the Model 8210 OFF, except the 1/64 switch, which should be left ON.
7. Set the OFFSET of the ADC to zero.
8. Adjust the ZERO control so that counts are being collected in the proper channel, as follows:

Gain	Channel
8192	128
4096	64
2048	32
1024	16
512	8
256	4

9. Repeat steps 4 through 8 until no further adjustments are necessary.
10. The voltage which can be seen at the CAL test point may be recorded and used in the future for quickly setting the ZERO control.

4.7 PEAK DETECT

In the AUTO mode, the linear gate, which allows a valid input pulse to be acquired, opens when the input rises above the input threshold. The input threshold level tracks the LLD setting up to 100 mV, maximum; therefore, the input signal's baseline must be less than 100 mV for proper ADC operation.

The linear gate closes when the input pulse falls below 90% of its peak amplitude. Wide input pulses may make the AUTOmatic detection of the 90% point less certain. To overcome this uncertainty, the DELAYED peak detect feature may be used. This feature allows input pulses up to 100 μsec wide to be converted. In this mode the linear gate

closes at the end of the selected delay time. The delay time can be selected with the ADJ control while monitoring the INSP test point next to the ADJ control.

In either peak detect mode, the INSP test point provides a positive logic pulse; the pulse width represents the linear gate time.

4.8 GATE

Input pulse conversions may be enabled or disabled by using the GATE function. This function is not the same as the linear gate, which is an internal circuit.

In the COINC mode, a positive logic pulse at least 250 nsec wide or a positive dc level must be present at the GATE connector during the linear gate time. The opening and closing of the linear gate can be seen at the peak detect INSP test point.

If the GATE input is low during the linear gate time, conversion will not take place.

An internal jumper (EARLY/LATE) is shipped in the LATE coincidence position, which means that the GATE pulse must be present sometime during the linear gate time to be effective. Since a common gating signal is the output of an independent SCA module, this late-arriving pulse can be accommodated by using the DELAYED peak detect mode and adjusting the linear gate time, as seen at the INSP test point, so that the linear gate closes after the SCA's output arrives. Thus the need for delaying the ADC INput signal can be eliminated.

If the jumper is changed to the EARLY coincidence position, the GATE signal must be present before the linear gate opens and remain for at least another 250 nsec.

EARLY coincidence is preferable when a high count rate is being gated because of the appreciable dead time introduced in the LATE coincidence mode. However, LATE coincidence gating is easier to do since a delay amplifier is not needed.

In the ANTI mode, the logic sense of the GATE signal is inverted. That is, a logic low will enable the linear gate and a logic high will disable it.

Note that in the ANTIcoincidence mode, the gating logic must be set for LATE coincidence for proper operation.

In any gating mode, an open GATE (nothing connected to the GATE connector) acts as if an enabling level were present.

4.9 SAMPLED VOLTAGE ANALYSIS

The ADC is usually used in the Pulse Height Analysis (PHA) mode, but by changing the PHA/SVA switch to the SVA position, analog voltages can be sampled by the ADC. The result will be an amplitude distribution curve of the input signal. The input signal must be between 20 mV and 10 V in amplitude to be sampled. If desired, an amplitude window may be set with the LLD and ULD controls.

The GATE input supplies the sampling signal, which must be equal to or greater than one microsecond in width. However, for pulse inputs (rather than dc levels or slowly changing ac signals), the GATE input signal must be narrower than the input pulse width.

The sampling rate should be at least twice the frequency of the input signal for accurate sampling.

4.10 REAR PANEL CONNECTORS

J101 CAB - Used to connect the ADC to the Analyzer.

J102 M/R - Used to connect the 8222A Mixer/Router to the ADC.

J103 STAB - Used to connect a Digital Stabilizer to the ADC.

J104 PUR - Accepts the REJect signal from, and provides the Linear Gate (LG) signal to, the Model 2020 amplifier.

J105 DEAD TIME - A dual-function connector which can be used as either an external dead time input from the Model 2020 amplifier or an internal dead time output. The mode is selected by an internal jumper (J9). Shipped in the NEGative INput mode.

Further information and signal specifications for J105, J102 and J104 can be found in Section 2 and for J101 and J103 in Appendix B.

Section 5.
ADC Theory of Operation

5.1 ADC BASEBOARD

5.1.1 Stretcher (Sheet 1 of the schematics)

The Stretcher is a discrete op-amp configured as a positive peak detector/holder including a calibrated precision ramp-down circuit. The peak holder has negative feedback via R28 and C9 providing a gain of +1. The Stretcher comprises transistors Q5 through Q7 and Q9 through Q23, and IC A55. Transistor array A55 is connected as a Darlington differential amplifier and allows a larger dynamic range at its input. Thus, the input signal is connected directly without attenuation, for improved signal-to-noise ratio characteristic. FET Q17 and transistor Q12 are connected to form a buffer providing low output and high input impedances. R21 and C7 form a low-pass filter limiting the input high-frequency noise and rise time. Diode D5 provides a negative input clamp. Q22 and Q23 are constant-current sources. Their bases are biased to approximately -16 volts and +16 volts respectively. R34 sets Q22's collector current to approximately 6 mA, while R13 sets Q23's collector current to approximately 3 mA allowing the differential stage to balance. RV10 can vary Q22's collector current by approximately ±2%, enabling the differential amplifier to be precisely balanced, establishing the Stretcher Output dc offset. The two current sources are slaved together providing good power supply rejection and thermal stability.

Pin 8 of the differential amplifier drives the base of Q18. When the differential amplifier receives a signal, more positive with respect to the peak holder output, A55 steers current, turning Q18 on. Q18 supplies current limited by R14 and charges capacitor C12 through Cascode Q16. The base of Q16 is biased by R17, R19 and R36 to approximately +10 volts. A55 and Q18, continues to source the precision current to C12. The resultant voltage generated on C12 is buffered to the Stretcher Output by FET follower Q17/Q12 and follows the positive transition of the input signal. When the input signal slope reduces to zero, or goes negative, A55 steers all current through pin 12. Q23 now pulls the base of Q18 positive, turning it off. R18 is included to ensure that Q16 also turns off when current from Q18 extinguishes. With the ramp and Q18 OFF, the voltage developed on C4 remains until the ramp-down cycle begins. R29 adds a zero to the peak holder transfer-function, ensuring stability. Signals present on C12 are voltage-translated slightly negative because of the output-buffer offset. The output buffer supplies a buffered signal to the differential-amplifier negative input (A55 Pin 9) via feedback resistor R25, zero-crossing comparator, and Stretcher/Input interrogation comparators. During the ramp-down cycle, the peak holder is gated OFF: that is, input signals can no longer influence C12. Q19 and Q20 are connected as a differential switch which normally biases the base of Q21, in conjunction with R8 and R10, to approximately +12 volts. Thus, Q21's base-emitter junction is reversed-biased outside Q18's voltage-control range, allowing the peak holder to operate normally. However, just prior to the ramp-down cycle, the STR OFF signal is set true, current through R7 is steered from Q20 to Q19. The base of Q21 is now increased to approximately +16.5 volts and reverse biases the base-emitter junction of Q18, disabling the Stretcher.

5.1.2 Ramp-Down Generator (Sheet 1)

The ramp-down generator is a gated precision-current source. A constant sink-current is developed and switched between ground (ramp off) and the peak holder storage cap (ramp on). The ramp-down circuit comprises Diodes D6, D7, transistors Q5 through Q7, Q9 through Q11, Q13 through Q15 and op-amp A54. D6 and D7 are 6.2 volt zener diodes, referenced to the -24 volt supply, producing a temperature stable reference-voltage source of -11.6 volts referenced to ground. This reference voltage is attenuated by R51, R53, RV9 and applied to the input of op-amp A54. Transistors Q5 and Q6 perform a voltage-to-current transformation. The op-amp input reference voltage (A54 pin 3) also appears at the emitter of Q5, establishing a constant voltage across the current set (conversion gain) resistors (R54 through R60) producing a precision current-flow. Since the transistors' combined current gains are high, the same current also flows through their collectors. R54 and R55 set the 8192 gain or ramp current. R56, R57, R58, R59 and R60 set the 4096, 2048, 1024, 512 and 256 conversion gain or ramp currents respectively. The ramp current is precisely calibrated using RV9. The precision ramp current is steered to ground or the peak-holder storage capacitor by current steering transistors Q13 and Q14. These transistors are connected as a differential switch. For the ramp down or track modes, the control logic sets $\overline{\text{RAMP ON}}$ to a logic "0". Thus the base of Q11 is biased more negative than that of Q10. Collectors Q11 and Q10 bias the base of Q14 more positive than that of Q13, setting Q14 ON, and Q13 OFF. The precision ramp current flows through Q14 and Q15, sinking current from the holding capacitor. Q15 is a Cascode with its base biased at approximately -5 volts by resistors R17, R19 and R36. This negative current flow continues for the duration of the $\overline{\text{RAMP ON}}$ Signal. Capacitor C12 is discharged with a high degree of linearity towards -24 volts. However at the zero crossing, the control logic sets RAMP ON to a logic "1" setting Q14 OFF and Q13 ON. The constant current is now steered to ground through Q13; current no longer flows from the storage capacitor.

For an invalid conversion, the Control Logic sets DUMP to a logic "1". Q7 and Q9 are both biased on, a current (significantly higher) determined by R46, independent of the precision current generator, now dominates, producing a much faster RAMP DOWN or DUMP cycle

Table 5.1
Read Registers

Register	Function	7	6	5	Bit 4	3	2	1	0
0	PHA } Module PHA-MR } Type	0 0	0 0	0 0	0 0	0 0	0 0	0 1	1 0
1	STATUS	All Trigger Enable	FIFO In Ready	FIFO Out Ready	—	—	PARA NOT VALID	WAIT	ACTIVE
2	RESERVED	—	—	—	—	—	—	—	—
3	RESERVED	—	—	—	—	—	—	—	—
4	INTERRUPT SOURCE	—	—	—	—	—	—	STOP INTR	START INTR
5		—	—	—	—	—	—	—	—
6*	INTERRUPTING UNIT	#7	#6	#5	#4	#3	#2	#1	#8
7	DMA PORT (DATA)	MSB							LSB
8-15	RESERVED	—	—	—	—	—	—	—	—

*The ALL code must be enabled to read register 6. ALL code is an RH in the Unit portion of the Address

Table 5.2
Write Registers

Register	Function	7	6	5	Bit 4	3	2	1	0
0	RESERVED	—	—	—	—	—	—	—	—
1	IMMEDIATE	—	—	—	CLEAR FIFO	CLEAR TIMER	STOP NEXT	STOP IMMED TICK	START
2	RESERVED	—	—	—	—	—	—	—	—
3	RESERVED	—	—	—	—	—	—	—	—
4	RESERVED	—	—	—	—	—	—	—	—
5	RESERVED	—	—	—	—	—	—	—	—
6	RESERVED	—	—	—	—	—	—	—	—
7	RESERVED	—	—	—	—	—	—	—	—
8	ULD Data	MSB							LSB
9	LLD Data (Byte 1)	MSB							LSB
A	LLD MSB Data	—	—	—	—	—	—	LLD BIT 10	LLD BIT 9
B	RANGE**	ATE	DEPEND	LIST	INTEN	—	R2	R1	R0
C	OFFSET	—	—	4096/	2048/	1024/	512/	256/	128
D	GAIN*	—	—	8192/	4096/	2048/	1024/	512/	256/
E	M/R CONTROL	EG4	EG3	EG2	EG1	IND/	INC/	INB/	INA/
F		—	—	—	—	—	—	—	—

*Only one bit active at any time.

**Range is selected as follows:

RANGE	R2	R1	R0
256	0	0	0
512	0	0	1
1024	0	1	0
2048	0	1	1
4096	1	0	0
8192	1	0	1

5.2.3 ADC Baseboard Interface

The Sequencer, Input Control, Header and ADC Address Latch and the FIFO and Latch, all found on the block diagram, can be grouped into the ADC Baseboard Interface Logic.

The sequencer is used to control the ADC Baseboard Interface logic. It is constantly monitoring the Data Ready (DATRDY) signal from the baseboard waiting for an indication that a conversion has been completed and the ADC requires servicing. When the DATRDY signal is true, the sequencer reads the address of conversion from the ADC baseboard in two bytes. The sequencer then checks for a conversion address of zero, which is invalid. If the conversion address is valid, the sequencer checks the output ready and input ready status of the FIFO. Output ready indicates that data is currently in the FIFO and a header byte is not required. If the FIFO is empty, a header byte must be loaded into the FIFO prior to the conversion address. This header is generated by the Input Control logic. Input Ready indicates that the FIFO is not full and can accept additional data. If the FIFO is full, then the sequencer must wait until data is transferred out of the FIFO leaving room for additional data. When all of the above conditions are true, the sequencer loads the two bytes of conversion data into the FIFO and releases the ADC.

The FIFO is 16 bytes deep and holds conversion data until the CAB controller can respond to the DMARQ and read the data from the FIFO.

5.2.4 Live Timer

The live time is generated by dividing down a 4.194304 MHz Oscillator to generate a time tick (TT) output from the live time logic at a 1-second period. This period assumes no dead time is generated by the ADC Baseboard. The Dead Time (DT) signal from the ADC Baseboard is used to disable the Live Time Counter. In this manner, Live Time counting is disabled whenever the ADC cannot accept a pulse, thereby correcting the Live Time with the Dead Time.

The output, TT, from the Live Timer is monitored by the sequencer and serviced in a manner similar to the servicing of the Data Ready from the ADC Baseboard. A unique header is generated for live time conversions and two bytes of zero data are loaded into the FIFO.

5.2.5 Mixer Router Interface

The Mixer Router control register contains the signals required to control the mixer router module. These control lines select the number of inputs and enable thse inputs. The Input Control logic on the Remote Interface Board recognizes that a Mixer Router is attached and uses six lines generated by the Mixer Router to tag the conversion address generated by the ADC baseboard with the proper routing bits. These routing bits direct the conversion into the memory group associated with the input that captured the pulse which has been converted by the ADC baseboard.

Appendix A
Installation

A.1 UNIT NUMBER SELECT SWITCH

Located at the top of the 8076 and accessible through the wrap is the Unit Number Select Switch. The setting of this switch determines the unit number of the particular 8076. The unit number can range from 1 to 8, therefore, positions 0 and 9 are invalid settings. Each 8076 connected to a 9132 Collect Interface must have a unique unit number.

A.2 CONNECTION TO THE CAB

The 8076 is connected to the CAB via the 34-pin ribbon cable entering the NIM area from the 9132 Collect Interface. Any connector except the last one can be plugged into J101 CAB on the rear panel of the 8076. Physical position and unit number do not necessarily have to correspond. Unused unit connectors are left for future expansion.

A.3 CAB TERMINATION BOARD

Supplied with the 9132 is the CAB Terminator Board. This board plugs onto the connector at the end of the CAB cable from the 9132. It must be installed to insure reliable operation of units tied to the CAB.

Appendix B
Connector Signals

B.1 J101 - CAB

Pin	Signal Name	Pin	Signal Name
1	DAT ADR 0/	18	GND
2	GND	19	INIT/
3	DAT ADR 1/	20	GND
4	GND	21	DMARQ/
5	DAT ADR 2/	22	GND
6	GND	23	INTRQ/
7	DAT ADR 3/	24	GND
8	GND	25	POLL/
9	DAT ADR 4/	26	GND
10	GND	27	RD/
11	DAT ADR 5/	28	GND
12	GND	29	WT/
13	DAT ADR 6/	30	GND
14	GND	31	ADRSTB/
15	DAT ADR 7/	32	GND
16	GND	33	+5 Volts
17	not used	34	GND

B.2 J102-8222A MIXER/ROUTER DATA AND CONTROL CONNECTOR

Pin	Direction	Signal	Description
1	IN	EG3	Enable 3rd of Group
2	Not Used		
3	OUT	$\overline{\text{HIMR}}$	Mixer/Router Installed
4	IN	$\overline{\text{CTM}}$	Clear Timer
5	OUT	$\overline{\text{RA}}$	Time Code Bit 0
6	OUT	$\overline{\text{INHADD1}}$(IA1)	Inhibit Add to Memory
7	IN	$\overline{\text{MRAK}}$	Mixer/Router Acknowledge
8	IN	$\overline{\text{TRMR}}$	ADC Release
9	OUT	RB	Time Code Bit 1
10	IN	EG1	Enable 1st of Group
11	IN	$\overline{\text{EG4}}$	Enable 4th of Group
12	OUT	$\overline{\text{MRTT}}$	Time Tick Ready
13	IN	EG2	Enable 2nd of Group
14	Not Used		
15	IN	$\overline{\text{IND}}$	Enable 16 inputs
16	OUT	$\overline{\text{DT}}$	Mixer/Router Busy
17	OUT	2^{N-2}	Routing Code Bit 0
18	Not Used		
19	OUT	$\overline{2^{N-1}}$	Routing Code Bit 1
20	IN	$\overline{\text{INB}}$	Enable 4 inputs
21	OUT	2^{N}	Routing Code Bit 2
22		GND	
23	OUT	$\overline{2^{M}}$	Routing Code Bit 3
24	IN	$\overline{\text{INC}}$	Enable 8 inputs
25	IN	$\overline{\text{INA}}$	Enable 2 inputs
26	Not used		

B.3 J103 - STABILIZER

Pin	Signal	Description
1	$\overline{SA2^0}$	
3	$\overline{SA2^1}$	
5	$\overline{SA2^2}$	
7	$\overline{SA2^3}$	
9	$\overline{SA2^4}$	
11	$\overline{SA2^5}$	Binary address data. Negative true logic; data is valid when STAB TRIG is true (low); TTL - LS outputs.
13	$\overline{SA2^6}$	
15	$\overline{SA2^7}$	
17	$\overline{SA2^8}$	
19	$\overline{SA2^9}$	
21	$\overline{SA2^{10}}$	
23	$\overline{SA2^{11}}$	
25	$\overline{SA2^{12}}$	
12	INT	Intensify; originates in the Digital Stabilizer and passed directly to the memory storage unit. This signal can be used to aid in determining the proper settings of the peak and window controls of the Stabilizer. Negative true logic.
14	STAB GAIN	Gain correction; an analog voltage from the Stabilizer. It is used to correct ADC Gain drifts. $Z_{IN} \approx$ 5k ohms; ± 5 V input yields a gain change of ≈ ± 5% of full scale.
16	STAB ZERO	Zero correction. an analog voltage from the Stabilizer. It is used to correct ADC Zero drifts. $Z_{IN} \approx$ 9.5k ohms; ± 5 V input yields a Zero change of ≈ ± 2% of full scale.
20	STAB TRIGGER	Stabilizer Trigger; Positive true logic pulse; provides stabilizer data sample window. About 1 μsec wide.
22	GND	Ground
26	- 12 V	Negative 12 V dc.
18	$\overline{\text{RST}}$	Reset Test; a logic low level resets the ADC.

B.4 J104 - PUR

Pin	Signal	Description
1	LG/	Linear Gate; provides a negative true logic signal; logic low when the ADC accepts an input. Initiated when the input signal exceeds the input reference threshold; returns to a logic high at the end of the ADC acquisition cycle. TTL output through a 47 ohm series resistor 4.7k ohm pull-up resistor to 5 V.
2	REJ	Reject. receives a positive true logic signal which is used to initiate an ADC reject sequence. It must occur during and remain active until the end of the ADC's LG signal. At this point the conversion attempt will be aborted. Amplitude 2.5 to 7 V width ≥ 50 nsec, loading ≤ + 800 mA at +3 V
3	GND	Ground

B.5 J105 - DEAD TIME

A rear panel LEMO dual-function connector: external dead time INPUT or ADC dead time OUTPUT. Either of these modes can be internally selected with a jumper plug (J9). Shipped in the INPUT mode.

INPUT - Accepts a negative true logic signal which is ORed with the ADC dead time. Logic low when true; amplitude ≤ 400 mV; 0 to +7 V maximum; loading < -1.4 mA at 400 mV.

OUTPUT - Provides a logic signal representing the ADC acquisition and conversion times; an internal jumper plug (J10) provides the option of POSitive true or NEGative true logic pulse signal; shipped in the POSitive true position. TTL compatible totem-pole output (LS) with a 4.7 kilohm pull-up resistor to 5 V.

Appendix C
The Canberra Acquisition Bus (CAB)

C.1 INTRODUCTION

This Appendix covers information on the devices which connect to the bus, the different states in which they operate, a description of the bus signals, and other information on interaction of the various system devices.

C.2 NOTATION

It may be appropriate at this point to define a consistent notation to be used throughout this appendix. The popular terms, one, zero, true, and false can be ambiguous. Hence the terms active high (asserted near +5 V) and active low (asserted at 0 V) are used in their place. The signal name without a slash (/) indicates the signal is active high, and the signal name with a slash (/) indicates the signal is active low.

C.2.1 CANBERRA ACQUISITION BUS SUPPORT

The Canberra Acquisition Bus supports two types of devices:

a.) Bus Master
b.) Acquisition Units (ACQs)

On this bus there is one and only one bus master and up to eight (8) acquisition units.

Bus Master

The bus master is the bus arbitrator. The master:

- resolves and grants bus priority
- monitors the bus status
- polls and handles bus interrupts
- controls the bus reset line
- provides power to the bus termination module
- controls all data transfers over the interfacing bus using the Read (RD/) and write (WT/) signals.

Acquisition Units (ACQs)

The ACQ has no bus control capability. It decodes the address lines and acts upon the command signals from the bus master. The ACQ drives the bus data lines only when requested to do so by the bus master.

C.3 CAB OPERATING STATES

There are three operating states used on the CAB: the reset state, the load state, and the active state.

a.) The reset state
The entire system enters this state immediately after power up or a system reset procedure. All previous data are lost and there is no communication between the bus master and the ACQs.

b.) The load state
This state is when the parameter information of the ACQ is initially loaded or changed. This state occurs just prior to the activation of an ACQ.

c.) The active state
This is the state when an acquisition unit is actively transferring data to the bus master (at the master's command). Any number of acquisition units can be active at a time.

C.4 CAB INTERFACING SIGNALS

The CAB interfacing signals are grouped into five groups based on their functions. The five groups and the number of signals in each group are:

C.4.1 ADDRESS/DATA LINES (AD0/- AD7/)

These eight bi-directional signal lines are used to carry address and data information between the bus master and the acquisition units connected to the Canberra Acquisition Bus.

C.4.2 CONTROL LINES

There are three control lines that are generated by the bus master:

a.) Address Strobe (ADRSTB/)
This control line is used to indicate whether the information on the address/data lines is address or data. When the address strobe (ADRSTB/) is active, it indicates that the information on the address/data lines is address. The ACQs decode the information on the address/data lines to determine which unit is being accessed by the master when ADRSTB/ is active low.

b.) Read Signal (RD/)
This is one of the two direction indicators of the data on the address/data lines with respect to the bus master. When RD/ is active, it indicates that the data on the address/data lines is being read by the bus master (data is coming from the addressed acquisition unit to the bus master).

c.) Write Signal (WT/)
This is the second direction indicator of the data on the address/data lines. When WT/ is active, the data on the address/data lines is being written by the master (data is coming from the bus master to the addressed acquisition units).

C.4.3 INTERRUPT SIGNALS

There are also three signals used in handling interrupts:

a.) Status Interrupt Request (INTRQ/)
This signal is OR-wired to all acquisition units. Any unit can generate an active low level on this signal at any time to report any change in status such as start of acquisition, task completion, unit failures etc. . . . This interrupt request signal is always monitored and the proper action will be provided by the bus master.

b.) DMA Interrupt Request (DMARQ/)
This signal is also OR-wired to all acquisition units. Any unit can generate an active low level on this signal to indicate that the unit is ready to transmit data to the bus master. This signal is always monitored and the bus master will provide the proper actions.

c.) DMA Poll Signal (POLL/)
The bus master generates this signal in responding to the DMARQ/ signal. The bus master uses this signal to command the requesting acquisition unit(s) to assert a low level on one of the eight address/data lines assigned to that particular unit determined by its unit number. The bus master then examines the address/data lines to determine all the requesting acquisition unit(s). The bus master then services the requesting unit(s) one by one on a priority basis until all original requests have been satisfied.

C.4.4 INITIALIZATION SIGNAL (INIT/)

This signal is generated by the bus master. It is used to reset all the bus devices to a known reset state. Signal INIT/ is an extension of the INIT/ generated on the system bus.

C.4.5 POWER AND GROUND

a.) +5 V
This signal is tapped directly out of the +5 V power source of the bus master. It is only used to power the termination module connected at the end of the Canberra Acquisition bus cable.

b.) Ground
This signal is used by the termination module and as a guard between the other CAB signals. It is tied to the CAB connector's even-numbered pins.

C.5 ADDRESS BYTE DESCRIPTION

The bus master accesses the ACQs by writing a specific byte of data onto the address/data lines. This byte is called the address byte. It contains the ACQ register address and a particular ACQ number.

a.) ACQ Registers
Bits 4-7 of the address byte are the unit register address bits. These four bits represents up to sixteen (16) registers contained in each acquisition unit.

b.) ACQ Number
The acquisition unit number occupies that the least four significant bits (bits 0-3). These bits represent sixteen codes. Codes 1-8 are individual ACQ numbers. Code 15 (1111 in binary) represents the code for "all" acquisition units. Each ACQ has a number from 0 to 7. The users can arbitrarily assign the unit number by setting a switch in the ACQ. The acquisition unit knows it is being accessed when it decodes its unit number from this bit field in the address byte. Multiple units cannot have the same unit number.

C.6 CAB CYCLES

The Canberra Acquisition Bus has three bus cycles used to transfer data between the bus master and the acquisition units.

a.) Address cycle
The bus master puts the address byte on the address/data lines containing the unit number and a register pointer. At the same time the address byte is on the address/data lines, the bus master activates the ADRSTB/. The address byte is kept stable long enough for all the units to decode it. The pulse duration of the ADRSTB/ controls how long the address byte is stable. The addressed units are now ready to accept data from the bus master. All other units will ignore any activities on the address/data lines until a new address byte is sent. The bus master can cause more than one unit to be active when it uses the "all" code (1111_2).

b.) Read cycle
During this cycle, the bus master reads the contents of the internal register determined in the register address bit field of the address byte from all of the

addressed ACQs. The bus master sends the read signal RD/ and the active ACQs immediately put the required data byte on the address/data lines.

c.) Write cycle
In this cycle the bus master writes data to the addressed ACQs. The bus master generates the write strobe (WT/) and a data byte on the address/data lines. The addressed units have to accept this data byte before WT/ ends.

C.7 CAB COMMUNICATION SEQUENCES

There are three communication sequences used on the CAB: the Initialization, DMA, and Interrupt sequences.

C.7.1 THE INITIALIZATION SEQUENCE

This sequence generally occurs prior to activating an ACQ. The bus master first uses the address byte to address the unit. The address byte has the unit number code on the four LSBs and the register address pointer of the register the bus master wants to load or change. The address byte is accompanied by the ADRSTB/. The ACQ decodes the address byte and awaits the transfer of a data byte from the master.

The bus master sends the register data on the address/data lines accompanied by the WT/ signal. The bus master continues to address other registers and write data until all required parameters are loaded. The bus master should then read register 1 to verify the "parameter valid" flag has been satisfied.

C.7.2 THE DMA SEQUENCE

The ACQs perform their functions after receiving their needed parameters and commands from the bus master. Any unit can then set DMARQ/ when it has data to transfer. This is the start of the DMA sequence. The bus master acknowledges the DMARQ/ by sending out the POLL/ signal. All requesting units pull down the address/data line assigned to that unit. The bus master then services the requesting units one at a time on a priority basis. It sends an address byte with the highest priority unit addressed and the DMA register (register 7). All other non-addressed ACQs pull away their DMARQ/.

The addressed unit will dump data bytes synchronous to the master's RD/ pulses until the complete block has been transferred. The ACQ, upon completion, terminates the DMA by pulling away its DMARQ/. The bus master then terminates RD/ pulses and addresses the next highest priority ACQ if more than one were originally pending and repeats the process until all units are serviced.

The bus master terminates the DMA sequence by sending the deselect address byte with the "deselect" code (1000_2) for the four LSBs and the register address 0 for the four MSBs. All units can make DMA requests again when they have more data. The bus master never does a write cycle in the DMA sequence. The CAB is specified only for DMA dumps to the bus master.

C.7.3 THE INTERRUPT SEQUENCE

The ACQs set the INTRQ/ any time they have a change in status. The bus master does not generate the POLL/ in this case. It addresses "all" units with a register 6 pointer. All requesting units pull the appropriate address/data lines assigned to the unit when a read cycle is performed. The bus master responds by sending the address byte with the address of the highest priority unit and the registers addresses 1, 4, or 5 depending on how the interrupt logic is handled in the unit. All inactive units pull away the INTRQ/ in exactly the same manner as in the DMA sequence. The remaining steps of this sequence are the same as in DMA sequence. However, the bus master is not restricted to just read cycles.

BASIC WARRANTY

Equipment manufactured by Canberra Industries, Inc. is warranteed against defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in the instruction manuals. During the warranty period, repairs or replacement will be made at Canberra's option on a return to factory basis. The transportation cost, including insurance to and from Canberra, is the responsibility of the Customer except for defects discovered within 30 days after receipt of equipment where shipping expense will be paid by Canberra to and from Canberra.

The customer must obtain an authorized customer service return number before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty.* In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment.

The Canberra Basic Warranty applies only to equipment manufactured by Canberra which is returned to the factory. If equipment must be repaired at the customer's site, the actual repair labor and parts will be provided at no charge during the warranty period. However, travel expenses to and from the customer's site, (travel time labor, and living expenses while on site), shall be paid by the customer unless an On-Site Warranty Option has been purchased. This option may only be purchased prior to shipment of the equipment to the customer.

The express warranties set forth herein are the only warranties with respect to the products, or any materials or components purchased from others and furnished by Canberra, and there are no other warranties, expressed or implied. The warranty of merchantibility is expressly limited as herein provided and all warranties of fitness are expressly disclaimed and excluded. Canberra shall have no liability for any special, indirect or consequential damages, whether from loss of production or otherwise, arising from any breach of warranty hereunder or defect or failure of any product or products sold hereunder.

EXCLUSIONS

Warranty service is contingent upon the proper use of all equipment and does not cover equipment which has been modified without Canberra's written approval or which has been subjected to unusual physical or electrical stress as determined by Canberra Service personnel. Canberra Industries shall be under no obligation to furnish warranty service (preventive or remedial): (1) if adjustment, repair or parts replacement is required because of accident, neglect, misuse, failure of electrical power, air conditioning, humidity control, transportation, or causes other than ordinary use; (2) if the equipment is maintained or repaired or if attempts to repair or service equipment are made by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by neutrons or heavy charged particles. Damage from these causes is readily identifiable as described in the manual accompanying each detector. Be windows are susceptible to mechanical damage and to corrosion from harsh or humid environments. Such damage is not covered by the warranty.

Although Canberra may frequently supply, as part of systems, equipment manufactured by other companies, the only warranty that shall apply to such non-Canberra equipment is that warranty offered by the original manufacturer, if any.

Canberra will, upon request, offer, as an option, warranty coverage for non-Canberra equipment such as computers and peripherals sold as part of a system supplied by Canberra. Quotations on this coverage may be obtained by contacting Canberra Customer Service or any of our sales staff.

SOFTWARE

Canberra warrants software media from defects discovered within 30 days after receipt.

Canberra assumes no responsibility for user-written programs or programs published as part of information exchange in Canberra periodicals.

Engineering assistance for software development is available and can be contracted through the Sales Department.

INSTALLATION

Installation of equipment purchased from Canberra shall be the sole responsibility of the customer unless the installation is specifically contracted for at the prevailing Canberra field service rates. To insure timely installation after receipt of equipment, it is recommended that installation be contracted for at the time the equipment is ordered.

ON-SITE WARRANTY OPTION

The On-Site Warranty Option provides for free on-site warranty work (Canberra pays all travel and living expenses) within the first 90 days after delivery of equipment to the customer. If installation is ordered from Canberra, the 90 day period commences upon completion of the initial installation. After the 90 day period, labor and materials used on site will still be covered by the basic warranty, but the customer shall pay for all travel expenses—travel time labor and living expenses incurred for any on-site service.

A maintenance contract may be purchased covering the period after the 90 days on-site warranty period, or after initial installation of the equipment. This is to be contracted through Canberra Customer Service.

REPAIRS

Any Canberra-manufactured instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. When returning instruments for repair, contact the Customer Service Department for shipping instructions and an Authorized Customer Service Return Number.

All correspondence concerning repairs should include the Model number and a description of the problem observed.

Once repaired, all equipment passes through our normal preshipment checkout procedure. Return shipping expense on out-of-warranty repairs will be charged to the customer.

For instruments out of warranty, the customer must supply a purchase order number for the repair before the item will be returned.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, immediately notify Canberra and the carrier making delivery, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in processing damage claims.

RETURN SHIPMENTS

Canberra Customer Service Department must be notified in advance if equipment is to be returned for any reason. Canberra can suggest the best means of shipping and will be able to expedite the shipment in case it is lost or delayed in transit.

The customer must obtain an authorized customer service return number before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty.* In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment. Care should be exercised in packing equipment for return. The customer is responsible for adequate packing to prevent damage in shipment. If the original shipping container is not available and the customer does not have the means to provide a suitable container, Canberra can provide a container for a fee.

Equipment should be returned to your area service center or to Canberra, Meriden. For shipment from outside the U.S., our shipping address is:

Canberra Industries, Inc.
c/o M.C.B. Customhouse Brokers, Inc.
Bradley International Airport
Air Cargo, Complex A
Windsor Locks, CT 06096 U.S.A.

SERVICE AND SERVICEABILITY

Canberra has gone to great lengths to insure that the instruments provided are functionally modular and therefore easy to service. In addition to modularity, Canberra has embarked on an extensive System Service Program to provide a totally responsive service capability. Complete Service Contracts with special arrangements for 24 hour response and weekend standby services are available from Canberra. For a detailed description of our Customer Service Program, please contact our Systems Service Department in Meriden, Connecticut, U.S.A.