PREAMP/AMPLIFIER
Models 7404-01/7404-01A
7404-01B/7404-01C/7404-01S

0387

Operator's Manual

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

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FIGURE LISTING

Section 1. Introduction

1.1 DESCRIPTION

There are several versions of the Model 7404-01. The characteristics of each are listed in the following table:

Model	Amplifier Shaping	Bias Voltage Range	Input Connector	Physical Application	Detector Application
7404-01	0.5 μsec	± 500 V	None	Direct Mount to 7404	SSB
7404-01A	0.5 μsec	± 500 V	BNC Male	Direct Mount to 7400 A	SSB
7404-01B	0.5 μsec	± 500 V	BNC Female	General Purpose	SSB
7404-01C	0.5 μsec	± 500 V	BNC Female	General Purpose	SSB
7404-01S	1.5 μsec	± 3000 V	SHV	General Purpose	Proportional Counter

All versions of the Model 7404-01 contain a charge-sensitive preamplifier and a linear shaping amplifier which provides signal conditioning required for counting or spectroscopy. The unit accepts either a positive or a negative charge output of Surface Barrier Detectors or Gas Proportional Counters and provides near-Gaussian-shaped unipolar output pulses.

The preamplifier is a low noise design with a diode-protected FET front end. It converts detector charge into a voltage step whose amplitude is proportional to the total charge collected in each event. The nominal charge gain is 200 mV/pC. The pulse decays with a nominal time constant of 470 μsec.

The amplifier section comprises two differentiators and two complex-pole integrators, followed by a polarity selector, a dc restorer, and a driver. The low pass filters maximize the signal-to-noise ratio, provide improved output pulse symmetry, and minimize detector rise time variation sensitivity. The baseline restorer compensates for the effects of baseline shift on the output signal as a result of amplifier interstage RC coupling networks. A test point (TP) is provided on the front panel which allows the output signal to be monitored.

The gain is continuously adjustable by means of a 22-turn screwdriver control on the front panel. The output OFFSET is also adjustable by means of a front panel 22-turn control and covers a range of ± 200 mV dc.

A TEST INPUT is provided on the rear panel to assist in system setup and to simplify trouble shooting. The nominal voltage gain from the TEST INPUT to the OUTPUT is dependent on the setting of the front panel GAIN control

Section 2. Specifications

2.1 INPUTS

DETECTOR INPUT accepts charge pulse from radiation detectors, such as Silicon Surface Barrier or Proportional Counter.

TEST INPUT is capacitively-coupled to preamp input; Z_{in} = 93 ohms.

HV INPUT accepts detector bias voltage; see Section 1.1 for voltage range.

2.2 OUTPUTS

OUTPUT provides positive linear near-Gaussian shaped unipolar pulses; amplitude linear to +10 V, +12 V max.; dc restored; output dc level adjustable for 0 ± 200 mV via front panel OFFSET control; $Z_{out} < 1$ ohm; short circuit protected.

2.3 PERFORMANCE

	7404-01, 01A, 01B, 01C	7404-01S
Operating Temp	0 - 50° C	0 - 50° C
Gain Range	17 - 40 V/pC	11 - 88 V/pC
Gain Drift	≤ ± 200 ppm/° C	≤ ± 200 ppm/° C
DC Drift	≤ ± 100 μV/° C	≤ ± 100 μV/° C
Integral Nonlinearity	≤ ± 0.4%	≤ ± 0.4%
Pulse Shaping	0.5 μsec Unipolar	1.5 μsec Unipolar
Noise Contribution	≤ 11.5 X10^{-17} Coulombs true rms referred to input at max. gain and 0 pF input capacitance.	≤ 9 X10^{-17} Coulombs true rms referred to input at max. gain and 0 pF input capacitance.

2.4 Connectors

	7404-01	7404-01A	7404-01B 7404-01C	7404-01S
Detector Input	.040 Pin	BNC (Male)	BNC	SHV
Bias Input	BNC; also Power Conn. (Pin 3)	Same	Same	SHV
Test Input	BNC; also Power Conn. (Pin 8)	Same	Same	BNC
Power	Amphenol 17-20090	Same	Same	Same
Output	BNC	BNC	BNC	BNC

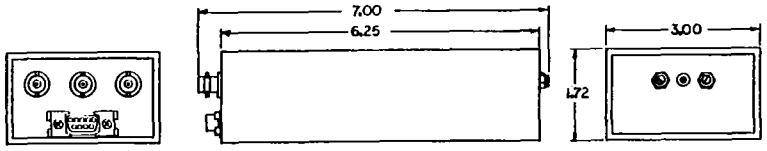
BNC is UG-1094/U unless otherwise noted.

2.5 POWER REQUIREMENTS

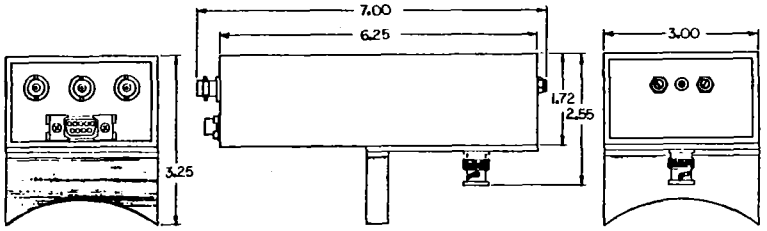
+24 V dc — 80 mA +12 V dc — 30 mA
-24 V dc — 30 mA -12 V dc — 39 mA

2.6 PHYSICAL

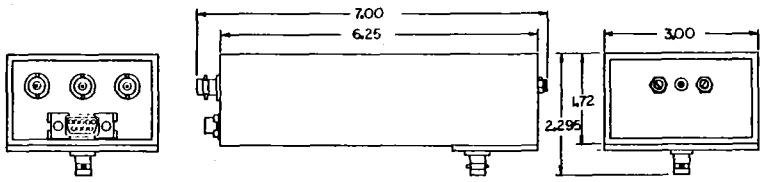
SIZE - See Figure 2.1 for outline details.
NET WEIGHT - 0.5 kg (1.1 lbs.)
SHIPPING WEIGHT - 0.55 kg (approx. 1.2 lbs.)



7404-01



7404-01A



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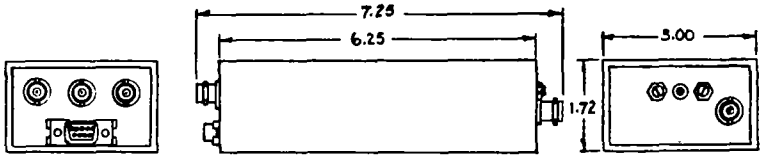
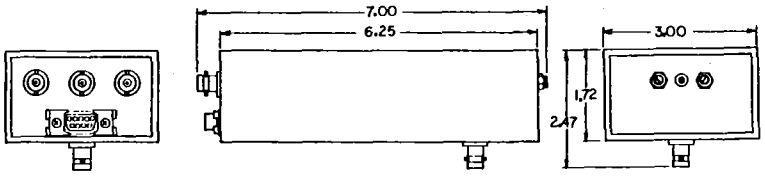


7404-01C



7404-01S

Figure 2.1
Outline Drawings

Section 3.
Controls and Connectors

3.1 FRONT PANEL

GAIN - 22-turn screwdriver adjustment provides the following gain ranges:

7404-01, 01A, 01B, 01C	17-40 V/pC
7404-01S	11-88 V/pC

OFFSET - 22-turn screwdriver adjustment provides ± 200 mV offset of output baseline.
TP - Allows observation of amplifier output (use a high-impedance probe).

3.2 REAR PANEL

HV INPUT - Accepts detector bias voltage.
TEST INPUT - Accepts test signal from a reference pulser, such as the Model 1407.
OUTPUT - Supplies amplifier output signal to a Mixer/Router or an ADC.
POWER CONNECTOR - Provides dc power to the amp/preamp. Can also accept test and HV inputs (see Section 5.1.2).

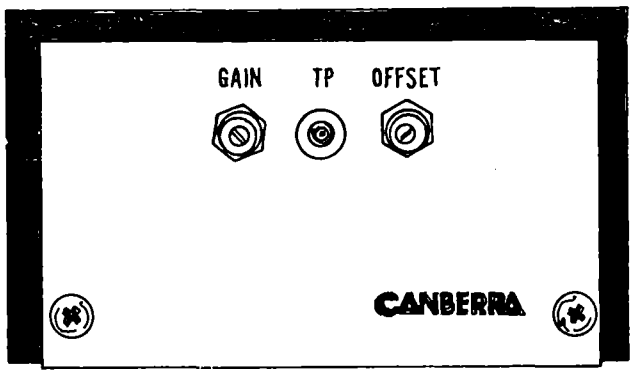


Figure 3.1
Front Panel

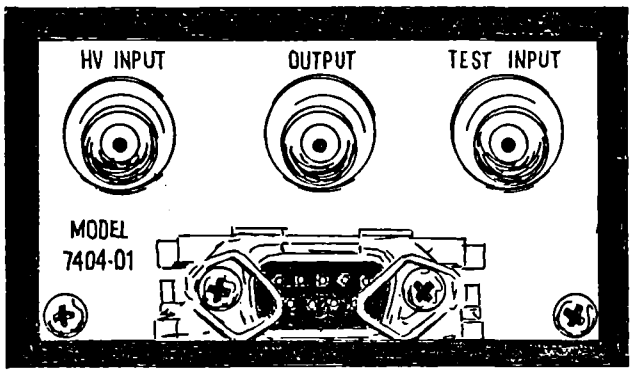


Figure 3.2
Rear Panel

3.3 INTERNAL CONTROLS

POLARITY - PC board mounted jumper provides inverting or noninverting operation. Factory set for inverting operation.
POLE-ZERO (RV-1) - PC board mounted potentiometer - factory set for proper compensation of first stage decay time constant.
TEST INPUT GAIN (RV-2) - PC board mounted potentiometer - factory set for energy calibration of 7404-01 when used with 7404.
PULSE RESPONSE (RV-3) - PC board mounted potentiometer - factory set for proper rise-time and stability.
DC RESTORER CURRENT (RV-4) - PC board mounted control - factory set for optimum restorer current.

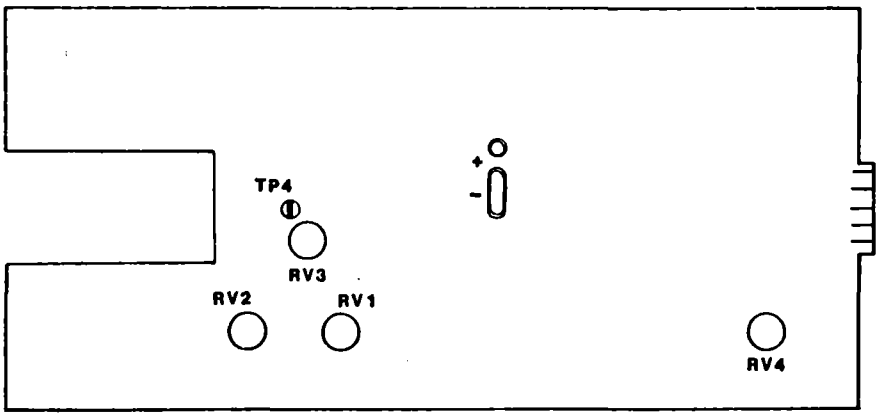


Figure 3.3
Internal Controls

Section 4. Installation

4.1 7404-01
Fastens to 7404 by means of two screws through the bottom front plate (accessible by removing cover) and by the front plate screws which must be removed and reinserted through the 7404 panel.

Input signal pin is inserted into BNC feedthrough of 7404. (Dress the wire so it does not touch other components.)

4.2 7404-01A
Attaches to 7400A by means of BNC connector. Rubber cradle conforms to 7400A body to support the unit horizontally.

4.3 7404-01B, 01C
Connects to detector or to electrical feedthrough by means of 93 ohm BNC cable. Remember than cable capacitance will increase noise from preamplifier, so keep the cable short.

4.4 7404-01S
Connects to detector by means of SHV cable.

Section 5. Operating Instructions

5.1 SETUP

5.1.1 Polarity Selection
All versions of the 7404-01 are factory set in the inverting mode. This means that the output will be positive for detectors requiring positive bias (Proportional Counters, Standard SSB Detectors, Diffused Junction Detectors, etc.). Some SSB detectors require negative bias. If used with this type of detector, change the internal polarity selecting jumper to (+) before applying power to the unit. Refer to figure 3.2.

5.1.2 Power Requirements
The 7404-01s require ±12 and ±24 V dc which is obtainable from the 7404 or from NIM BINs or various MCAs. The power input connector is wired according to the NIM Standard, but it makes use of additional pins for certain signals available from the 7404. Do not apply inappropriate power or signals to these pins*.

Power Connector	Function
Pin 1	Ground
Pin 2	Not used
*Pin 3	Bias Input
Pin 4	+12 V dc
Pin 5	Not used
Pin 6	-24 V dc
Pin 7	+24 V dc
*Pin 8	Test Input
Pin 9	-12 V dc

Bias Input and Test Input on the Power Connector can be used - but appropriate 93 ohm coaxial cable MUST be employed.

5.1.3 Connecting the Detector
The charge sensitive preamplifier produces noise as a function of capacitance loading the input. This load includes both cable and detector capacitance, so cable capacitance should be minimized for best results.

CAUTION

The input circuit has low impedance coupling to the sensitive input-FET, and it carries the H.V. Bias, so caution should be exercised to prevent arcing in the cable or connections to the detector. Such discharge or arcing can easily destroy the FET. The input signal must also be properly shielded (use coaxial cable) to prevent noise pickup.

5.2 OPERATION

5.2.1 Applying Bias
Because the input is ac coupled to the Bias network, the preamplifier will usually go into saturation during application, charge, or removal of detector bias. At such times, the output signal including output noise will disappear until the bias network is charged to the new operating bias.

For detectors which undergo depletion with application of bias (semiconductor types), the noise will diminish as bias is increased until depletion is reached or until increasing leakage-current noise overcomes the noise associated with decreasing detector capacitance. You can use this as a guide to application of bias on such detectors.

Typically, a faulty detector will exhibit high noise at less than recommended bias. For all of these observations an oscilloscope is required.

5.2.2 Adjusting Zero and Gain

The zero should be adjusted with a scope on the output to set the dc output to zero volts.

The gain adjustment is used (along with MCA conversion gain) to establish the energy range of the output signal.

If you want the MCA channel number to reflect energy in keV, you will need to adjust both gain and the ADC Baseline (zero) iteratively to (1) eliminate any offset in the system and (2) establish the desired overall system gain (1 keV/channel).

5.3 TROUBLESHOOTING

It is often difficult to distinguish detector problems from electronics problems. An oscilloscope, a voltmeter, and a precision pulser (such as the Canberra Model 1407) are necessary to perform most troubleshooting tasks. Listed below are some common problems that can be diagnosed using these tools.

Symptom	Check
A. No output without Bias Applied	1. Input Power 2. DC Level at TP-4 (if not 0-2 Volts FET may be faulty)
B. No output with Bias Applied	1. Check without detector connected (shield input) 2. DC Level at TP-4 vs. Bias Voltage. (If not constant decoupling capacitor may be faulty)
C. Noisy Output	1. Check noise vs. Bias with detector connected. (SSB detector noise should decrease with voltage) 2. Check noise vs. Bias without detector connected. (If not constant decoupling capacitor may be faulty)

Section 6. Theory of Operation

The Model 7404-01 Preamp-Amp incorporates a low-noise charge-sensitive preamplifier and a unipolar output shaping-amplifier.

The preamplifier consists of input FET Q3, differential amplifier Q1 and Q2, output follower FET Q4, and current sinks Q9 and Q10. This group of devices functions as an inverting feedback amplifier whose closed-loop gain is set by the charge-integrating capacitor C15. Bias stabilization is provided by the dc feedback path through R16. This component serves to discharge C15 following each charge integration, and sets the tail-pulse shape of the preamplifier at a nominal 470 μsec decay time constant. Diode D1 provides protection for Q3 from the transient voltages experienced from momentary breakdowns in the detector bias circuit due to accidental faults.

The test input includes a calibration adjustment potentiometer RV2 which can be set to allow a controlled voltage-pulse input to generate a shaped output signal that is calibrated to read out in MeV.

Following the preamplifier is a pole/zero-compensated differentiator (C6, R20). The now abbreviated tail pulse is amplified by a fixed gain non-inverting feedback amplifier formed by differential pair Q7 and Q8, driver Q5, and push-pull outputs Q6 and Q11. The preset gain of 30 raises the signal level to be compatible with the shaping process to follow.

Preliminary integration is provided by R26, L4, and C20 before the signal is fed to the split-load inverter Q12, which permits polarity selection by the internal jumper plug. Q13 buffers the signal before the second integration is realized in R32, L5, and C24. The filtered signal is then amplified again by A1, which incorporates the front-panel-mounted gain control in its feedback path. The signal is usually a positive-going pulse at this point, and D4 limits the excursion by clamping the output of A1 to enhance prompt overload recovery.

Capacitor C26 couples the positive pulse into Q15, a simple restorer, which stabilizes the dc reference level for the pulse. This provides a proper baseline from which the output may be quantized in an ADC or SCA.

Output amplifier A2 provides the final stage of gain and permits the introduction of a dc offset/zero adjust, controlled by a front panel potentiometer. D5 limits the positive excursion to prevent saturation in either A2 or output transistor Q14 and insures prompt overload recovery.

WARRANTY

This warranty covers Canberra hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Equipment manufactured by Canberra's Instruments Division, Detector Products Division, and Nuclear Systems Division is warranted against defects in materials and workmanship for one year from the date of shipment.

Canberra warrants proper operation of its software only when used with software and hardware supplied by Canberra and warrants software media to be free from defects for 90 days from the date of shipment.

If defects are discovered within 30 days of the time you receive your order, Canberra will pay transportation costs both ways. After the first 30 days, you will have to pay the transportation costs.

This is the only warranty provided by Canberra; there are no other warranties, expressed or implied. All warranties of merchantability and fitness for an intended purpose are excluded. Canberra shall have no liability for any special, indirect or consequential damages caused by failure of any equipment manufactured by Canberra.

EXCLUSIONS

This warranty does not cover equipment which has been modified without Canberra's written permission or which has been subjected to unusual physical or electrical stress as determined by Canberra's Service Personnel.

Canberra is under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by abuse, neutrons, or heavy charged particles.

SHIPPING DAMAGE

Examine shipments carefully when you receive them for evidence of damage caused in transit. If damage is found, notify Canberra and the carrier immediately. Keep all packages, materials and documents, including your freight bill, invoice and packing list. Although Canberra is not responsible for damage sustained in transit, we will be glad to help you in processing your claim.

OUT OF WARRANTY REPAIRS

Any Canberra equipment which is no longer covered by warranty may be returned to Canberra freight prepaid for repair. After the equipment is repaired, it will pass through our normal pre-shipment checkout procedure.

RETURNING EQUIPMENT

Before returning equipment for repair you must contact your Regional Service Center or one of our factories for instructions. For detector repair, contact the Canberra Detector Division in our Meriden, Connecticut, factory for instructions. If you are going to return the equipment to the factory, you must call first to get an Authorized Return Number (ARN).

When you call us, we will be glad to suggest the best way for you to ship the equipment and will expedite the shipment in case it is delayed or lost in transit. Giving you shipping advice does not make us responsible for the equipment while it is in transit.

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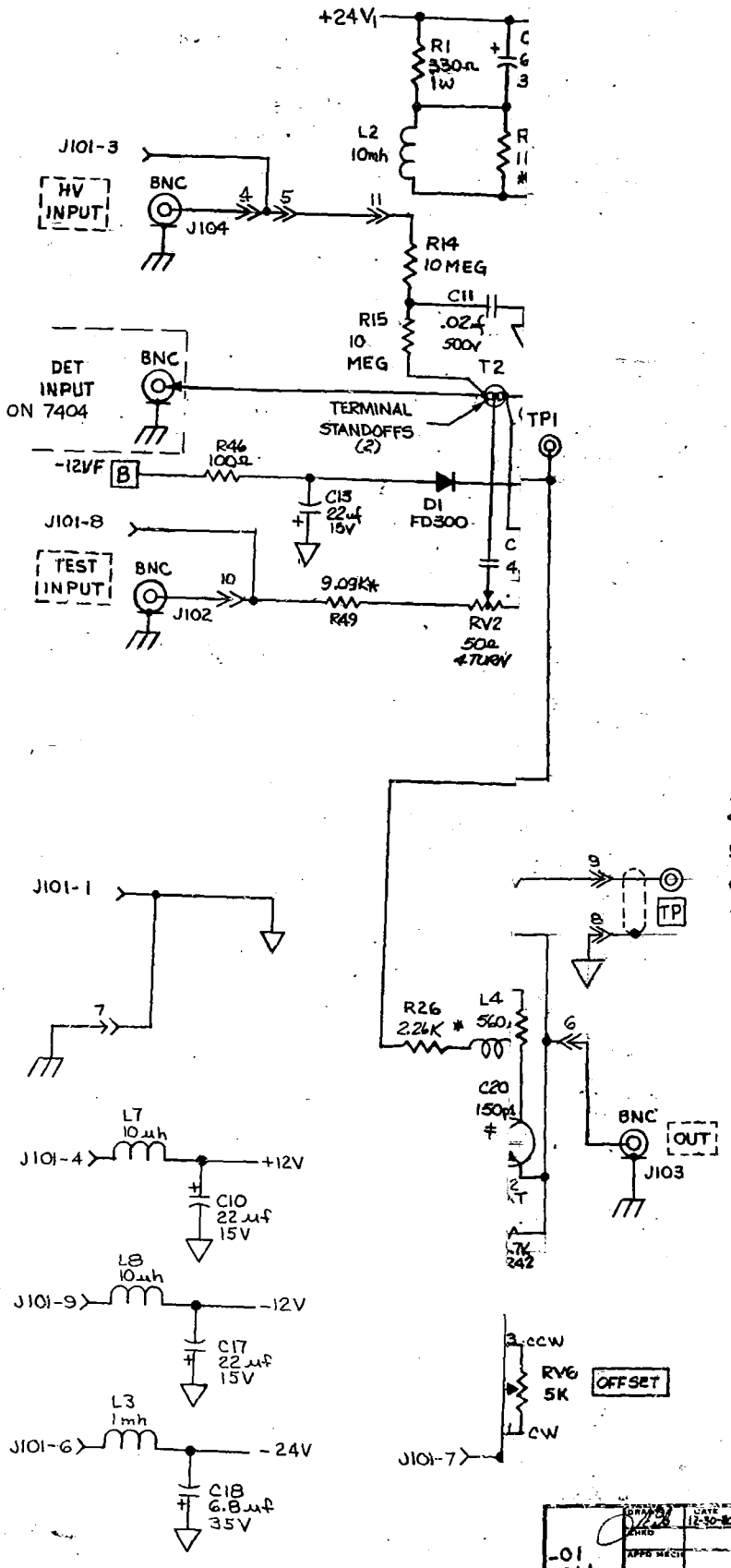
REV	CHANGE	ECN	BY	DATE	APVD
A	REVISED & REDESIGNED		RMC	6-5-81	
B	REVISED		HC	7-22-81	
C	REVISED		HC	9-29-81	
D	REVISED		HC	11-12-81	
E	REVISED		HT	12-4-81	
F	REVISED & RELEASED	3023	SAS	12-30-82	
G	REV R1	3422	ZP	4-83	
H	REV R15 AR12133	3773	ZP	4-30-84	
J	REV R19 & R37 AR14105	5386	AC	6-1-89	
K	AR15115, AR15237	8388	WP	9-29-92	



NOTES:

1. UNLESS NOTED ALL RESISTORS ARE 1/4 W ±5%
2. * INDICATES RN55C RESISTORS.
3. ≠ INDICATES MONO COG CAPACITOR.
4. Ø INDICATES POLYCARB CAPACITOR.
5. [ ] INDICATES REAR PANEL CONNECTION.
6. [ ] INDICATES FRONT PANEL CONNECTION.
7. [A] INDICATES SAME SHT. CONNECTION. REFERENCE LETTER.
8. ■ INDICATES NPO TCZ CAPACITOR.

LAST COMP. REF. NO:	
RESISTORS	R50
CAPACITORS	C32
TRANSISTORS	Q15
VAR. RES.	RV6
I.C.'S	A2
DIODES	D5
CHOKES	L8
TEST POINT	TP4

-01
-01A
-01B
-01C

SCHEMATIC
PREAMP/AMP
MODEL 7404-01

CANBERRA

NEXT ASSY A-18430

DO NOT TEMPLATE DRAWING

DRAWING NO. B-18427 REV. K

REV	CHANGE	ECN	BY	DATE	APP'D
A	REVISED & REDESIGNED		AMC	6-80	
B	REVISED		HC	7-22-81	
C	REVISED		HC	8-28-81	
D	REVISED		HC	11-12-81	
E	REVISED		HT	12-4-81	
F	REVISED & RELEASED	3023	SAS	12-20-82	
G	REV R1	3422	ZP	4-85	
H	REV R15 AR12133	3773	ZP	4-30-87	
J	REV R19 & R37 AR14105	3980	AC	6-1-89	
K	AR15115, AR15237	4389	MP	9-29-92	

NOTES:

1. UNLESS NOTED ALL RESISTORS ARE 1/4 W ±5%
2. * INDICATES RN55C RESISTORS.
3. ≠ INDICATES MONO COG CAPACITOR.
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5. [ ] INDICATES REAR PANEL CONNECTION.
6. ▭ INDICATES FRONT PANEL CONNECTION.
7. [A] INDICATES SAME SHT. CONNECTION. A = REFERENCE LETTER.
8. ■ INDICATES NPO TCZ CAPACITOR.

LAST COMP. REF. NO:

RESISTORS	R50
CAPACITORS	C32
TRANSISTORS	Q15
VAR. RES.	RV6
I.C.'S	A2
DIODES	D5
CHOKES	L8
TEST POINT	TP4

-01	DRAWN	12-30-80	SCHEMATIC PREAMP/AMP MODEL 7404-01
-01A	APPD MECH		
-01B	APPD ELEC	12-26-81	
-01C	NEXT ASSY	A-18430	
USED ON	SCALE	DO NOT TRANSLATE DRAWING	DRAWING NO. B-18427 REV. K SHT 1 OF 1

CANBERRA