TIME ANALYZER
Model 2143

0786

Operator's Manual

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

Table of Contents

Section 1. Introduction

The Canberra Model 2143 Time Analyzer generates a rectangular output pulse whose peak amplitude is linearly proportional to the time interval between a START and a subsequent STOP input. There are built-in features such as the Time Single Channel Analyzer, COINCidence/ANTICOINCidence gating, output STROBE, RESET, and STOP INHIBIT which enhance the utility and flexibility of this module for the spectrum of nuclear timing analysis needs.

The basic time-to-amplitude conversion (TAC) is used to analyze correlations between random nuclear events that occur within a selected interval of time, for time of flight, positron lifetime, pulse shape analysis in particle studies, and for pulse pair timing in position-sensitive detector systems. The Model 2143 offers 15 time ranges from 20 nanoseconds to 1 millisecond to span these needs. The positive unipolar TAC output is essentially flattopped for accurate measurement by a multichannel analyzer ADC.

Internal gating prevents a TAC output pulse for (1) overrange START to STOP time differences; (2) STOP inputs received prior to an accepted START; and (3) START or STOP signals received during the converter busy time. The front panel of OVERRANGE and VALID CONVERSION LEDs simplify setup of the instrument.

The COINCidence/ANTICOINCidence gating feature permits prompt (early) gating of a START/STOP pulse pair and is best used to minimize conversion time on unwanted pulses. The input must be received at least 10 nsec prior to and overlap the START input.

The single channel analyzer (SCA) portion of the Model 2143 operates on the TAC output pulse amplitude, and places equivalent timing restriction on the time spectrum being accumulated. For a selected TIME RANGE, a 0 to 100% "time window" can be selected with the front panel TIME and Δ TIME ten-turn locking-dial potentiometers. An SCA logic output is produced for every TAC pulse whose peak amplitude is greater than the TIME dial setting, but less than the sum of TIME + Δ TIME settings. A front panel SCA IN/OUT switch permits the user to gate the TAC output with the SCA directly, or to let the output be generated normally.

Both the TAC and SCA outputs are simultaneously adjustable in width (internal jumper plug for 0.5, 1.0, or 2.5 μsec) and the 2 outputs are synchronous, so timing jitter on the SCA output is essentially non-existent.

The TAC output is provided on the front panel with output impedance internally selectable for 10 ohms or 93 ohms. The output is direct coupled and essentially pedestal free.

Delay and strobe features have been provided, maximizing flexibility in fast timing systems with one or more slow side channels.

The front panel DELAY feature allows selection of the delay between the receipt of a STOP signal and the generation of an output signal.

Following a valid conversion, the strobe function allows an external control signal to determine if and when a TAC output is generated. The start and duration, or time window, in which a strobe signal will be accepted is controlled by the DELAY and CONV READY signals respectively. In the EXT Strobe Mode, the DELAY and CONV READY signals allow minimization of system dead time. In the INT Strobe Mode, the TAC output is generated immediately following the DELAY interval.

VALID START and VALID STOP auxiliary logic outputs are provided. The VALID START output duration is the time interval between an accepted START input, and the end of TAC reset time, and thus represents the full conversion busy time. The VALID STOP output duration is the time interval between an accepted STOP input, and the end of TAC reset time. Converter reset occurs after generation of a TAC output, upon receipt of a RESET/INHIBIT input, or upon detection of an overrange condition (no STOP input received within the selected time range). Reset time is a fixed 1 μsec on the X1, X10 and X100 MULTIPLIER ranges and is 10 μsec on the X1K and X10K ranges.

The front panel STOP INHIBIT adjustment allows rejection of STOP input signals in a range of 1% to 100% of each time range. This is useful for suppressing unwanted inputs in applications such as linear accelerators, and prevents false outputs. A MONITOR output is provided; when the output is true, STOP pulses are inhibited.

The RESET/INHIBIT input permits late anticoincidence gating. It is used to terminate a conversion cycle and prevent subsequent conversions while driven. This mode prevents a TAC output for slow energy analysis restrictions, for example.

The VALID START, VALID STOP, SCA, CONV READY, and MONITOR outputs are each available by internal selection as positive voltage pulses or negative fast NIM current pulses. The voltage outputs are also adjustable in peak amplitude for compatibility with interfacing instruments. Each positive output is source matched with a 50 ohm series resistive termination to prevent ringing due to reflections on unterminated cables, and the resulting multiple counting frequently experienced. The instrument is shipped with socketed resistors for each output which limit them to +5 V nominal (open circuit) for direct interface to common TTL circuitry. The user may remove the resistors as desired to obtain a +8 V nominal open circuit voltage for instruments requiring the NIM pulse level, or +4 V nominal into the 50 ohm load termination which some other instruments provide. This flexibility allows the user to adapt the output signal to his needs without risking the problems encountered with improperly driven cable and critical timing pulses.

Section 2. Specifications

2.1 INPUTS

START - Accepts negative or positive logic signals or levels as determined by internal jumper plug; shipped in negative position. Negative amplitude $\geq$ -250 mV. Positive amplitude $\geq$ 1 V. Width $\geq$ 2 nsec at above levels. $Z_{in} \approx 50$ ohm. Z_{in} selectable to $\approx$ 1 kilohm for positive input only by removal of internal resistor, input dc coupled. Leading edge initiates time conversion, front panel BNC connector. Inputs protected to $\pm$ 10 V.

STOP - Input specifications identical to START input. Leading edge terminates time conversion.

GATE - Input specifications identical to STRT input. Provides means of gating TAC output in either COINCidence or ANTICOINCidence mode. GATE must begin 10 nsec prior to and overlap START input.

STROBE - Accepts either a positive logic signal or dc level with amplitude 3 to 6 V, or a negative logic signal or dc level with amplitude -0.25 to -1.5 V, width $\geq$ 50 nsec, $Z_{in} \approx$ 1 kilohm for positve signals (selectable internally to 50 ohms), and 50 ohms for negative signals, dc coupled; initiates output pulse when in EXT strobe mode. Strobe must occur in time window set by CONV READY.

RESET/INHIB - Input specifications identical to strobe input; serves as a late anticoincidence input and terminates conversion cycle. The reset period ends at the conclusion of RESET/INHIB or the internal clear time, whichever occurs last.

2.2 OUTPUTS

TAC - Provides a positive flattopped rectangular unipolar pulse; constant pulse shape independent of TIME RANGE or amplitude; amplitude proportional to accepted START/STOP input pulse time difference; adjustable delay (0.5 to 10.5 μsec) and width (0.5, 1.0 or 2.5 μsec); rise time $\approx$ 250 nsec; dc coupled; front panel BNC connector $Z_{out} \approx$ 10 ohms or 93 ohms internally selectable. Shipped for 10 ohms and 1 μsec width.

VALID START (converter busy time) - Provides internally selectable positive voltage pulse of 5 or 8 V, with rise and fall times of $<$ 25 nsec, or negative current pulse of -16 mA with rise time of $<$ 10 nsec; shipped in negative position; $Z_{out} \approx$ 50 ohms, dc coupled; duration equal to time interval between accepted START input and end of cycle reset time; front panel BNC connector.

VALID STOP - Output pulse specifications identical to VALID START; duration equal to time interval between accepted STOP input signal and end of cycle reset time; front panel BNC connector. A VALID STOP does not necessarily indicate a VALID CONVERSION.

SCA - Output pulse specifications identical to VALID START; leading edge in time coincidence with and duration equal to TAC output; front panel BNC connector.

2.3 PERFORMANCE

TIME RESOLUTION - $<$ 0.01% of full scale plus 5 psec FWHM for all ranges. Time resolution is insensitive to count rate or START/STOP ratio.

TAC INTEGRAL NONLINEARITY - $<\pm$ 0.1% from 5 nsec to full scale on X1 MULTIPLIER range; $<\pm$ 0.1% from 1% to 100% of full range for all higher ranges.

TAC DIFFERENTIAL NONLINEARITY - $<\pm$ 2% from 15 nsec to full scale on X1 MULTIPLIER range; $<\pm$ 2% from 1% to 100% of full range for all higher ranges.

SCA TIME/Δ TIME INTEGRAL NONLINEARITY - $<\pm$ 0.5% of full scale.

TAC OUTPUT TEMPERATURE STABILITY - Better than $\pm$ 0.01%/°C ($\pm$ 100 ppm/°C) of full scale.

SCA TIME/Δ TIME TEMPERATURE STABILITY - Better than $\pm$ 0.01%/°C ($\pm$ 100 ppm/°C) of full scale.

OUTPUT DELAY/OUTPUT WIDTH TEMPERATURE STABILITY - Better than $\pm$ 0.01%/°C ($\pm$ 100 ppm/°C) of full scale.

TEMPERATURE OPERATING RANGE - 0 to 50°C.

TAC OUTPUT DROOP - $<$ 0.015%/μsec of delay from completed conversion to TAC output. Delay time is determined by front panel DELAY setting or external strobe acceptance, or both.

INTERNAL CLEAR TIME - Fixed 1 μsec recovery time on X1, X10 and X100 MULTIPLIER ranges, and 10 μsec on X1K and X10K MULTIPLIER ranges; occurs after each normal output and each overrange.

GATE PEDESTAL - Essentially zero pedestal, factory calibrated.

SCA OUTPUT TIME WALK - None, with respect to TAC output.

MINIMUM START TO STOP CONVERSION TIME - $\approx$ 2 nsec.

COUNT RATE CAPABILITY - START, STOP, GATE inputs capable of count rates greater than 25 MHz.

2.4 CONNECTORS

All signal connectors are located on the front panel and are BNC type.

2.5 POWER REQUIREMENTS

+24 V dc — 50 mA	+12 V dc — 250 mA
-24 V dc — 50 mA	-12 V dc — 250 mA

2.6 PHYSICAL

SIZE - Standard double-width NIM module 6.86 $\times$ 22.12 cm (2.70 $\times$ 8.71 inches) per TID-20893 (rev.)

NET WEIGHT - 1.3 kg (2.8 lbs.)

SHIPPING WEIGHT - 2.3 kg (5.0 lbs.)

Data sheet included in lieu of section 3 which appears to be missing information within section 3 can be found in the data sheet

Model 2143 Time Analyzer

Features

- 15 ranges of time-to-amplitude conversion, 20 nsec to 1 msec
- Time resolution < 0.01% + 5 psec FWHM on any range
- DC coupled for optimum count rate
- Built-in single channel analyzer and linear gate
- COINCidence/ANTICOINCidence gating inputs
- Selectable output delay and width
- Adjustable STROBE function
- All functions on front panel

Description

The Canberra Model 2143 Time Analyzer generates a rectangular output pulse whose peak amplitude is linearly proportional to the time interval between a START and a subsequent STOP input. There are built-in features such as the Time Single Channel Analyzer, COINCidence/ANTICOINCidence gating, output STROBE, RESET, and STOP INHIBIT which enhance the utility and flexibility of this module for the spectrum of nuclear timing analysis needs.

The basic time-to-amplitude conversion (TAC) is used to analyze correlations between random nuclear events that occur within a selected interval of time, for time of flight, positron lifetime, pulse shape analysis in particle studies, and for pulse pair timing in position sensitive detector systems. The Model 2143 offers 15 time ranges from 20 nanoseconds to 1 millisecond to span these needs. The positive unipolar TAC output is essentially flattopped for accurate measurement by a multichannel analyzer ADC.

Internal gating prevents a TAC output pulse for (1) overrange START to STOP time differences; (2) STOP inputs received prior to an accepted START; and (3) START or STOP signals received during the converter busy time. The front panel OVERRANGE and VALID CONVERSION LEDs simplify setup of the instrument.

The COINCidence/ANTICOINCidence gating feature permits prompt (early) gating of a START/STOP pulse pair and is best used to minimize conversion time on unwanted pulses. The input must be received at least 10 nsec prior to and overlap the START input.

The single channel analyzer (SCA) portion of the Model 2143 operates on the TAC output pulse amplitude, and places equivalent timing restriction on the time spectrum being accumulated. For a selected TIME RANGE, a 0 to 100% "time window" can be selected with the front panel TIME and Δ TIME ten-turn locking-dial potentiometers. An SCA logic output is produced for every TAC pulse whose peak amplitude is greater than the TIME dial setting, but less than the sum of TIME + Δ TIME settings. A front panel SCA IN/OUT switch permits the user to gate the TAC output with the SCA directly, or to let the output be generated normally.

Both the TAC and SCA outputs are simultaneously adjustable in width (internal jumper plug for 0.5, 1.0, or 2.5 μsec) and the 2 outputs are synchronous, so timing jitter on the SCA output is essentially non-existent.

The TAC output is provided on the front panel. Output impedance is internally selectable for 10 ohms or 93 ohms. The output is direct coupled and essentially pedestal free.

Delay and strobe features have been provided maximizing flexibility in fast timing systems with one or more slow side channels.

The front panel DELAY feature allows selection of the delay between the receipt of a STOP signal and the generation of an output signal.

Following a valid conversion, the strobe function allows an external control signal to determine if and when a TAC output is generated. The start and duration, or time window, in which a strobe signal will be accepted is controlled by the DELAY and CONV READY signals respectively. In the ext Strobe Mode, the DELAY and CONV READY signals allow minimization of system dead time.

VALID START and VALID STOP auxiliary logic outputs are provided. The VALID START output duration is the time interval between an accepted START input, and the end of TAC reset time, and thus represents the full conversion busy time. The VALID STOP output duration is the time interval between an accepted STOP input, and the end of TAC reset time. Converter reset occurs after generation of a TAC output, upon receipt of a RESET/INHIBIT input, or detection of an overrange condition (no STOP input received within the selected time range). Reset time is a fixed 1 μsec on the X1, X10 and X100 MULTIPLIER ranges and 10 μsec maximum on the X1K and X10K ranges.

Description (Cont'd.)

The front panel STOP INHIBIT adjustment allows rejection of STOP input signals in a range of 1% to 100% of each time range. This is useful for suppressing unwanted inputs in applications such as linear accelerators, and prevents false outputs. A MONITOR output is provided; when the output is true, STOP pulses are inhibited.

The RESET/INHIBIT input permits late anticoincidence gating. It is used to terminate a conversion cycle and prevent subsequent conversions while driven. This mode prevents a TAC output for slow energy analysis restrictions, for example.

The VALID START, VALID STOP, SCA, CONV READY, and MONITOR outputs are each available by internal selection as positive voltage pulses or negative fast NIM current pulses. The voltage outputs are also adjustable in peak amplitude for compatibility with interfacing instruments. Each positive output is source matched with a 50 ohm series resistive termination to prevent ringing due to reflections on unterminated cables, and the resulting multiple counting frequently experienced. The instrument is shipped with socketed resistors for each output which limit them to +5 V nominal (open circuit) for direct interface to common TTL circuitry. The user may remove the resistors as desired to obtain a +8 V nominal open circuit voltage for instruments requiring the NIM pulse level, or +4 V nominal into the 50 ohm load termination which some other instruments provide. This flexibility allows the user to adapt the output signal to his needs without risking the problems encountered with improperly driven cables and critical timing pulses.

Specifications

INPUTS

START - Accepts negative or positive logic signals or levels as determined by internal jumper plug; shipped in negative position. Negative amplitude ≥ −250 mV. Positive amplitude ≥ 1 V. Width ≥ 2 nsec at above levels. $Z_{in} \approx 50$ ohm. Z_{in} selectable to ≈ 1 kilohm for positive input only by removal of internal resistor; input dc coupled. Leading edge initiates time conversion; front panel BNC connector. Inputs protected to ± 10 V.

STOP - Input specifications identical to START input. Leading edge terminates time conversion.

GATE - Input specifications identical to START input. Provides means of gating TAC output in either COINCidence or ANTICOINCidence. GATE must begin 10 nsec prior to and overlap START input.

STROBE - Accepts either a positive logic signal or dc level with amplitude 3 to 6 V, or a negative logic signal or dc level with amplitude −0.25 to −1.5 V; width ≥ 50 nsec; $Z_{in} \approx 1$ k ohm for positive signals (selectable internally to 50 ohms), and 50 ohms for negative signals, dc coupled; initiates output pulse when in EXT strobe mode. Strobe must occur in time window set by CONV READY.

RESET/INHIB - Input specifications identical to strobe input; serves as a late anticoincidence input and terminates conversion cycle. The reset period ends at the conclusion of RESET/INHIB or the internal clear time, whichever occurs last.

OUTPUTS

TAC - Provides positive flattopped rectangular unipolar pulse; constant pulse shape independent of TIME RANGE or amplitude; amplitude proportional to accepted START/STOP input pulse time difference; adjustable delay (0.5 to 10.5 μsec) and width (0.5, 1.0 or 2.5 μsec); rise time ≈ 250 nsec; dc coupled; front panel BNC connector. Z out ≈ 10 ohms or 93 ohms internally selectable. Shipped for 10 ohms and 1 μsec width.

VALID START (converter busy time) - Provides internally selectable positive voltage pulse of 5 or 8 V, with rise and fall times of < 25 nsec, or negative current pulse of −16 mA with rise time of < 6 nsec; shipped in negative position; $Z_{out} \approx 50$ ohms, dc coupled; duration equal to time interval between accepted START input and end of cycle reset time; front panel BNC connector.

VALID STOP - Output pulse specifications identical to VALID START; duration equal to time interval between accepted STOP input signal and end of cycle reset time; front panel BNC connector.

SCA - Output pulse specifications identical to VALID START; leading edge in time coincidence with, and duration equal to, TAC output; front panel BNC connector.

STOP INHIBIT MONITOR - Output pulse specifications identical to VALID START; provides observation of front panel STOP INHIBIT RANGE adjustment; front panel BNC connector.

CONVersion READY - Output pulse specification identical to VALID START. Active from end of DELAY period. Duration determined by front panel potentiometer. Range determined by internal jumper - 1 to 20 μsec or 10 to 200 μsec; shipped in 1-20 μsec position. Indicates period when STROBE input will initiate output pulse.

FRONT PANEL CONTROLS

TIME RANGE - Three-position rotary switch to select full scale time interval of 20, 50, or 100 nsec between accepted START and STOP input pulses.

MULTIPLIER - Five position rotary switch to extend TIME RANGE by X1, X10, X100, X1K or X10K.

DELAY - 22 turn screwdriver potentiometer to vary TAC output delay time; 0.5 to 10.5 μsec range, with adjacent toggle switch in VARiable; fixed 150 nsec relative to STOP input with switch in MINimum. A test point is provided to monitor the DELAY time setting.

GATE MODE - Toggle switch to select COINCidence or ANTICOINCidence gated mode of operation. Time conversion is enabled (COINC) or inhibited (ANTICOINC) upon receipt of a GATE input signal.

TIME - 10-turn locking dial potentiometer to select minimum time of interest from 0 to 100% of selected TIME RANGE.

Δ TIME - 10-turn locking dial potentiometer to select time window width from 0 to 100% of selected TIME RANGE.

SCA IN/OUT - Toggle switch to select whether TAC output is gated with Time SCA.

STROBE MODE - Toggle switch to select INTernal or EXTernal strobe operation.

CONVersion READY WIDTH - 22-turn, screwdriver adjustable potentiometer determines time duration that STROBE input will initiate output pulse; jumper selectable to 1 to 20 μsec or 10 to 200 μsec, shipped for 1 to 20 μsec.

STOP INHIBIT - Toggle switch to enable (ON) or disable (OFF) STOP INHIBIT RANGE adjustment.

STOP INHIBIT RANGE - 22-turn potentiometer to reject unwanted STOP input signals from a minimum of 1% up to 100% of selected TIME RANGE (minimum 20 nsec).

INTERNAL CONTROLS

TAC OUTPUT WIDTH - Jumper plug to select 0.5, 1.0 or 2.5 μsec output pulse width for both SCA and TAC outputs.

TAC OUTPUT IMPEDENCE - Jumper plug to select $Z_o = 10$ ohms or $Z_o = 93$ ohms.

START +/−, STOP +/−, GATE +/− : Jumper plug to determine input polarity of respective signals.

VALID START +/−, VALID STOP +/−, SCA +/−, STOP INHIBIT +/−, CONVERSION READY +/− : Jumper plugs to select either positive voltage or negative current mode outputs for the related BNC connectors.

GATE Z_{in}, STROBE Z_{in} - Jumper selectable for 50 ohms or 1 k ohm on positive input signals.

CONV READY - Jumper selectable for 1 to 20 μsec or 10 to 200 μsec range.

PERFORMANCE

TIME RESOLUTION - < 0.01% of full scale plus 5 psec FWHM for all ranges. Time resolution is insensitive to count rate of START/STOP ratio.

TAC INTEGRAL NONLINEARITY - < ± 0.1% from 5 nsec to full scale on X1 MULTIPLIER range; < ± 0.1% from 1% to 100% of full range for all higher ranges.

TAC DIFFERENTIAL NONLINEARITY - < ± 2% from 5 nsec to full scale on X1 MULTIPLIER range; < ± 2% from 1% to 100% of full range for all higher ranges.

SCA TIME/Δ TIME INTEGRAL NONLINEARITY - < ± 0.5% of full scale.

TAC OUTPUT TEMPERATURE STABILITY - Better than ± 0.01%/°C (± 100 ppm/°C) of full scale.

Specifications (Cont'd.)

SCA TIME/Δ TIME TEMPERATURE STABILITY — Better than ± 0.01%/°C (± 100 ppm/°C) of full scale.
OUTPUT DELAY/OUTPUT WIDTH TEMPERATURE STABILITY - Better than ± 0.01%/°C (± 100 ppm/°C) of full scale.
TEMPERATURE OPERATING RANGE - 0 to 50°C.
TAC OUTPUT DROOP - < 0.015%/μsec of delay from completed conversion to TAC output. Delay time is determined by front panel DELAY setting or external strobe acceptance, or both.
INTERNAL CLEAR TIME - Fixed 1 μsec recovery time on X1, X10 and X100 MULTIPLIER ranges, and 10 μsec on X1K and X10K MULTIPLIER ranges; occurs after each normal output and each overrange.
GATE PEDESTAL - Essentially zero pedestal, factory calibrated.
SCA OUTPUT TIME WALK - None, with respect to TAC output.
MINIMUM START TO STOP CONVERSION TIME - ≈ 2 nsec.
COUNT RATE CAPABILITY - START, STOP, GATE inputs capable of count rates greater than 25 MHz.

CONNECTORS

All signal connectors are located on the front panel and are BNC type.

POWER REQUIREMENTS

+24 V dc — 50 mA	+12 V dc — 250 mA
-24 V dc — 50 mA	-12 V dc — 250 mA

PHYSICAL

SIZE - Standard double-width NIM module 6.85 × 22.12 cm (2.70 × 8.71 inches) per TID-20893 (rev.)
NET WEIGHT - 1.3 kg (2.8 lbs.)
SHIPPING WEIGHT - 2.3 kg (5.0 lbs.)

Section 4.
Operating Instructions

4.1 GENERAL

The purpose of this section is to familiarize the user with the operation of the Model 2143 Time Analyzer and to check that the unit is functioning correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

4.2 INITIAL CHECKOUT

Before attempting to use the Model 2143 Time Analyzer, the user should remove the left side cover of the instrument and set the internal jumper plugs to provide the desired input and output characteristics. Reference Section 3.3 for the locations of these jumpers. The functions of each jumper are elaborated below. It is recommended that these selections be performed with the power OFF.

INPUTS: The polarity of the START, STOP, and GATE input signals is selected by jumper plugs. Refer to figure 3.2 for their location. Since most fast timing discriminators provide a negative output these jumpers are shipped in the negative position and should be changed only if the desired input signal is positive.

Since reflection-induced ringing can cause timing degradation, both polarities of the START, STOP and GATE inputs are terminated in 50 ohms.

The input circuits for VALID CONVERSION and RESET/INHIBIT each accept positive voltage or negative current NIM pulses without the need for polarity selection switches. The input impedance for the negative current pulse is the usual 50 ohms. The input impedance for the positive voltage pulse may be set for an effective 50 ohms, or 1k ohms to accommodate the characteristics of different sourcing equipment. The user should select the 50 ohm impedance if the input pulse is to come from an instrument having an output impedance of less than 10 ohms. This will minimize reflection-induced ringing which could cause a degradation of performance in the Model 2143 due to its very sensitive input circuits. For use with instruments which provide a 50 ohm nominal output impedance, the 1k ohm position of the jumper plug is recommended.

OUTPUTS: The VALID START, VALID STOP, SCA, MONITOR, and VALID CONVERSION outputs each may be selected individually to provide a positive voltage or a negative current NIM pulse. The positive voltage pulse may further be selected to source either a 5 V or 8 V nominal open circuit voltage level to accommodate the threshold and interface needs of other instruments. The positive voltage pulse output provides a 50 ohm nominal source impedance to prevent ringing and pulse reflections, which can cause spurious effects or multiple pulse counting. The negative current pulse output is shunt terminated in 50 ohms nominal for the same reason.

The user may select the positive voltage pulse by setting the appropriate jumper near the identified output to +, and the negative current output by setting the jumper to −. The positive voltage pulses are normally set to 5 V, and can be individually increased to 8 V by removing a socketed 1.5K ohm resistor near the screened-on output function name.

WIDTH: The TAC output pulse may be set for a nominal width (at the 50% level) of 0.5, 1.0, or 2.5 μs to accommodate the pulse requirements of the ADC being used. In each case, the risetime of the output pulse is controlled to 0.25 μs to prevent slew rate-induced errors in the peak detector of the ADC. The user should set the WIDTH jumper plug into the sockets corresponding to the desired pulse width. Note that the SCA output pulse (either positive or negative) will have the same width as the TAC output as selected above.

OUTPUT IMPEDANCE: The output impedance of the TAC output may be selected as either 10 ohms or 93 ohms. Use 10 ohms for driving short lengths of cable connected to an MCA. For long cable runs or when source matching is desired, use 93 ohms.

VALID CONVERSION: The width of the VALID CONVERSION signal is adjustable using a front panel potentiometer. The Valid Conversion jumper plug selects one of the two adjustment ranges provided. When this jumper is set to X1, the front panel potentiometer provides a range of 2 to 20 μs. When the jumper is set to X10, the range is 20 to 200 μs.

Once the internal jumper plugs have been set to provide the input/output characteristics desired, the user should make external cable connections to the instrument to set up a familiarization test. Again, these connections should normally be done with power OFF.

The most straightforward method to verify proper operation and/or calibration of the Model 2143 Time Analyzer is to apply a known fixed-frequency pulse to both the START and STOP inputs and to observe the amplitude of the TAC output. As illustrated in Figure 4.1, a pulse waveform (either positive or negative) is first applied to the STOP input and then linked by a "tee" to the START input. The input signal should be adjusted to deliver $\geq$2 V if using positive signals, and $\geq$ −250 mV for negative signals. Note that with START and STOP linked together, the net input impedance will be reduced to as low as 25 ohms in this demonstration, and will attenuate a pulse generator's normal output. Since the START signal is delayed by the extra cable length, the STOP signal arrives first and is ignored. Thus, a START signal and the STOP signal one cycle later generate a conversion time equal to the period of the input signal.

For a reference condition, a 1 MHz pulse with a width of up to 0.5 μs, or a suitable square wave from a laboratory function generator, may be used initially. It is suggested that the Model 2143 be configured as follows:

Internal Jumpers
- START, STOP, GATE as needed for input signal
- RESET, STROBE impedance to 50 ohms
- LOGIC OUTPUTS +/- to +
- WIDTH to 1 μs
- OUTPUT IMPEDANCE to 10 ohms
- VALID CONVERSION to 1

Front Panel
- TIME RANGE to 20
- MULTIPLIER to X100
- COINC/ANTI to ANTI
- STOP INHIBIT to OFF
- DELAY to MIN
- STROBE MODE to INT
- SCA ON/OFF to OFF

Given the above setup, the user should observe a TAC output pulse of 5 V peak amplitude on an oscilloscope. A change in the frequency (rate) of the applied input will then result in a proportional change in the amplitude of the TAC output. By reducing the rate to approximately 0.45 MHz (2.2 μs period), the user may verify that the TAC output disappears and the front panel OVERRANGE indicator will come on.

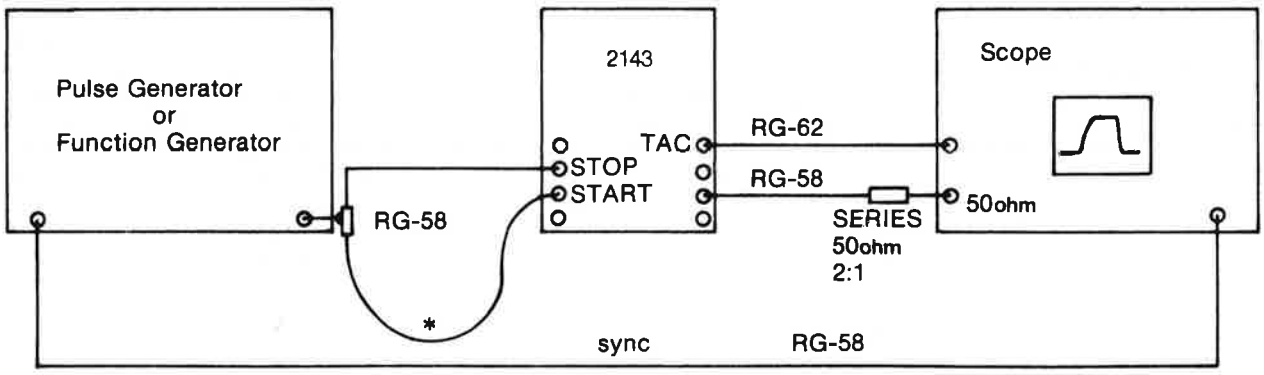


Figure 4.1a
Checkout Setup

*Note: Because of the internal analog and logic propagation delays of the Model 2143, a cable about 10 feet (3 m) in length should be used between the tee connector and the START input to obtain a useful TAC output using this setup.

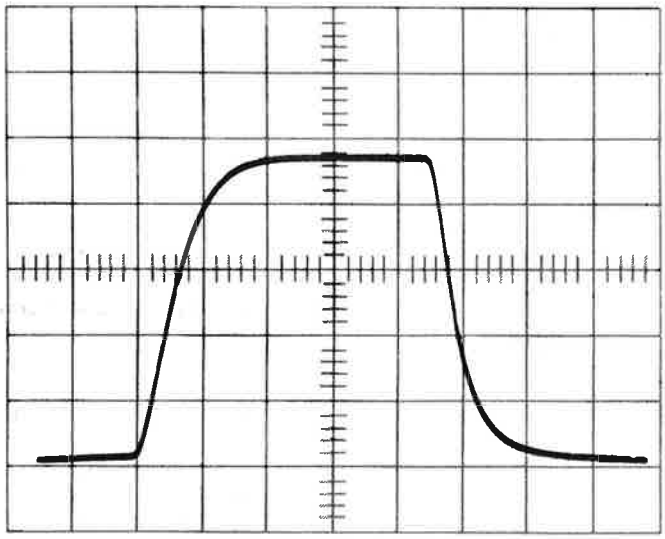
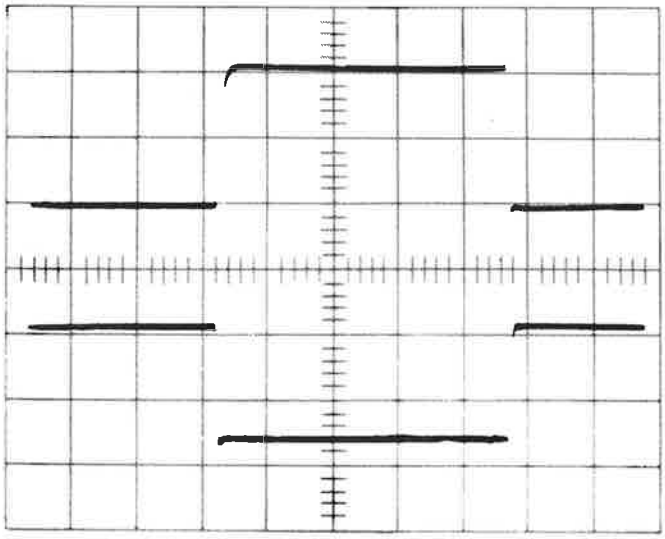


Figure 4.1b
Typical TAC Output Signal

At this point the user may examine the VALID START, VALID STOP, and SCA output pulses (see discussion of SCA below) in either + or - modes. Figure 4.1 illustrates the proper method of connection to use when observing these outputs on an oscilloscope. Figure 4.2 illustrates typical SCA output pulses using the prescribed termination; Figure 4.3 illustrates the aberrations caused by ungrounded oscilloscope probes (top) and oscilloscope input capacitance on direct viewing (bottom).

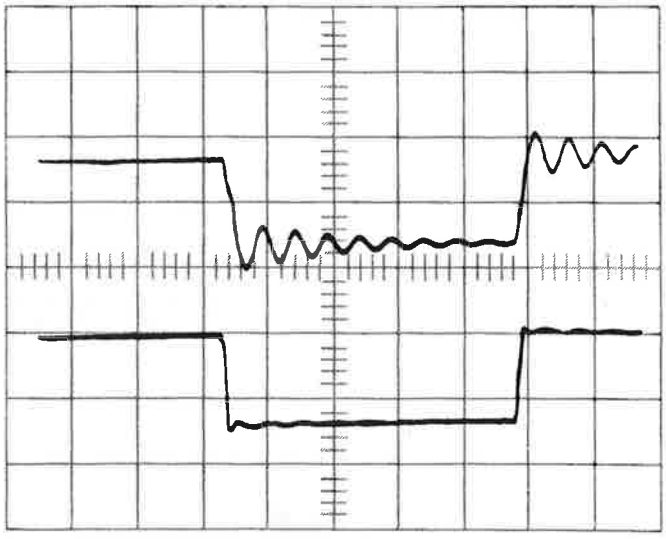


UPPER: + 2 V/cm

LOWER: -0.2 V/cm

HORIZ. at 100 nsec/cm

Figure 4.2
Typical SCA Output Pulses



UPPER: Ungrounded Scope Probe

LOWER: At scope without proper termination

Both Vert. at 0.5 V/cm
Horiz. at 100 nsec/cm

Figure 4.3
-SCA Output Pulses

4.3 USE OF SCA FUNCTIONS

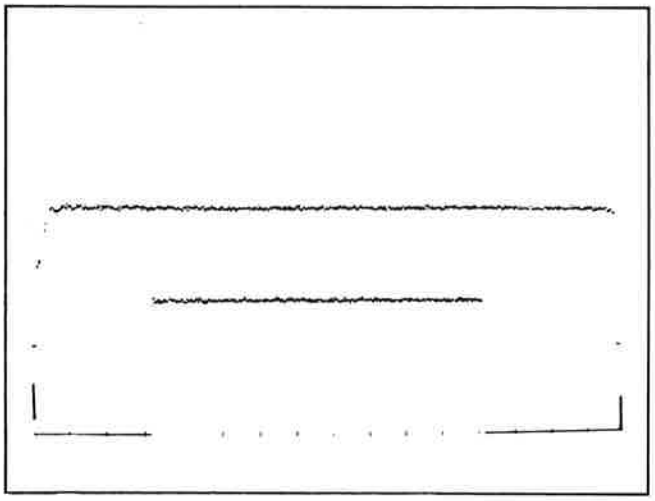
The Time Single Channel Analyzer function is most commonly used to restrict the spectrum of pulse pairs received by the instrument to a narrow range of most interest in a given experiment. These may represent coincidences from several detectors representing particle disintegrations, annihilations, lifetimes, etc. The Time SCA function evaluates the result of a given time-to-amplitude conversion and generates a logic ouput for input time differences within the bounds set by the front panel controls.

The TIME control on the front panel sets the lower limit for the SCA region or window, as scaled from 0 to 100% of any selected time range. The Δ TIME control sets the width of the SCA window over the same 0 to 100% range, so that the upper limit of time is read as the sum of TIME + Δ TIME dials.

The logic output decision of the SCA function may be used to gate the TAC output so that only those pulses within the set SCA limits will be delivered to an external ADC for analysis. This is done by setting the front panel SCA ON/SCA OFF switch to SCA ON. When this switch is set to SCA OFF, all outputs will be delivered to the ADC.

Using the setup of Section 4.2, but with SCA ON, and the front panel TIME dial control set to 2.0 and the Δ TIME dial control to 6.0, an oscilloscope observation of the TAC output will be seen only for pulses between 2.0 and 8.0 V as the input test frequency is varied up and down.

Figure 4.4 below depicts the differential nonlinearity of the Model 2143 as observed on a Canberra MCA using random noise pulses to generate a time spectrum on the 20 × 100 nanosecond range, and with the SCA set as above. The sharp skirts of the spectrum attest to the precision of the SCA built into the Model 2143.



UPPER TRACE:
without SCA

LOWER TRACE:
SCA IN, with
TIME = 2.0
Δ TIME = 6.0

Figure 4.4
2000 nsec Differential Nonlinearity

4.4 USE OF THE STOP INHIBIT FUNCTION

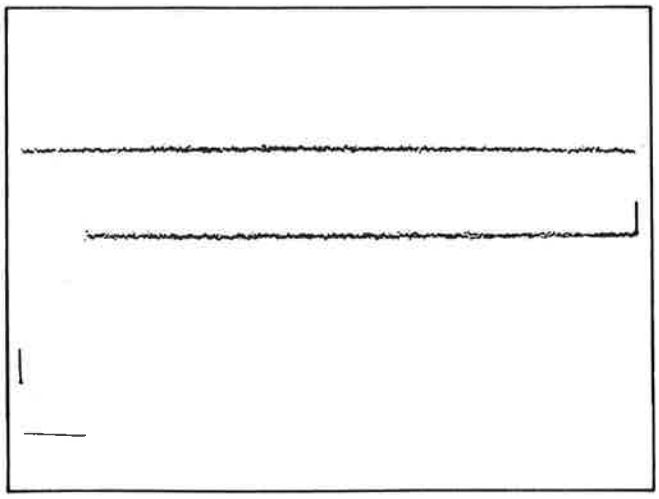
It is possible in some experiments to have STOP pulses that are caused by, or contaminated by, noise or by pulse reflections. If these unacceptable STOP pulses were not rejected in some way, they would initiate unintended time analysis cycles, contribute to the Time Analyzer's dead time, and thus affect the high throughput qualities of the Model 2143.

The self-contained Time SCA would reject these STOP pulses by creating a time window which would restrict the TAC output to acceptable pulse pairs. However, this would still incur increased dead time and possibly block time analysis on a desired START/STOP pair.

The STOP INHIBIT function has been designed to overcome this limitation by setting a "time threshold" which begins with an accepted START pulse and is adjusted by the operator to end just before an acceptable STOP pulse. The Time Analyzer will not recognize STOP pulses which are below this threshold.

By careful adjustment of the STOP INHIBIT control, unacceptable (early) STOP input pulses can be suppressed, Time Analyzer dead time reduced and the generation of false TAC outputs avoided. As an aid in setting the Inhibit threshold, there is a MONITOR output BNC which provides a logic pulse whose width is equal to the blocking time interval following an accepted START input pulse.

Figure 4.5 illustrates the effect of a STOP INHIBIT set at approximately 10% of the 1 microsecond range of the Model 2143, as seen on a flat time spectrum using random pulser inputs.



UPPER TRACE:
Typical 1 μsec time spectrum.

LOWER TRACE:
Same as above with STOP INHIBIT set to approximately 10% of full scale.

Figure 4.5
Effect of STOP INHIBIT on a Time Spectrum

4.5 USE OF THE COINCIDENCE FUNCTION

The most common use of the Coincidence function is for early (prompt) gating of START/STOP pulse pairs as an aid in reduction of the Time Analyzer's dead time. Since the internal logic of the Analyzer is set to reject any STOP pulses that arrive before an accepted START pulse, a means of accepting or rejecting a START pulse will allow the operator to control pulse pair conversion.

By selecting one of the two modes of gating and applying a specified signal to the GATE connector, the operator can enable or disable the acceptance of a START pulse, and thus the conversion of any pulse pairs, depending on the established criteria of a given experiment.

In the COINCidence mode, an applied GATE signal will enable the operator to select a START pulse for beginning a conversion cycle by causing the GATE signal to coincide with the selected START pulse. Noncoincident pulse pairs will not be processed by the Analyzer.

In the ANTICOINCidence mode, the GATE signal will inhibit the acceptance of a START pulse and prevent the occurrence of an undesired conversion cycle. All other pulse pairs will be converted.

In either mode, an applied GATE signal will affect acceptance of a START pulse if the GATE signal is received at least 10 nsec prior to and overlaps the START pulse by approximately 50 nsec.

Note that if the Coincidence function is not to be used, the mode switch must be left in the ANTICOINCidence position and the GATE input must be left open.

4.6 USE OF THE STROBE FUNCTION

The Strobe function allows the external logic to determine when and if a TAC output is generated. This occurs after the TAC conversion and reduces ADC dead time by preventing undesired TAC outputs. Figure 4.6 shows timing diagrams, illustrating the use of the Strobe function.

When the Strobe Mode switch is set to INTernal, the TAC functions normally. After the DELAY period, every conversion produces a TAC output pulse.

In the EXTernal Strobe Mode an external Strobe signal must be applied during the VALID CONVERSION interval to produce a TAC output pulse. This interval starts at the end of DELAY and has a width determined by the front panel CONV. READY WIDTH potentiometer and the internal X1 or X10 jumper.

If a Strobe signal is applied during the VALID CONVERSION interval a TAC output pulse will be generated immediately. If the Strobe signal is absent during the VALID CONVERSION interval, the TAC is reset at the end of VALID conversion and no output pulse is generated.

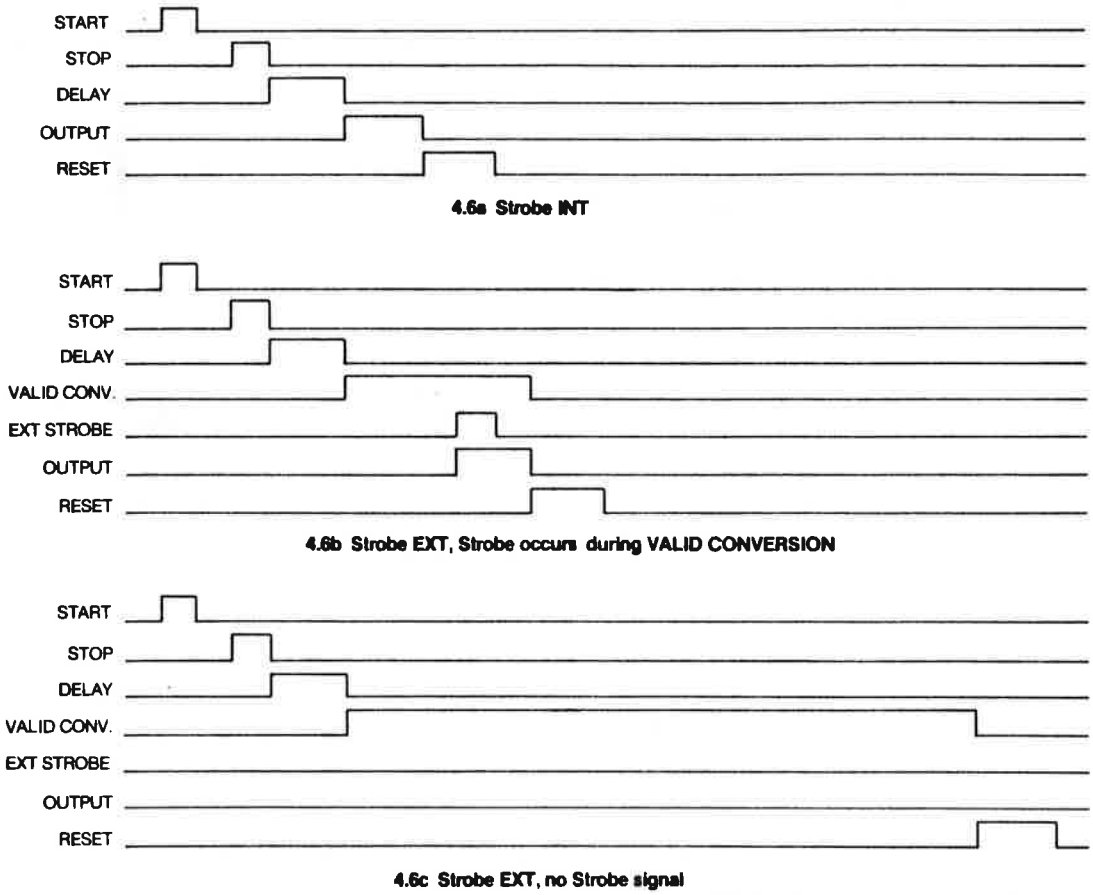


Figure 4.6
Timing Relationship of TAC Signals

Section 5.
Theory of Operation

The Model 2143 Time to Amplitude Converter (TAC) is shown in block diagram form in figure 5.1. The basic time to amplitude converter consists of an integrator which charges a capacitor with a constant current during the time interval from a START signal to a STOP signal. The current linearly charges the capacitor, producing a ramp voltage. After the STOP signal, the voltage present on the capacitor is linearly proportional to the START to STOP time interval.

The other portions of the circuitry shown in the block diagram serve to interface the basic time to amplitude circuit to the inputs and outputs of the TAC or to provide various other logic or control functions. The input circuits and the latches generate signals which control the switches associated with integrating capacitor and the current source. The buffer is a high input impedance, low output impedance circuit which provides drive capability to the output linear gate and amplifier as well as the various comparitors for the OVERRANGE, SCA, and MONITOR functions. The control logic generates control signals which activate various portions of the circuit sequentially during each conversion.

Input signals are applied to the START, STOP, and GATE input circuits. All three circuits are substantially the same. Each consists of a high speed comparator with the capability of responding to a positive or negative NIM input signal with the polarity chosen by the position of the input jumper. When a suitable input occurs, the comparator output changes state and provides a logic signal to drive the inputs of the latches that follow. The input circuits are very fast and are limited in count rate primarily by the width of the input signal. This allows high count rate signals to be applied directly to the TAC input, with no timing degradation.

The START and STOP input circuits drive the clock inputs of high speed D-type latches. The GATE input circuit drives the D input of the START latch and is able to provide fast COINCIDENCE/ANTICOINCIDENCE gating. The START latch output drives the D input of the STOP latch and ensures that STOP signals prior to a START signal are signal rejected. The outputs from the START and STOP latches provide a logic signal which is true for the START to STOP signal time interval. This signal and a separate output from the START latch are used to drive the switches which control the actual time to amplitude conversion.

In order to provide the 2143's various RANGE and MULTIPLIER, both the current source and the integrating capacitor are variable. The current source, consisting of the operational amplifier A21 and transistors Q12 and Q13 is varied with the front panel RANGE switch to provide the 20, 50, and 100 RANGEs. Likewise the integration capacitor, consisting primarily of C39, C40, C41, and C42, is chosen with the front panel MULTIPLIER switch.

Prior to a conversion, the integrating capacitor is clamped at ground potential. At the start of the conversion, the clamp transistor (Q18) is turned off by a logic signal from the START latch, thus steering the current source to the integrating capacitor through Q19. This results in a negative going ramp starting from ground on the integrating capacitor. When a STOP signal is received, the current source is steered away from the integrating capacitor by Q20. The integrating capacitor retains the charge it received during the conversion. This charge results in a fixed voltage on the integrating capacitor which represents the time interval converted.

Transistors Q25, Q26, and Q27 form a unity gain, zero offset buffer which provides a high impedance load on the integrating capacitor. This avoids discharging the integrating capacitor while still providing drive capabilities to the output circuitry and comparators which follow the buffer.

Transistors Q1, Q2, Q3, Q5, and Q6 with A6 form the output circuit, which has an inverting gain of two. Thus a full scale conversion is −5 V on the integrating capacitor and +10 V at the output. The output also functions as a linear gate. A shaped output pulse is generated when Q4 is driven off by the OUTPUT drive circuitry.

A conversion is considered valid if a STOP signal is received during the conversion interval. Receipt of the STOP signal steers the current source away from the integrating capacitor, as described above. It also initiates the output sequence controlled by the string of logic one-shots A20a, A20b, A16a, and A16b for DELAY, VALID CONVERSION, OUTPUT, and RESET, respectively.

For a valid conversion, an output signal is generated by the OUTPUT one-shot and the entire circuit is RESET. This clears the logic, clamps the integrating capacitor to ground, and prepares the circuit for the next conversion. If there was no STROBE signal in the VALID CONVERSION interval or if an OVERRANGE was detected, the circuit is RESET without generating an output.

Several comparators monitor the output fo the buffer: the OVERRANGE comparator, the two SCA comparators, and the STOP INHIBIT comparator. The OVERRANGE comparator detects an overrange condition if the ramp exceeds −5 V. If this occurs, the converter circuitry is reset without generating an output. The two SCA comparators determine if the conversion is within the range set by the Lower Level and Upper Level controls. The STOP INHIBIT comparator determines when a selected percentage of the conversion range has been exceeded and allows STOP inputs to be accepted if this function is enable.

Five logic outputs are provided by the 2143: the VALID START, VALID STOP, SCA, CONVERSION READY, and STOP INHIBIT MONITOR outputs. All are identical and consist of a positive NIM voltage driver and a negative NIM current driver. The desired output polarity is selected by a jumper plug.

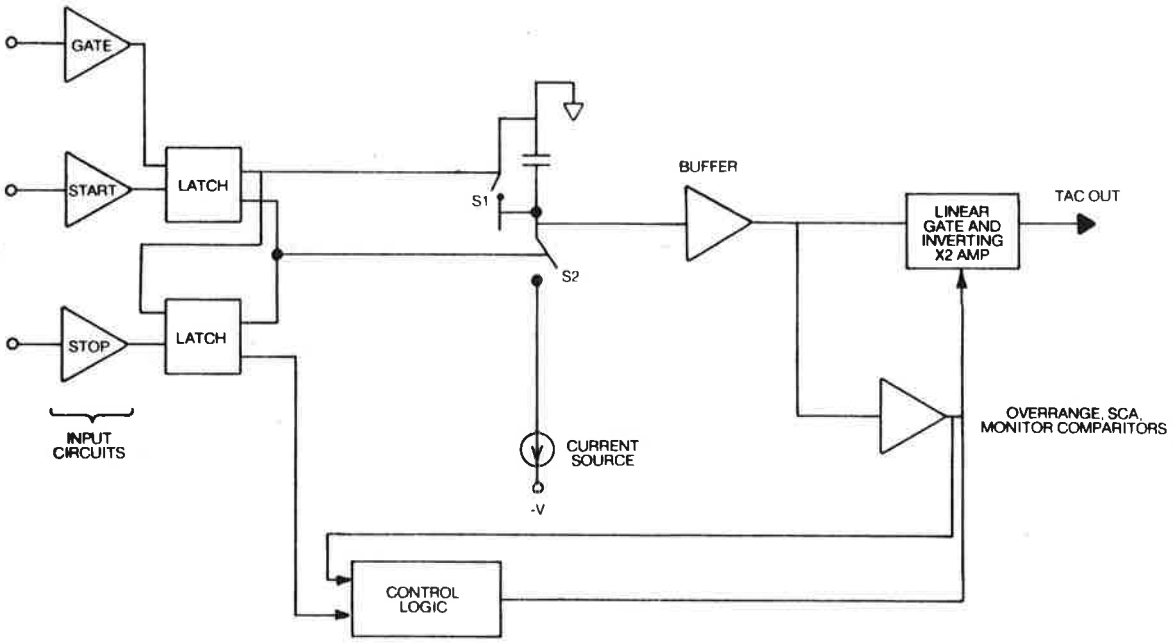


Figure 5.1
2143 Block Diagram

Warranty

Canberra (we, us, our) warrants to the customer (you, your) that for a period of ninety (90) days from the date of shipment, software provided by us in connection with equipment manufactured by us shall operate in accordance with applicable specifications when used with equipment manufactured by us and that the media on which the software is provided shall be free from defects. We also warrant that (A) equipment manufactured by us shall be free from defects in materials and workmanship for a period of one (1) year from the date of shipment of such equipment, and (B) services performed by us in connection with such equipment, such as site supervision and installation services relating to the equipment, shall be free from defects for a period of one (1) year from the date of performance of such services.

If defects in materials or workmanship are discovered within the applicable warranty period as set forth above, we shall, at our option and cost, (A) in the case of defective software or equipment, either repair or replace the software or equipment, or (B) in the case of defective services, reperform such services.

LIMITATIONS

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES OR REMEDIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, EXEMPLARY, PUNITIVE, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE. REPAIR OR REPLACEMENT OF THE SOFTWARE OR EQUIPMENT DURING THE APPLICABLE WARRANTY PERIOD AT CANBERRA'S COST, OR, IN THE CASE OF DEFECTIVE SERVICES, REPERFORMANCE AT CANBERRA'S COST, IS YOUR SOLE AND EXCLUSIVE REMEDY UNDER THIS WARRANTY.

EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident, neglect or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

Software License

When purchasing our software, you have purchased a license to use the software, not the software itself. Because title to the software remains with us, you may not sell, distribute or otherwise transfer the software. This license allows you to use the software on only one computer at a time. You must get our written permission for any exception to this limited license.

BACKUP COPIES

Our software is protected by United States Copyright Law and by International Copyright Treaties. You have our express permission to make one archival copy of the software for backup protection. You may not copy our software or any part of it for any other purpose.