DUAL COUNTER
Model 2072A

0788

Operator's Manual

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M156R2 7/88 Printed in U.S.A.

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FIGURE LISTING

Section 1. Introduction

The Canberra Model 2072A Dual Counter provides, in a single width NIM module, two eight decade counters. Both count INputs accept fast negative NIM or positive pulses, jumper selectable. A discriminator is provided allowing positive inputs to be compatible with unipolar and bipolar linear signals or TTL logic pulses. The front panel positive DISCriminator covers an input range of +100 mV to +10 V permitting selective counting, eliminating spurious counting from noise or other erroneous pulses.

The Model 2072A accommodates input counting rates of 100 million counts per second (100 MHz) for negative inputs and 25 million counts per second (25 MHz) for positive inputs.

Display of either counter's content is accomplished with a six digit Liquid Crystal Display. The LCD includes eight annunciators which describe the display and dynamic state of the unit. Automatic x100 range shift provides an indication of the six most, or six least significant digits.

Master-Slave system operation can be accomplished via the front or rear panel interconnection of the ENABLE signal, or by either of the two optional I/O interfaces.

The Canberra NIM Daisy Chain option provides interfacing to all Canberra printing counters, timers, and readout scanners. Standard with the NIM Daisy Chain option is a Read Out Buffer capability such that with any number of counting modules a total of only 100 microseconds dead time is required.

The alternate Canberra GPIB (IEEE-488) option provides interfacing to a GPIB bus, and allows a GPIB Controller to start, stop, and read out counting systems.

For an accumulation of data in channel A, a jumper can be changed to prevent the resetting of channel A.

External connection to the A or B GATE inputs will permit gating of incoming pulses in the respective channel. The gating of external time inputs allows 1 μsec resolution. Thus when a system-busy signal is connected to this input, the 2072A will provide extremely accurate dead-time corrections.

Section 2. Specifications

2.1 INPUTS

A and B IN - Front panel BNC connectors accept positive linear, TTL, or negative NIM fast logic signals, jumper selectable. Positive operation accepts unipolar, bipolar, or TTL signals; amplitude: 0 to +10 V, +12 V maximum; input amplitude must exceed the adjustable discriminator level for 20 nsec to be counted. Negative NIM fast logic amplitude: -0.6 V to -1.6 V; minimum width 4 nsec below -0.6 V; input rise and fall times: 1 nsec to 300 nsec; $Z_{in} \approx 1$ k ohms dc for positive signals and ≈ 50 ohms for negative signals.
GATE A - Counting control for channel A. Amplitude: + 4 to + 5 V or open circuit allows counting; zero to + 0.8 V inhibits counting; $Z_{in} \approx 100$ k ohms to + 5 V bus. When used as time gating, system busy can be used for accurate dead-time correction.
GATE B - Counting control for channel B. Signal specifications and time gating identical to GATE A.

2.2 INPUT/OUTPUT

ENABLE - Front panel BNC connector, bidirectional as input or output, open collector function, logic "0" OR; sinks 20 mA, sources from 4.7 k ohm to + 5 V bus.
As an Output - Provides counting control to other 2071A, 2072A or compatible modules; 0 to + 0.8 V enables counting, + 4 V to + 5 V disables counting.
As an Input - 0 to + 0.8 V enables counting mode; + 4 V to + 5 V or open circuit disables counting mode.

ENB/OVF - Rear panel BNC connector having a multifunction capability, ENABLE or OVERFLOW; internally selected with a jumper plug; shipped in the OVF position.
OVF - Outputs a + 5 V pulse coincident with the eighth decade reset; rise and fall times < 200 nsec; width 3 μsec nominal; dc coupled; sinks 5 mA, sources 2.5 mA at 2.5 V; internal jumper selects channel A or B as source. Shipped in the channel A position.
ENB - Same as front panel ENABLE above.

2.3 FRONT PANEL CONTROLS

START/STOP - Two-position momentary toggle switch initiates or terminates a counting sequence.
RESET - Manual push-button resets both counters to zero.
A/B DISPLAY SELECT - Two-position toggle switch selects which counter's contents are displayed on the LCD.

2.4 PERFORMANCE

CAPACITY - Eight decades per channel, allowing $10^8 - 1$ counts in each.
COUNT RATE - 100 MHz max., negative; 25 MHz positive.
PULSE PAIR RESOLUTION - 10 nanoseconds, negative; 40 ns positive.
TEMPERATURE OPERATING RANGE - 0 to 45° C.

INDICATORS - Six digit Liquid Crystal Display with auto (x100) shift for displaying six most-significant digits. Five annunciators on LCD describe the display. These are: OF (overflow), x100, CNT, A, B. Active counting is indicated by CNT blinking. Leading zeroes are suppressed.

2.5 INTERNAL CONTROLS

STANDARD JUMPERS (When set, perform the following):

- Inhibit reset of channel A when starting. In this mode channel A accumulates counts and is reset only by the manual pushbutton.
- Select OVERFLOW or ENABLE as the function of the rear panel connector.
- Select OVERFLOW output from channel B instead of channel A.
- Allow a pulse on ENABLE INPUT to start the module.
- Select input A and B to accept positive linear and TTL, or negative NIM signals.

2.6 POWER

	2072A Alone	with -01	with -02
+12	120 mA	155 mA	123 mA
-12	200 mA	235 mA	203 mA
+24	35 mA	35 mA	35 mA
-24	0	0	0

2.7 PHYSICAL

SIZE - Standard single width NIM module; 3.43 × 22.12 cm (1.35 × 8.71 inches) per TID-20893 (rev. A)
NET WEIGHT - 0.94 kgs (2.0 lb.)
SHIPPING WEIGHT - 3.2 kgs (7.0 lb.)

2.8 OPTION: 207x-01 GPIB (IEEE 488) INTERFACE

A. Features

- Asynchronous ASCII data transmission bit parallel, character serial
- Uniquely addressable, switch controlled
- Talk/Listen mode
- Talk Only mode
- Auto recycle minimizes readout dead time
- Field installable
- Form feed or carriage return at end of word

B. Description

The General Purpose Interface Bus links a Canberra NIM counting module into the IEEE 488 standard communications network. As a Listener, this interface receives Start, Stop, and Readout commands from a controller. As a Talker, it supplies its accumulated data to a peripheral device. A Talk Only mode provides a controllerless means for a single module to read out to a peripheral Listener. The Auto Recycle mode allows the selected module to place itself (and the rest of the Canberra counting system) back into the count mode at the conclusion of its readout, thus minimizing system dead time. A side panel cutout provides access to Set or Verify a Talk/Listen Address, select Talk Only mode, enable Auto Recycle, or select Form Feed/Carriage Return at the end of a word. This interface is a single PC board with a connector that allows convenient field installation.

C. Specifications

SIGNALS - The input/output signals on the GPIB connector are TTL compatible. True equals 0 to + 0.4 V, False equals + 2.5 to + 5 V.
CONTROLS - Side-panel cutout provides access to:
Address select switches (5)
Talk-Listen/Talk Only switch
Auto Recycle switch
FF/CR switch
Internal jumper enables Stop command response (DC 2).
CONNECTOR - Standard GPIB connector on rear panel.
CONFORMITY - Option 01 contains the following subset of capabilities (for explanation see IEEE-488 Standard) SH1, AH1, T1, TE0, L0, LE0, SR1, RL0, PP0, DT0, C0, DC0/DC2 selectable.

D. General Description of GPIB

The General Purpose Interface Bus is a link or network by which system components communicate with each other. Each system participant performs at least one of three roles: Controller, Talker, or Listener.

A Controller manages bus communications primarily by directing or commanding which devices are to send data to other devices (Talker), or receive data from other devices (Listener) during an operational sequence. A controller may also be interrupted or it may command specific action between devices.

The GPIB consists of 16 lines which are grouped into three sets according to function; there are 8 data lines, 3 control lines, and 5 general management lines. The 8 data lines carry ASCII characters (bit parallel) asynchronously; the control lines provide a data transfer handshake compatible with both slow and fast devices; the bus management lines allow initialization, interrupts, and special controls.

E. Cable

One Canberra Model C2072-2 GPIB Data/Control cable 0.6 m (2 feet) long is supplied for connection to the GPIB bus.

2.9 OPTION: 207x-02 CANBERRA NIM DAISY CHAIN INTERFACE

A. Features

- Synchronous BCD data transmission bit parallel, character serial
- Readout sequence determined by interconnect order
- Field installable
- System control via individual Start, Stop, and Reset signals
- Compatibility with Canberra counters and scanners
- Readout Buffer

B. Description

The Canberra NIM Daisy Chain Interface Option provides the basic 2072A module with a readout/control capability compatible with previous Canberra data-acquisition series modules.

Readout Buffering is available by moving jumper DD to position CC on the 2071A Master unit. This sets the Recycle

time to 100 microseconds. Operating the Master, and hence the entire system, in the Recycle mode provides a minimal (100 microsecond) dead time buffered counting system.

The problem of data transfer from the eight digit 2072A to the standard six-digit system is handled by a toggle switch on the interface board. It selects either the six most-significant digits or the least-significant digits. Two digits are lost in either case.

Control signals, Start, Stop, and Reset are received only if the unit is to be a system slave. A master until will generate Start, Stop, and Reset. This logic is under internal jumper control.

C. Signals

CONTROL IN - Accepts Start, Stop, Reset, and Print pulses (5 V negative going from + 5 V level, rise time 500 nanoseconds maximum, width 1.0 microseconds minimum. Also HOLD command (dc level change from + 5 V to + 0.5 V maximum during printout) is accepted. Rear panel 15-pin "D" connector (Amphenol 17-10150).

CONTROL OUT - Provides Start, Stop, and Reset commands (5 V negative going pulses from + 5 V level, rise time 500 nanoseconds maximum, width 1.9 microseconds minimum). Data output information is presented in the form of Serial BCD (logic 1 = + 4 to + 5 V dc, logic 0 = 0 to + 0.5 V dc). This connector also provides the "next unit" Print command; eighth and successive Print command pulses are routed out via a logic gate. All control lines except Print command are wired directly between Control In and Control Out connectors. Rear panel 15-pin "D" connector (Amphenol 17-20150).

D. Controls

SIGNIFICANT DIGIT SWITCH ($10^7 - 10^2/10^5 - 10^0$) - $10^7 - 10^2$ position selects readout of the six most significant digits of the eight-digit word. $10^5 - 10^0$ position selects readout of the six least significant digits of the eight-digit word. Jumpers allow the Model 2072A to act as a system master or as a slave.

E. Cable

One Canberra Model C1404-2 Data/Control cable 0.6 m (2 feet) long is supplied for connection to other Canberra data acquisition series modules.

Section 3.
Controls and Connectors

This section outlines the uses of the Model 2072A's controls and connectors. A complete listing of signal parameters will be found in Section 2, SPECIFICATIONS.

3.1 FRONT PANEL

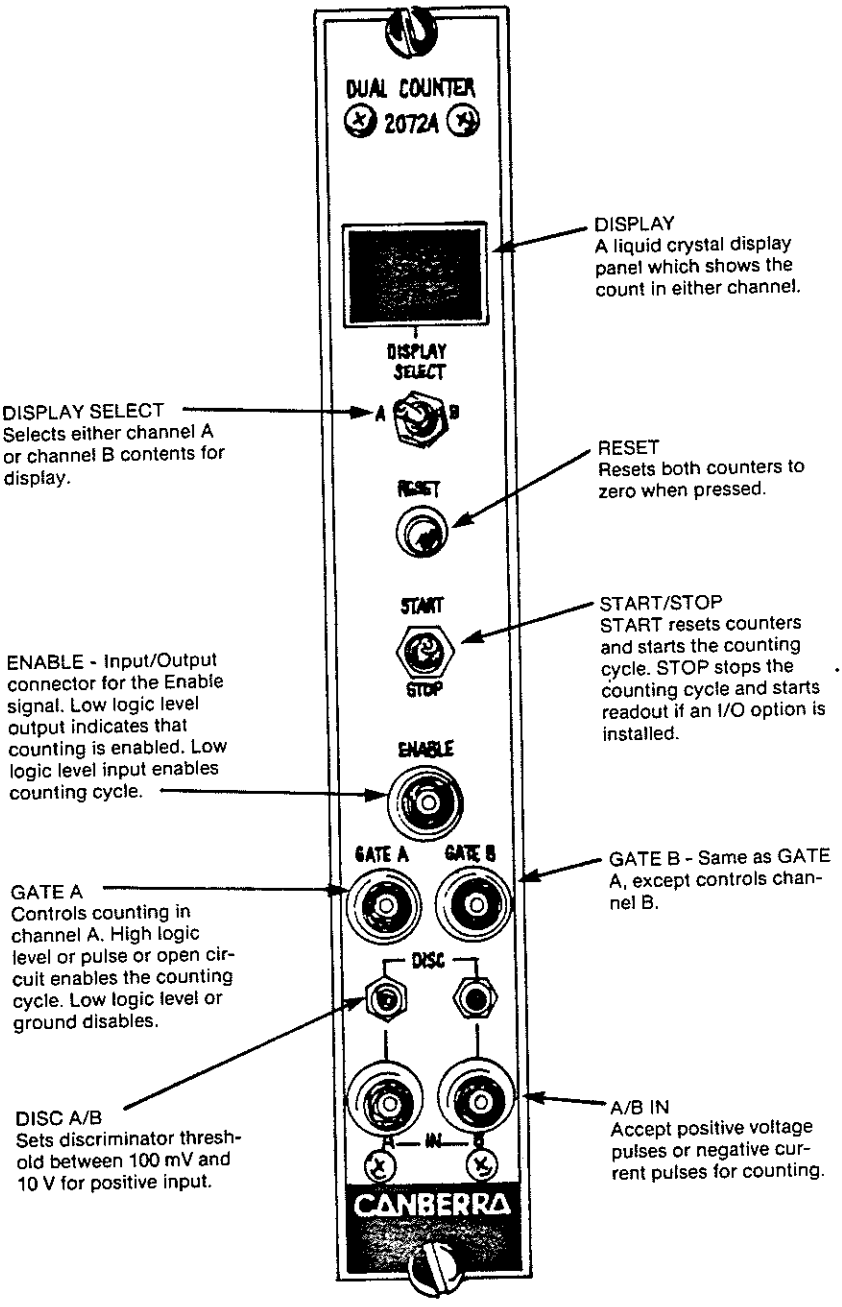
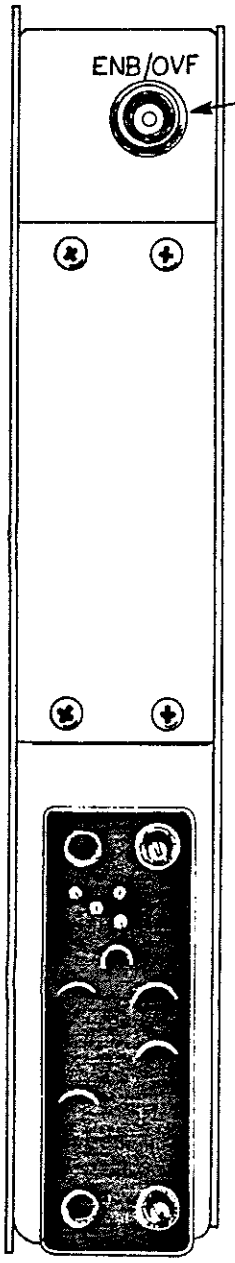


Figure 3.1
Front Panel

3.2 REAR PANEL



ENB/OVF
Jumper Selectable
ENABLE - Input/Output connector for the Enable signal. Low logic level output indicates that counting is enabled. Low logic level input enables counting cycle.
OVERFLOW
Provides a positive logic pulse when the 8×10^7 counter bit resets in channel A.

Figure 3.2
Rear Panel

3.3 JUMPER OPTIONS

The Model 2072A jumpers are defined as follows:

Jumper	Function
A*	Allows the GATE B signal to enable counter B
B	Prevents the GATE B signal from disabling counter B
C*	Allows the GATE A signal to enable counter A
D	Prevents the GATE A signal from disabling counter A
G*	Allows the logic to reset channel A
H	Prevents the logic from resetting channel A
J*	Channel A provides OVERFLOW signal
K	Channel B provides OVERFLOW signal
Z	Selects falling edge of ENABLE input pulse to start count
W*	Selects dc level of ENABLE to start and store count
R*	Connects front panel GATE A to GATE A function
S	Connects front panel GATE A to ENABLE function
EE	Selects rear panel ENABLE function
FF*	Selects rear panel OVERFLOW function
AP*	Selects positive A input
AN	Selects negative A input
BP*	Selects positive B input
BN	Selects negative B input

*Indicates factory set position.

1. To disable logic reset of channel A and use manual reset only:
   move jumper G to position H

2. To disable the gate signal to channel A:
   move jumper C to position D

3. To disable the gate signal to channel B:
   move jumper A to position B

4. To change the Overflow output from channel A to channel B:
   move jumper J to position K

5. To change rear panel OVERFLOW to ENABLE:
   move jumper FF to position EE

6. To change A INput from positive to negative (NIM) input:
   move jumper AP to position AN

7. To change B INput from positive to negative (NIM) input:
   move jumper BP to position BN

8. To allow the falling edge of the ENABLE input pulse to place the Unit in count:
   move diode W to position Z;
   be sure to orient the diode with the band toward the bottom of the board

9. To allow the front panel GATE A input to perform ENABLE function:
   move jumper R to position S

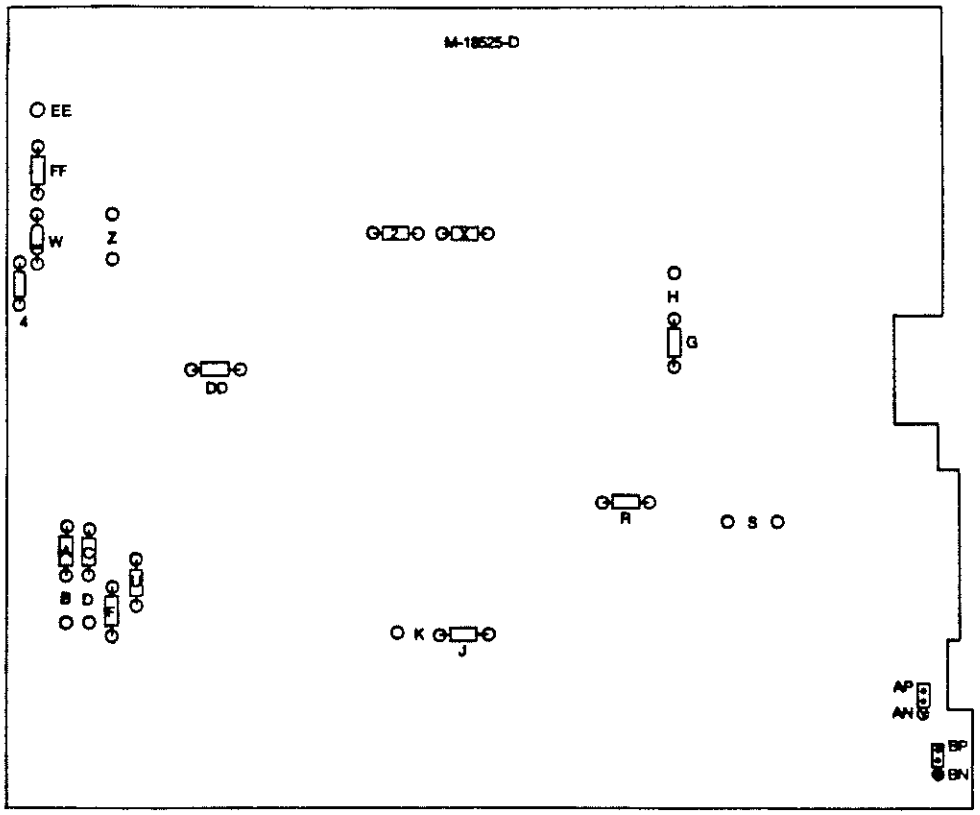


Figure 3.3
Internal Jumpers

Section 4. Operation

The Model 2072A Dual Counter is a two-channel event counter. The unit will accept positive voltage logic pulses or negative current pulses (jumper selectable). Positive inputs are normally clamped to + 5 V and will see a nominal input impedance of 1k ohms. Negative inputs see a nominal 50 ohm input impedance.

4.1 DISPLAY ANNUNCIATORS

The liquid crystal display panel has, in addition to numerals to display counter contents, five annunciators which describe the display's readout and the dynamic state of the unit.

X100 Shows that the six most significant digits are being displayed.

OF Shows that the displayed channel has overflowed and is counting up from zero again.

CNT Shows that the selected channel is displaying counts. Blinks when the channel is active.

A/B Shows which channel's contents are being displayed.

4.2 COUNTING

The Model 2072A may be used as a single counter or as a two-channel counter. To use it as a single counter, connect the incoming counts either to A IN or to B IN, and set the DISPLAY SELECT switch to that channel.

To use the Model 2072A as a dual counter, connect the two sources of incoming counts to both A IN and B IN. Display of either channel's contents depends on the position of the DISPLAY SELECT switch, which may be changed at any time.

Pressing the START/STOP switch to START will start the counting, which will continue until the switch is pressed to STOP or until an external stop command is received from one of the I/O options. The unit can also be started and stopped remotely by using the ENABLE connector. Refer to Section 4.6.

4.3 RESET

At any time, even during a count cycle, pressing the RESET button will clear both counters to zero. If a counting cycle is in progress, it will resume as soon as the RESET button is released.

By changing an internal jumper, channel A automatic reset can be inhibited. In this mode, channel A can be reset only by pressing the RESET button. See Section 3.3.1.

The RESET button also functions as a display check. When the button is pressed, the display will show all "eights." Therefore, holding the button down will allow the operator to verify that the display is functioning correctly.

4.4 SYSTEM OPERATION

Several of the 2071A and 2072A counting modules can be configured in a Master/Slave relationship by connecting their ENABLE connectors in parallel with 93 ohm coaxial cable (type RG-62), using "tee" connectors between the cable segments.

When the system is connected in this way, pressing START on one unit will start all units together.

The Master unit in the system is the one whose START button has been pressed, all other units are Slaves. Note that in this mode, the Slave presets are disabled. The Master unit's preset will control the entire system. Pressing STOP on the Master will stop all units together.

The input/output options may also be used to set the system up in the Master/Slave mode. See Sections 5 and 6 for details.

4.5 GATE A AND B

The GATE functions are available on the front panel GATE A and B connectors.

The GATE connectors accept positive logic pulses or a dc level to enable counting in either channel. Internal jumpers may be moved to disable the function for either channel or both channels. See Sections 3.3.2 and 3.3.3.

A logic high signal (+ 4 to + 5 V) or an open input will enable counting; a logic low signal (0 to + 0.8 V) will disable counting.

4.6 ENABLE

The ENABLE function is available on both the front and rear panel. The rear panel ENB/OVF (ENABLE or OVERFLOW) connector is factory set to the OVERFLOW position. To select rear panel ENABLE function, see Section 3.3.5.

The ENABLE connector provides a logic low output (0 to 0.8 V) when the unit is enabled for counting. This output can be used to signal another unit that the Model 2072A is active. For instance, when using the Model 2072A as the Master unit in the Master/Slave System outlined in Section 4.4.

The ENABLE connector can also receive a logic low pulse to enable the Model 2072A for counting. For instance, as a Slave unit in the Master/Slave System.

To increase the Enable line's flexibility, an internal jumper (W) has been provided. If this jumper is moved to the Z position (see Section 3.3.8), the falling edge of an input pulse on the ENABLE connector will start the unit's counting cycle.

When the unit is started in this way, it is the Master unit in the system. The Enable line will be held low by this unit until its preset is reached, thus enabling all other units in the system.

If the Model 207x-02 Daisy Chain Interface is installed, it will not be necessary to use the Enable line. The Interface has all necessary signals to start and stop the unit.

If the Model 207x-01 GPIB Interface is installed, the Enable line will be used if the entire system is to start and stop at the same time. If the GPIB Controller is to address each unit separately, the Enable line will be used only if each individually addressed unit is the Master unit in separate sub-systems.

An internal jumper can be moved to change the front panel GATE A function to ENABLE. See Section 3.3.9.

4.7 OVERFLOW
The OVERFLOW function is available at the rear panel ENB/OVF (ENABLE or OVERFLOW) connector which is factory set to the OVERFLOW position. To select the rear panel ENABLE function, see Section 3.3.7.

The rear panel OVERFLOW connector provides a positive logic pulse every time that channel A exceeds its count capacity (10^8 counts). This signal can be connected to the input of another counter to extend the counting capacity of the system.

The OVERFLOW signal can be connected to the B INput, instead of another counter, to extend the counting capacity of the system.

An internal jumper can be changed to allow the overflow of channel B to generate the OVERFLOW signal. See Section 3.3.4.

Section 5.
Daisy Chain Interface

The Model 207x-02 Daisy Chain Interface option provides both data input/output and system control. It is compatible with all existing Canberra Daisy Chain Systems.

The CONTROL IN and CONTROL OUT connectors present all Bus commands, with the exception of the Print clock, in parallel to all units in the system. The Print clock is presented serially to one unit at a time.

Since the Model 2072A is an eight-digit counter and the Daisy Chain System is capable of recording only six digits, a switch has been included on the Interface Board to select output of either the six most significant digits ($10^2 - 10^7$) or the six least significant digits ($10^0 - 10^5$). Refer to Figure 5.1 for switch location.

The nature of the data collection being performed will define which six digits to include in the data output. The unit is shipped with the switch in the six least significant digits ($10^0 - 10^5$) position.

5.1 SYSTEM SETUP
A system of up to 50 data input modules and one scanner are connected with Model C-1404 cables. One 60 cm (two foot) cable is included with each Model 207x-02.

The CONTROL OUT connector of each unit is connected to the CONTROL IN connector of the next unit in the system. The last unit in the system is connected back to the scanner.

The system Master unit is defined as the one on which the START control is pressed. All other units are then Slave units.

When the Master unit is started, it generates a System Start command on the Daisy Chain Bus, which starts all Slave units at the same time.

When any unit reaches its preset, it stops and generates a System Stop command on the Bus. All units will stop at the same time.

With a 2071A in the system set to the SINGLE count mode, the system will run through one data collection cycle and stop when preset is reached.

With a 2071A in the system set to the RECYCLE count mode, the system will start, stop when any unit reaches its preset, pause ten seconds or 100 microseconds (jumper selectable in the 2071A), clear all counters, and start counting again.

5.2 PRINTING SYSTEM
If a Model 2088 Communications Interface (RS232), or a Model 2089 Serial Scanner-Printer is connected in the system, the data collected by each unit can be printed out. A Model 9182 EIA to 20 mA Current Loop Adapter can be connected to the 2088 for 20 mA current loop operation.

Standard with the NIM Daisy Chain option is a readout buffer. By taking advantage of the buffer circuitry, system dead time can be reduced. In a Recycle Mode, the buffer allows the unit to be placed back into the counting mode after the data has been latched into the readout buffer. After 10 seconds or 100 microseconds, jumper selectable on a master 2071A, counting resumes and readout begins. During the readout time, the display will not be updated, but correct counting will go on. As with most buffers, counting time must be longer than readout time.

The first unit in the system to print out will be the one connected to the Scanner's CONTROL OUT connector. The second unit to print out will be the one connected to the first unit. The last unit to print out will be the one connected to the Scanner's CONTROL IN connector.

5.3 COMPUTER CONTROL

The Model 2088 Communications Interface can be used to allow a computer to control the system. Refer to the Model 2088's manual for details on computer system operation.

5.4 DAISY CHAIN JUMPER OPTIONS

The Daisy Chain option board has four jumpers which will allow the user to tailor the option for specific applications. Three of these jumpers are 4.7k ohm resistors; the fourth is a 2.7 ohm resistor. Refer to Figure 5.1 for jumper locations.

1. Jumper A allows the Enable pulse's rising edge or the Model 2072A's control logic to generate the Daisy Chain Bus STOP command.

   In the B position, this unit will not generate the STOP command.

2. Jumper C allows the Enable pulse's falling edge or the Model 2072A's control logic to generate the Daisy Chain Bus START command.

   In the D position, this unit will not generate the START.

3. Jumper E allows the Enable pulse's falling edge or the Model 2072A's control logic to generate the Daisy Chain Bus RESET command.

   In the F position, this unit will not generate the RESET command.

4. Jumper G allows the Model 2072A's front panel RESET control to generate the Daisy Chain Bus RESET command.

   In the H position, manual Reset will not generate the RESET command.

Please be aware that these jumpers do not need to be changed to make this unit a Slave unit. Slave status is normally defined by system operation.

If any or all of these jumpers were to be changed to their optional positions, this unit would be permanently defined as a Slave unit. It would never become a system Master unit until the jumpers were changed back to their usual setting.

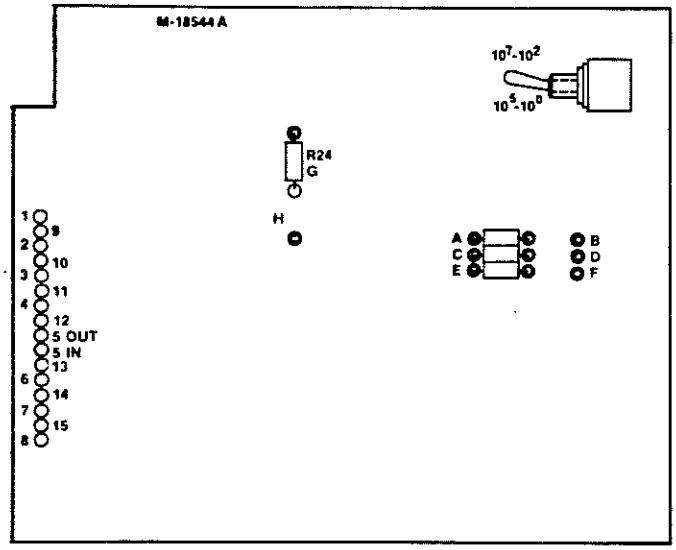
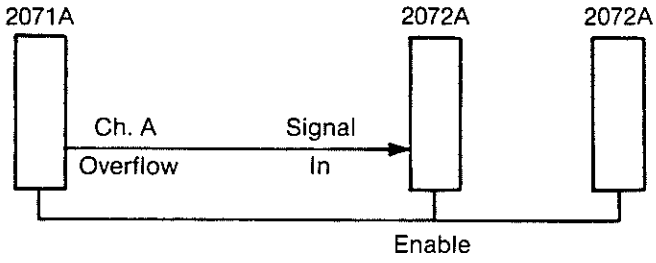


Figure 5.1
Daisy Chain Option Controls

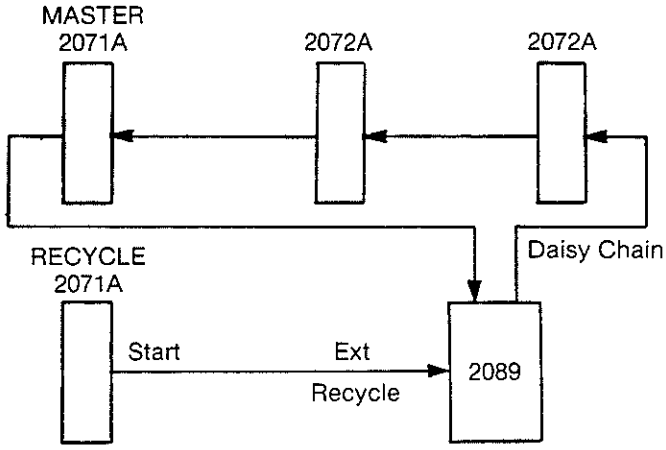
5.5 TYPICAL SYSTEMS

The following figures show some the possible system setups.

1. Multi-input system with preset time and ability to count overflow from channel A of the 2071A.

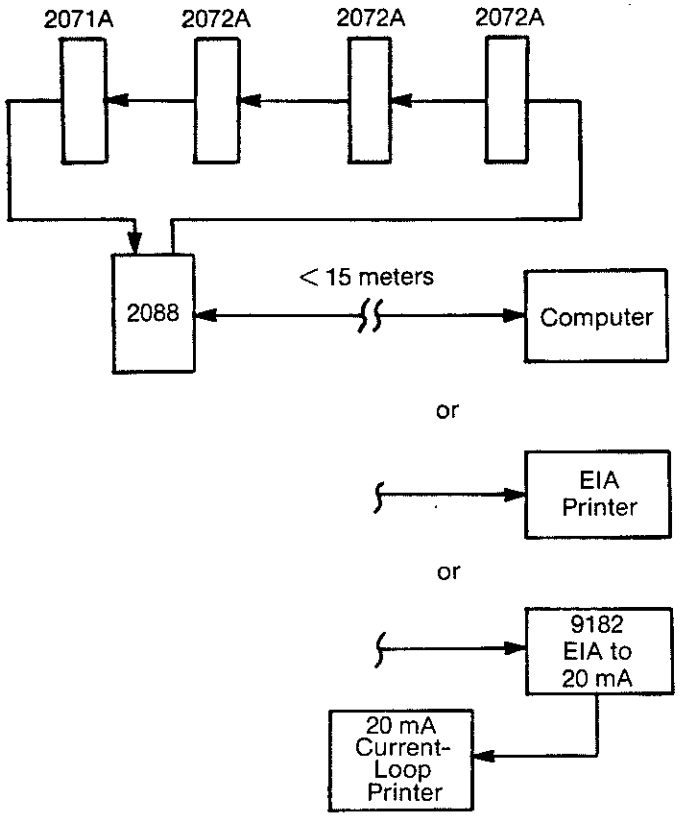


2. Multi-input 100 MHz Daisy Chain Printing System - preset controlled by master 2071A, recycle time controlled by 2071A. Printout from 2089 printer lists preset time and contents of 5 counters.



Note: The Model 2071A will require a factory modification (SERF) in order to operate with the Model 2089 External Recycle.

3. Multi-input 100 MHz Daisy Chain system with individual preset time for the 2071A counter. Slaves must reach preset before master. For this system, slaves are defined by changing the -02 option's internal jumpers (See Section 5.4).The 2072A counters are controlled by the master.



5.6 USING THE MODEL 1488 SCANNER

If a Model 1488 Scanner is to be used instead of the Model 2088, the 1488 PRINT MODE switch must be set to PROMPT.

In the DELAYED mode, the HOLD command is not normally asserted until after the TTY motor-start time out, which will not allow proper data buffering.

For proper operation in the DELAYED mode, open the 1488 and look for a 10 ohm resistor soldered to points A-B (refer to schematic B-12177). Unsolder the resistor from points A-B and solder it to points A-C. This will cause prompt generation of the HOLD command on receipt of the Daisy Chain's STOP pulse.

The 1488's FORMAT switch must be set to LINE. Setting the switch to CONTINUOUS will cause incorrect data to be read out.

5.7 FIELD INSTALLATION OF THE DAISY CHAIN OPTION

The Daisy Chain Interface option consists of: four lockwashers, 8 Phillips-head screws, the rear panel control connector plate, and the interface board.

To install the option, first remove both side covers, each of which is held in place by five Phillips-head screws. Then:

1. Carefully place the interface board in the unit so that the line of small circular connectors is at the rear of the board.

2. With the interface board's four standoffs lined up with the four holes in the motherboard, press the board gently down to mate the interboard connectors.

   The interface board should mate smoothly with the unit's connector. If any resistance is felt, the connector is not properly aligned; lift the interface board up a little and realign the four standoffs with the mounting holes before pressing down again.

3. Fasten the interface board to the motherboard with four screws and lockwashers.

4. Mount the control connector plate on the rear panel with the four remaining screws.

5. Carefully align the ribbon cable's pins with the sockets of J4 at the rear of the interface board.

6. Press the cable's pins firmly down into the connectors until the cable is flush with the tops of the connectors.

7. Place S1, the six-digit select switch, in the desired position.

8. Before replacing the side covers, check the installation for proper operation.

5.8 CONTROL IN/OUT CONNECTORS

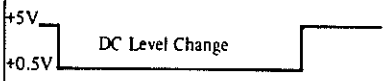
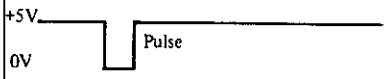
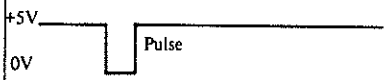
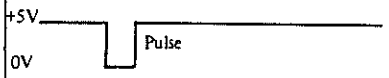
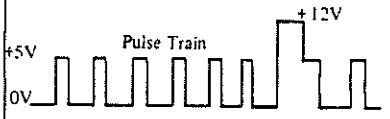
PIN No.	FUNCTION	SIGNAL DESCRIPTION
1	BCD Data "1"	Logic 1 = +4V, Logic 0 = 0V
2	BCD Data "2"	Logic 1 = +4V, Logic 0 = 0V
3	BCD Data "4"	Logic 1 = +4V, Logic 0 = 0V
4	BCD Data "8"	Logic 1 = +4V, Logic 0 = 0V
5*	Print Clock	
6	System Hold	
7	System Stop	
8	System Start	
9	System Reset	
10	Display BCD "1"	Logic 1 = 0V, Logic 0 = +4V
11	Display BCD "2"	Logic 1 = 0V, Logic 0 = +4V
12	Display BCD "4"	Logic 1 = 0V, Logic 0 = +4V
13	Display BCD "8"	Logic 1 = 0V, Logic 0 = +4V
14	Display Clock	
15	Ground	

Figure 5.2
Control In/Out Connector Wiring

NOTES:
All data and control lines except Print Clock line (*pin 5*) are inter-wired directly between corresponding pins of the CONTROL IN CONTROL OUT connectors.

The Print Clock pulse *train* from the Data Scanner will appear on pin 5 of the CONTROL OUT connector after module has finished printing its data contents.

The signals on pins 10 through 14 are not used by this unit.

Section 6.
Interaction of Model 2072A With the GPIB

6.1 GENERAL DESCRIPTION OF GPIB

The General Purpose Interface Bus is a link or network by which system components communicate with each other. Each system participant performs at least one of three roles: Controller, Talker, or Listener.

A Controller manages bus communications primarily by directing or commanding which devices are to send data to other devices (Talker), or receive data from other devices (Listener) during an operational sequence. A Controller may also be interrupted or it may command specific action between devices.

The GPIB consists of 16 lines which are grouped into three sets according to function; there are 8 data lines, 3 control lines, and 5 general management lines. The 8 data lines carry ASCII characters (bit parallel) asynchronously; the control lines provide a data transfer handshake compatible with both slow and fast devices. The bus management lines allow initialization, interrupts, and special controls.

6.2 GPIB SWITCHES

The eight-section DIP switch on the option board is accessible through the hole in the unit's side cover. The switches should be set to the desired positions before putting the unit in a NIM Bin. Refer to Figure 6.1.

The first five switches, counting from the top, are used to set the unit's GPIB address. Each switch is labeled with its value and with ZERO and ONE. The address is the sum of all switches that are in the one position. An address of 31 (all switches in the ONE position) is illegal; it is reserved for the GPIB command UNTALK.

The sixth switch is labeled TALK ONLY. Refer to Section 6.3 for its uses.

The seventh switch is labeled RECYCLE. In the ON position, the unit will clear after readout and start counting again. In the OFF position, the unit is in the single cycle mode.

The eighth switch is labeled FF/CR. In the FF position, the message unit delimiter is sent out as an ASCII Form Feed. In the CR position, the delimiter is sent out as a Carriage Return. The choice of delimiter depends on the peripheral device being used.

6.3 SYSTEMS WITHOUT A CONTROLLER

The Model 2072A can operate in the Talk Only ON mode, which is used when data from a single module is to be passed directly to a single peripheral Listener device, such as a GPIB Printer. In this case a Controller is not required.

In Talk Only ON mode, the 2072A will transmit its data to the listener as soon as 2072A data acquisition is stopped (by front panel STOP or external ENABLE).

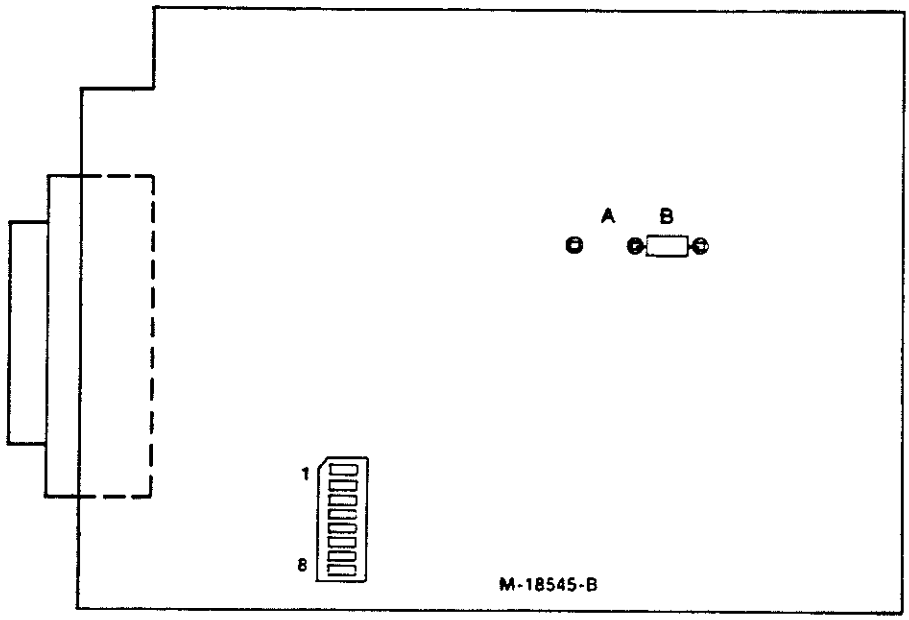


Figure 6.1
GPIB Option Controls

6.4 INTERACTION WITH A CONTROLLER

Communication with a Controller requires 207x-01's TALK ONLY switch to be off and REN (Remote Enable) asserted. The first requisite is for the Controller to cause the 2072A to be placed in its Remote mode. It does this by transmitting on the GPIB, MTA, (My Talk Address) or MLA (My Listen Address), with ATN (Attention) asserted. MTA or MLA must agree with the five-bit address setting on the 2072A. The following MTA or MLA would be sent if the address setting was 5.

	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
MTA	1	0	0	0	1	0	1
MLA	0	1	0	0	1	0	1

If MLA is sent, the 2072A does not respond further than placing itself into the Remote mode. Once in the Remote mode, the unit is able to generate an SRQ (Service Request) or respond to a DC (Device Clear). If MTA is sent, the unit goes into its Remote mode and transmits all of its data (19 bytes).

A typical sequence would begin with the operator pressing START on a 2071A that is connected to the GPIB. After reaching a preset, the 2071A will generate SRQ. The Controller would then, via a Serial Poll, determine the device(s) requiring readout and send the proper MTA to read the data. If the module is in the Recycle mode (switch on GPIB interface set to Recycle), the counters will be reset after readout and the counting cycle will begin again.

The 2072A will generate SRQs if it is stopped with the front panel START/STOP control, the ENABLE line, or upon receipt of a DEVICE CLEAR from the controller.

The time required to read data from a Model 2072A is determined by the sum of the response times of the Computer/Controller and 2072A. The 2072A responds to each query or handshake request within seven microseconds. This means the 2072A requires a maximum of 14 microseconds for each byte outputted. The 19-byte readout consumes 266 microseconds of 2072A synchronizing time. A readout to one Controller was measured at 12.5 milliseconds. This equates to 644 microseconds to accept data and generate handshake responses per byte, or a ratio of Controller to 2072A of 46 to 1. It is apparent that the Controller is the major contributor to readout time and therefore no readout times can be provided for the 2072A as an individual instrument.

Some additional capabilities are:

a. Controller Start

Since modules are independent, the Controller can start each module by performing a READ DATA Interchange (see Section 7.8). With a counter stopped and in a GPIB recycle mode, the completion of a READ DATA Interchange will cause it to clear and start counting. The controller can individually address each module for this sequence.

b. Controller Stop

The Controller can send a Universal DEVICE CLEAR out on the bus, and all modules will stop counting. Individual modules cannot be addressed with this command, and it will not clear the modules, only stop them. If internal jumper B is moved to A, the module will ignore the DEVICE CLEAR command (see Figure 6.1).

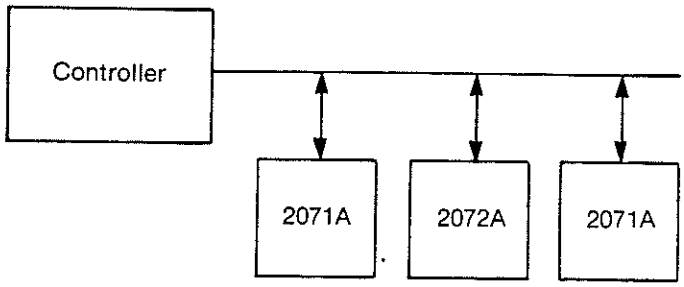
c. Read Out While Counting

The Controller can read out each individual 2071A or 2072A while it is counting by performing a READ DATA Interchange (see Section 7.8). In this case the module will be read out and will not clear, but continue counting. A point to remember here is that a module will clear itself only if it is restarted by:

1. A manual front panel START.
2. A manual front panel RESET.
3. An ENABLE signal input.
4. Being in a front panel RECYCLE mode and stopped either by reaching preset or by receiving a Device Clear from the Controller.
5. Being in a GPIB Recycle mode, stopped by reaching preset or receiving a Device Clear from the Controller, then read out by a READ DATA Interchange.

6.5 THREE COMMON METHODS OF OPERATION:

A. Controller completely controls modules.



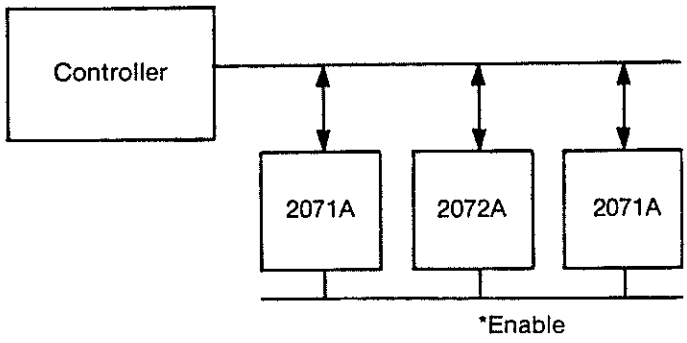
Sequence:

1. Controller performs READ DATA Interchange to start the modules. Each one must be addressed individually by the Controller. Thus, in this case, a simultaneous start is not possible. Data read out the first time is information left by previous operations.

2. Controller sends a DEVICE CLEAR, when desired, to stop all counters. Individual addressing is not possible with this command. All counters will simultaneously stop.

3. Controller again addresses each module with a READ DATA Interchange. Since they are in the Recycle mode (they would not have started in the first step if they weren't) each one clears, and restarts after reading out.

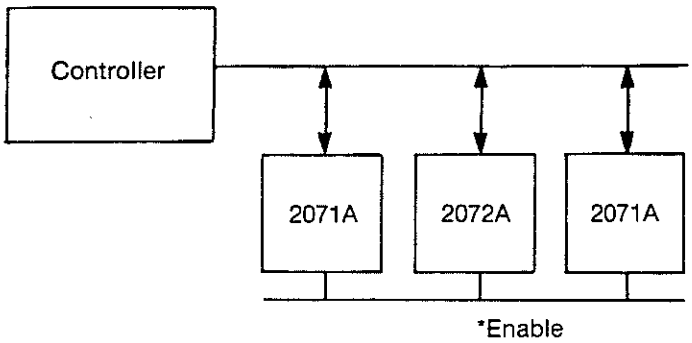
B. Controller acts only as a readout device.



Sequence:

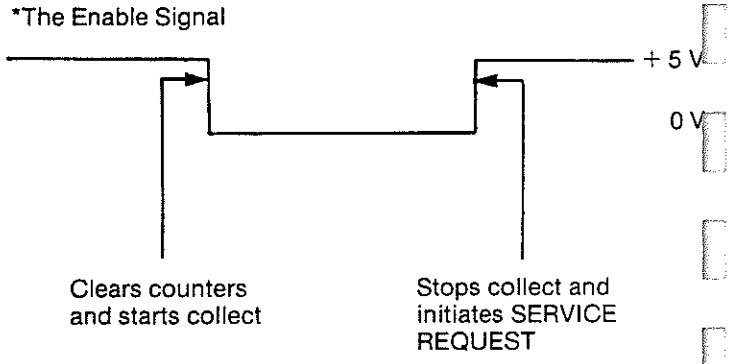
1. ENABLE input/outputs on all modules are connected.
2. The START switch on one 2071A is pushed (this defines it as the Master).
3. All modules are stopped when the master reaches its preset.
4. Each module sends a SERVICE REQUEST when it stops if it was first commanded to REMOTE by the Controller.
5. The Controller addresses each module and reads it out.
6. If the Master is in the front panel RECYCLE mode, upon being read out it will enable the system to start counting again. All modules will have been cleared by the leading edge of the ENABLE signal. Normally the Master would be interrogated last so that it does not start the system until all other units have been read out.

C. Controller initiates simultaneous start by addressing the master module.



Sequence:

1. ENABLE input/outputs on all modules are connected.
2. Controller addresses first 2071A and reads it out. This defines it as the Master. Because it is in the GPIB Recycle mode it reads out, clears, and starts collecting. Since the ENABLE ports are connected, the other 2071A and 2072A modules clear and simultaneously start collecting. The Single/Recycle switch on each of their GPIB interface cards and front panel must be in the SINGLE mode.
3. When the preset on the Master 2071A is reached, it stops all modules, and each one generates a service request on the GPIB Bus. The Controller now interrogates each module. It should address the Master 2071A last, since this module is in the recycle mode and would start the system again once it is read out.



The modules on which the START switch is not pushed will ignore their presets and be controlled by the ENABLE signal. The Master module is defined as the module that has been started first, either manually or by being addressed from the Controller. Its preset will determine the presets for all other 2071As and 2072As.

6.6 FIELD INSTALLATION OF THE GPIB OPTION

The GPIB Interface option consists of: four lockwashers, 8 Phillips-head screws, a rear panel cover plate marked J102, and the interface board.

To install the option, first remove both side covers, each of which is held in place by five Phillips-head screws. Then:

1. Carefully place the interface board in the unit so that the large connector at the rear of the board is flush with the rear panel.
2. With the interface board's four standoffs lined up with the holes in the motherboard, press the board gently down to mate the interboard connectors.

   The interface board should mate smoothly with the unit's connector. If any resistance is felt, the connector is not properly aligned; lift the interface up a little and realign the four standoffs with the mounting holes before pressing down again.
3. Fasten the interface board to the motherboard with four screws and lockwashers.
4. Place the J102 cover plate on the unit's rear panel and fasten it in place with the remaining four screws.
5. Before replacing the side covers, check the installation for proper operation.

6.7 CONNECTOR

A 24-pin standard GPIB connector (J102) is mounted on the rear panel. It carries the following signals:

Pin	Signal	Description
1	DIO1	Data I/O 1
2	DIO2	Data I/O 2
3	DIO3	Data I/O 3
4	DIO4	Data I/O 4
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready for Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	Shield	To earth ground
13	DIO5	Data I/O 5
14	DIO6	Data I/O 6
15	DIO7	Data I/O 7
16	DIO8	Data I/O 8
17	REN	Remote Enable
18	Twisted pair with pin 6	
19	Twisted pair with pin 7	
20	Twisted pair with pin 8	
21	Twisted pair with pin 9	
22	Twisted pair with pin 10	
23	Twisted pair with pin 11	
24	Signal Ground	

Figure 6.2
GPIB Connector Wiring

All GPIB signals are negative-true TTL compatible:
True = 0 to 0.4 V;
False = 2.5 to 5 V.

Section 7.
Theory of Operation

The Model 2072A includes two identical eight-decade counter channels, a six-decade liquid crystal display, optional readout to a Canberra Daisy Chain Scanner, to a GPIB (IEEE 488) system, or to an EIA Interface, suitable control logic, and the power supply.

7.1 EIGHT DECADE COUNTING CHANNEL

Each of the identical counting channels has an input circuit which accepts positive voltage or negative current logic pulses on the same input connector (jumper selectable). Negative current-pulses see a 50 ohm impedance while the positive voltage-pulses see a nominal 1k ohm impedance.

With the A input jumper in the AP position, positive voltage signals are fed to the inverting input (pin 3) of comparator A58. A voltage divider consisting of R37, R42, and R43 along with clamping diodes D11 and D12 protect A58 from positive or negative over-voltages. When the positive input signal exceeds the threshold level set at A58-2 by R35 and front panel DISC A (RV 2), A58-7 goes from ≈ 5 V to ground. This signal is fed through D10 to A56. Double counting with slow rise times is prevented by the feedback network consisting of R56, C20, and C21.

With the A Input jumper in the AN position, negative current input pulses are received by the 47 ohm terminating resistor R81 which develops a voltage drop fed to the base of Q8. When the voltage drop exceeds the threshold voltage set on Q9 base by R38 and R39, Q8 turns off and Q9 turns on. This brings Q9 collector and A56 input from ≈ 2.5 V to ground. Components D35, D34, R86 and D24 protect Q8 and Q9 from positive or negative overvoltages.

Operation of Channel B is identical to that of channel A.

Multiplexing counts or external time ticks to the counter is carried out by A56 (74F00). Two gates are used by each counting channel. The first decade, which is required to count at 100 MHz, is a 74S196. The second, counting at 10 MHz maximum, is half of a 74LS390. The remaining six decades reside in a LS7031. The 7031 contains six counting decades, latches, and multiplexing logic to read out the six decades plus the data of the two decades ahead. Additionally, it contains logic to recognize leading zeroes and overflow conditions. Thus, in a simple 40-pin IC, a single 14-pin IC, plus half of 16-pin IC, we have an eight decade counter with readout multiplexing.

A counting sequence is initiated with a reset pulse setting all eight decades to zero. External events are gated to the clock input of the 74S196. The eight bit of the 74S196 clocks the 74LS390, and in turn the eight bit of the 74LS390 clocks the 7031 input decade.

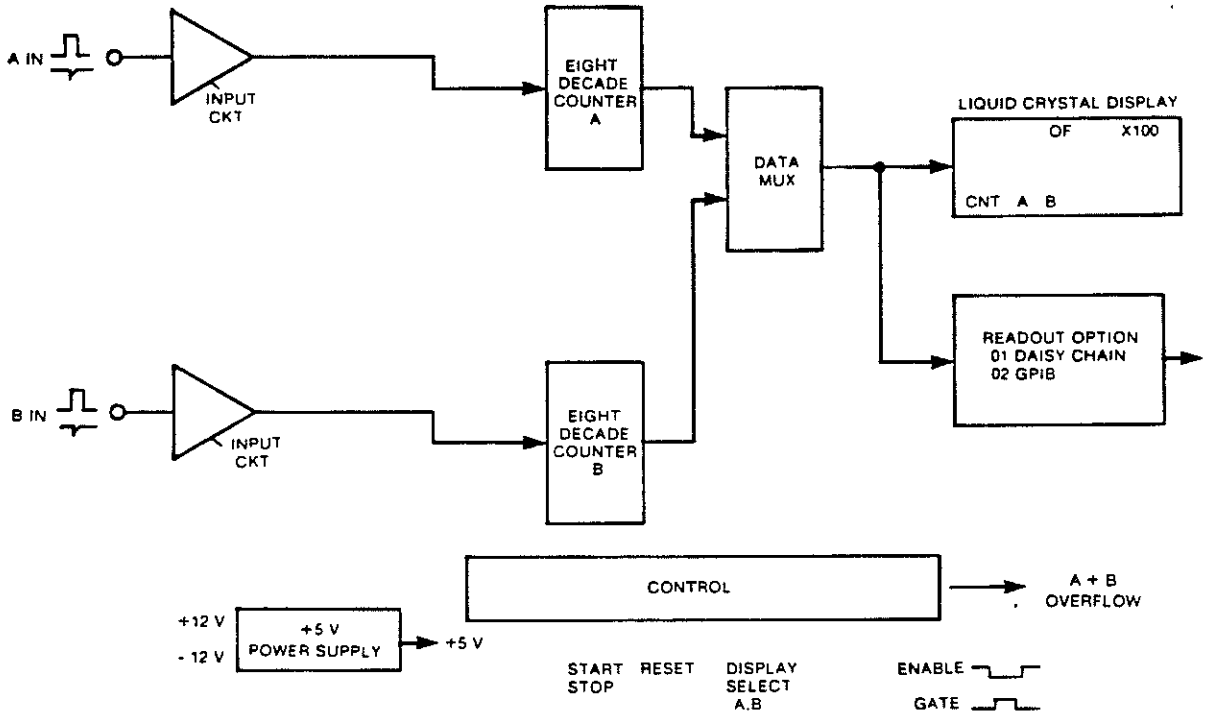


Figure 7.1
Model 2072A Block Diagram

To read the contents for display or read out the counter, data is transferred to latches within the 7031 by means of the Load Latch pulse. The next part of the sequence is to generate a Scan Reset which places the most significant digit (in BCD format) on the four data output lines. As each succeeding digit is required, a Scan Clock pulse is applied to the 7031 which places the next less significant digit on the data output lines. Because the display consists of six digits and the counter capacity is eight, at the time the 10^5 counter decade 8 bit resets, A29 is toggled to the one state. The signal out of the 7031 "D6" is this bit (8×10^5), and the output of A29 is called "X100". X100 true causes the X100 display annunciator to turn on and causes a two-digit shift in the data displayed.

The BCD data out of the 7031 is immediately passed through A53, a quad Exclusive-NOR gate. Its function is to either invert or not invert the data. The internal leading zero logic determines this and Blank Out is the signal. The utilization of this function is by the LCD display drivers. When they see a binary 15 they respond by displaying a blank. A BCD zero out of the 7031, if it is an insignificant (leading) zero, is then converted to binary 15 by inversion and is blanked on the display.

7.2 SIX DECADE LIQUID CRYSTAL DISPLAY

The six-decade liquid crystal display (LCD) has each digit driven by a seven-segment LCD driver IC. With this scheme, all digits are driven in parallel (that is, all ON segments are turned on at the same time). The requirement to turn a segment on is that an rms voltage be applied between the backplane and particular segment that is greater than the ON threshold for the LCD. This is accomplished by applying a square wave to the backplane and another to each segment. In-phase square waves result in zero rms (OFF) and 180° out-of-phase results in an rms of 5 V (ON). The type 4056 driver consists of a four-bit latch, a seven-segment decoder and an exclusive-OR array to select the proper phase of the signal applied to each segment.

The same clock (A32) used to strobe the data from the 7031s also provides the approximately 25 Hz square-wave display clock. In addition to the six digits, any of eight annunciators can be shown to describe the data being displayed. "CNT" is displayed when counts from an external source are selected for display. Because the data source may be from the A channel or B channel, A and B annunciators are provided. When the magnitude of the number exceeds six digits (10^5-1) a X100 annunciator is enabled and the displayed data is shifted so that the display is 10^7 to 10^2, the six most significant digits. It should be noted that losing two digits means a display error ranging from 0.01% to zero. GPIB readout data includes the full eight digits. The remaining annunciator "OF" (overflow) turns on when the counter reaches 10^8 counts and remains on until data is reset.

The annunciators are driven by three 4054 four-signal segment drivers. These include latches and exclusive-OR arrays to develop the display-signal phasing required. Combinatorial logic consisting of gates A5, A15, A16, A17, A25, A26, A27, A28 determine which annunciators are on. Additionally A1, a slow oscillator, causes CNT to blink during active counting.

The circuit to obtain data from each of the 7031s is essentially the same for readout or display. The selection of data from either the A channel or B channel is accomplished by multiplexer A37, whose data selection is controlled by the front panel Display Select switch and A23. A23 is needed so that the data can be changed remotely in readout, allowing readout of both channels.

An oscillator (A32) running at about 50 Hz (divided by the other half of A23, to 25 Hz for the display clock) supplies the 7031 scan clock and an 8-stage Johnson counter (A8). The eight outputs of the Johnson counter are synchronous with the 7031 Digit Strobes and hence, the 7031 output data. The Johnson counter outputs strobe the data into the display LCD drivers. Also the first (TP11) or third (TP12) strobe generates a scan reset. This maintains synchronization and generates the X100 display data shift. Scan reset with the first strobe allows a display of $10^5 \rightarrow 10^0$. Scan reset with the third strobe allows a display of X100 or $10^7 \rightarrow 10^2$. This is accomplished by sending the first and third strobe pulses through A38, a dual multiplexer controlled by X100 signals from the A counter and B counter. In readout, the A32 oscillator is replaced by read clocks from the readout option. This is accomplished by half of A12.

7.3 CONTROL

The block diagram area labeled Control provides interactive control with all the blocks on the diagram. The prime control capabilities are to place the unit into the count enabled mode, determine which counter counts external events, and various jumper controlled options.

The signal ENABLE, brought to a front panel or rear panel BNC connector, is the count enable function. A low is the true state, indicating counting is enabled. This is a bi-directional signal path which allows an external master unit to enable both channels for an externally determined time. The logic sequences in this mode are that once the ENABLE level has been pulled low by the master, a 10 microsecond reset pulse is generated (TP5) and sent to both A and B channels. This means a 10 microsecond dead time is incurred at the beginning of a measurement period.

A Model 2072A may be either a master or slave with no jumper or control changes. Determination of master or slave status is dependent on whether or not the START switch has been pressed. The START switch causes one-half of A3 to be set. It, in turn, drives the ENABLE line low through A14-11. At this point any other units receiving the ENABLE signal are enabled to count as slaves. After the 10 microsecond reset period has elapsed, both counting channels and the preset channel are allowed to accumulate data.

The presence of a Daisy Chain option results in a slightly different concept of master and slave. This option provides interconnected START, STOP, and RESET signals to all units in the system. The ENABLE signal is not used (not connected between units). In this case the unit whose START switch was pressed (not necessarily the master unit) causes the Daisy Chain START pulse to toggle A3 to the one state via signal ST5 in each module.

Termination of counting occurs when the master reaches preset, or when its STOP switch is pressed. The master unit then generates the STOP signal to the remainder of the system, terminating the experiment.

The GATE input signals normally control counting in channel A or channel B. Pulling the signal low, from an external source, will prevent any accumulation while held low. If the particular experiment requires one or the other channel only to be gated, internal jumpers (plug-in 2.7 ohm resistors) may be changed as follows. Jumper A allows gating to channel B. Remove A, install in B and channel B is not affected by the GATE signal. Jumper C allows gating to channel A. Remove C, install D and channel A is not affected by the GATE signal.

Manual data reset is accomplished by pressing the front panel RESET button. Data will be held reset while the button is pressed. To account for switch bounce, a final 10 microsecond reset is applied on release by A24 (pin 7). The application where manual reset is necessary is when jumper G is removed and jumper H installed. Now channel A is not reset with channel B, but only by the manual RESET button, allowing the A data word to accumulate continuously during succeeding count periods.

7.4 POWER SUPPLY

An inverter concept is applied to supply the five volts used by the module logic. Power supplied by the bin +12 V and −12 V buses is converted to ac by the oscillator made up of T1, Q3, Q4, and C17. Oscillation is in the 60 to 70 kHz range. The output of the secondary (T1 terminals 1, 2, and 3) is full-wave rectified by D17 and D18 providing the + 5 V for the logic. T2 supplies feedback to the input of T1 (terminal 5), proportional to the output loading and ripple. As the load increases (and the ripple), current is added to the normal T1 input so that the ripple is reduced, compensating for changes in loading.

Short circuit protection is provided by the circuit consisting of Q1, Q2, and their associated bias resistors and capacitors. Q2 is normally on, Q1 off. Q2 collector current passes through R57 to the bases of Q3 and Q4 where, in conjunction with the output phasing of T1 secondary (terminals 7 and 8), oscillation is maintained. When current through R61 is on the order of 200 mA, or more, sufficient voltage is dropped to turn Q1 on, causing Q2 to turn off, effectively stopping the oscillator. Neither Q3 nor Q4 can be on; causing the 5 V secondary to go to zero. At the same time the IR drop through R61 goes to zero allowing Q1 to turn off, Q2 to turn on and the supply to start up. As long as the current loading is excessive, the circuit will be protected by alternately turning off and on.

7.5 DAISY CHAIN OPTION

The Daisy Chain Option allows a user to choose a type of readout or no readout at all depending on his needs. This option provides the ability to interface with existing Canberra counting modules and scanners with one limitation. Old Canberra counters were all six-decade devices so that the readout capability is also six digits. The new eight-decade counter option includes a switch to select which six digits are to read out. The six least significant digits will be selected if the user knows his experiment will not result in more than 10^6-1 events counted. The six most significant digits can be selected when the experiment's results include numbers greater than 10^6. This readout selection results in loss of the 10^0 and 10^1 data digits and the attendant error in the data.

The option provides interconnection for five control signals, four data-bits, and ground on two 15-pin connectors.

The control signals and their functions are:

1. START: a bidirectional negative-going pulse swinging from + 5 V to ground with a minimum width of 1 μsec. The signal causes the counter it is applied to to initiate a counting cycle.

2. STOP: a bidirectional negative-going pulse going from + 5 V to ground with a minimum width of 1.5 μsec. The signal causes the counter it is applied to to terminate a counting cycle, and the scanner it is applied to to initiate a readout cycle.

3. RESET: a bidirectional negative-going pulse going from + 5 V to ground with a minimum width of 1 μsec. The signal causes the counter it is applied to to clear the data in its accumulators.

4. HOLD: a negative level at ground potential; + 5 V when false. This signal, generated by a scanner, disables the counter display-update function and enables the readout function.

5. PRINT CLOCK: a negative-going pulse going from + 5 V to ground with a minimum width of 3 μsec. The signal originates at the scanner module and is used to request each BCD data character. The counting module, after receiving its required number of print clocks, passes succeeding ones on to the next module. This signal is the only one not wired in parallel to both 15-pin control connectors.

The four data bits swing between + 5 V and ground, are high true, and have 1, 2, 4, 8 weights. The signals are diode-isolated from the bus so that any module can cause a true level regardless of the others.

Readout begins with the HOLD signal going true as a result of the STOP pulse generated by any module in the system. HOLD (level) generated by the system scanner, received by the Daisy Chain interface, causes the Read Clock Enable (RCE) level to be sent to the counter logic. This results in initialization of the logic placing the most significant data digit (10^7) on the data lines to the interface. After about 10 μsec to allow for data propagation through the cmos logic, the Readout flip-flop A7 is set (TP5 goes high). This removes the clear level applied to the Digit Counter (A4) and enables the fast clock (FCLK-A8) to advance the Digit Counter twice. This occurs before any Print Clocks arrive from the Scanner module. If the six least significant digits have been selected (10^5 - 10^0 switch position), the first two

fast clocks are also sent to the module as Read Clock (RCL) pulses. This advances the counter's output data from 10^7 to 10^5. When the six most significant digits are selected (10^7 to 10^2 switch position) the first two fast clocks are not sent to the module and the 10^7 data digit remains on the data lines to the option. When the scanner is ready for the first digit, a Print Clock pulse is sent. The leading edge loads the data into A3 (Data Latch). At the trailing edge, the next data digit is sent from the module to the option board. As the Scanner requires each additional digit, a Print Clock is sent requesting it, whereupon the leading edge loads the latch (A3) and the trailing edge causes the next digit data be presented to the latch. The seventh Print Clock causes gate A9c to be satisfied resetting the Digital Counter and the Data Latch.

The Fast Clock is allowed to generate two pulses placing the 10^5 data digit of the second data word on the data lines to the option. The two-bit Word Counter A2 keeps track of which word is being sent. After the second word has been sent, all succeeding Print Clocks are sent out to the next module via A1-8.

The bidirectional control signals START, STOP and RESET are received and/or generated as follows:

If the START switch is pressed, the ENABLE signal is sent to the option. An edge detector (A5a and A5b) generates a pulse to Q2 which generates the START pulse and sends it out to the remaining modules in the system. A START pulse sent from an external module is sent through the option to the main logic as ST5 where it toggles A3, setting the unit into the count mode.

The same edge-detector which causes the START pulse is also applied to Q3, which sends a RESET pulse to the other modules. Also pressing the front panel RESET button causes a RESET signal to be sent out to the external modules for as long as the button is pressed.

Pressing the STOP switch terminates the counting mode and causes a positive pulse (ECOL) to be sent to the option. It is applied to Q1, causing the STOP signal to be sent to the modules in the system. A received STOP signal, inverted twice, is sent directly to the main logic as STP where it clears A3, taking the unit out of the count mode.

Four jumpers have been included in the form of three 4.7k ohm resistors to Q1, Q2, Q3, and a 2.7 ohm in the RESET circuit. This gives the user some flexibility in choosing whether a given module should generate START, STOP, and RESET in a particular application.

7.6 GPIB INTERFACE OPTION (Talker)

This option provides the ability to read out the module data to the IEEE-488 interface bus. The system uses a byte-serial, bit-parallel format, with bidirectional lines for both data flow and addressing. The system employs a 16-line bus allowing interconnection of up to 15 instruments. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight lines transmit data and eight transmit handshake timing and control. Maximum accumulative length of cable in a system cannot exceed two meters (6.5 feet) per device or 20 meters (65 feet) per system, whichever is shorter. Data is transmitted as a series of seven-bit bytes in ASCII code. The eighth data line (parity bit) is not used since this option does not have parity generation capability.

The logic levels on the bus are negative TTL; that is, True = 0 V to +0.4 V dc, False = +2.5 V to +5V dc.

Bus signal nomenclature:

DIO8	data bit	Parity	ATN	Attention
DIO7	data bit	64	SRQ	Service Request
DIO6	data bit	32	IFC	Interface Clear
DIO5	data bit	16	NDAC	Not Data Accepted
DIO4	data bit	8	NRFD	Not Ready for Data
DIO3	data bit	4	DAV	Data Valid
DIO2	data bit	2	EOI	End Or Identify
DIO1	data bit	1	REN	Remote Enable

Control functions via eight-position DIP switch, accessible through a hole in the side cover, are as follows:

1-5. Talk Address Decode (1, 2, 4, 8, 16): Five switches set up in binary format provide the instrument a talk address range of from zero to 30. Address 31 is illegal.

6. TON (Talk Only): When selected, the capability is provided for a single device (Talker) to send data to a listener without the need for a controller. When a controller is in the system, the TON switch must be off.

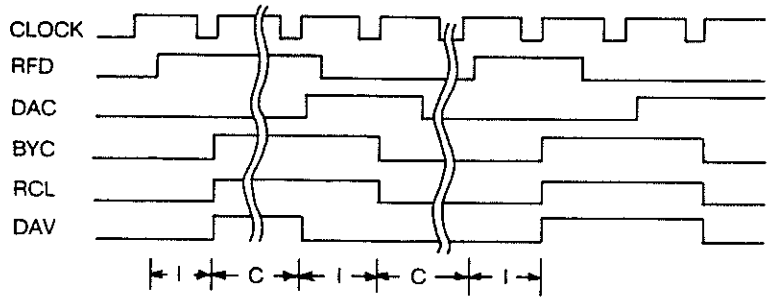
7. RCYL (Recycle): On provides the capability for the interface to restart the counter at the end of the readout cycle. It would be used by the master module in the counter system and its address would be the largest (ie, read out last). This minimizes readout dead time.

8. CR/FF (Carriage Return/Form Feed): Allows selection of message unit delimiter; selection usually based on needs of peripheral device printing the hard copy. ON provides CR; OFF provides FF.

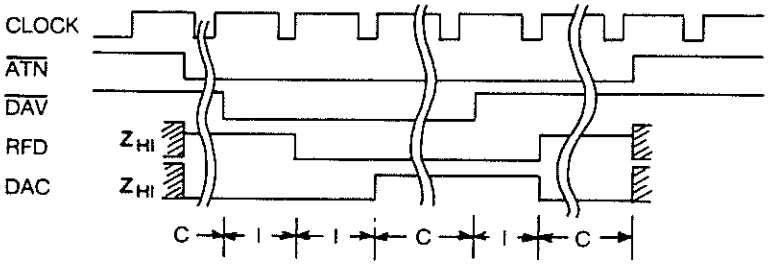
The Source checks that RFD is true, DAC is false, then puts the character information onto the data lines.

After data settling time, source generates DAV indicating valid data on the bus. The Acceptor sets RFD false because it is taking the data. When it has taken the data it sets DAC true. The source recognizes its character has been received when all listeners have set their NDAC false. The source sets DAV false and changes the data to the new character after it recognizes RFD true and DAC false again. Data is transmitted asynchronously at a rate determined by the slowest device, Source or Acceptor.

SOURCE HANDSHAKE TIMING



ACCEPTOR HANDSHAKE TIMING



I = Interface-2072A Response Time: 7 microseconds, maximum.
C = Controller Response Time: No limit. Varies with Controller.
True logic convention signals described in GPIB OPTION FUNCTIONAL DESCRIPTION
Source generates DAV
Acceptor generates RFD and DAC

Figure 7.2
GPIB Handshake Timing

7.7 GPIB OPTION FUNCTIONAL DESCRIPTION

The following twelve functions, identifiable on the GPIB Interface schematic, are described in terms of the function inputs and outputs with brief descriptions of the output functions.

1) Acceptor handshake timing

Inputs		
CK	CLOCK	FROM INTERNAL CLOCK
RSET/	RESET	FROM RESET LOGIC
DAV/	DATA VALID	BUS GENERATED
ATN/	ATTENTION	BUS GENERATED
Outputs		
RFD	READY FOR DATA	ACTIVE WHEN READY TO RECEIVE THE NEXT BYTE FROM THE BUS
DAC	DATA ACCEPT	ACTIVE AFTER DECODED BYTE HAS BEEN ACCEPTED BY THE MODULE
DVAL	DATA VALID	ACTIVE FOR ONE CLOCK PERIOD DURING STABLE AND VALID DATA - STROBES ALL MODULE DECODERS AND LATCHES

2) Source handshake timing

Inputs		
CK	CLOCK	FROM INTERNAL CLOCK
RSET/	RESET	FROM RESET LOGIC
DAC	DATA ACCEPT	BUS GENERATED
RFD	READY FOR DATA	BUS GENERATED
TE	TALK ENABLE	FROM TALK DELAY GENERATOR
TED	TALK ENABLE DELAY	FROM TALK DELAY GENERATOR
S3	STATE 3	FROM OUTPUT DATA SEQUENCER
Outputs		
BYC/	BYTE CLOCK	GENERATED TO SYNCHRONIZE INTERNAL CIRCUITS ON EACH OUTPUT BYTE
RDY/	READY	INACTIVE DURING THE PERIOD WHEN STATE AND BYTE CHANGES ARE OCCURRING - GOES INACTIVE ON DAC; ACTIVE ON THE RISING EDGE OF NEXT CK AFTER BYC GOES INACTIVE
TKIT/	TAKE IT	GENERATES DATA VALID TO THE BUS - GOES ACTIVE AFTER A DELAY TIME (ALLOWING DATA TO SETTLE) AND RFD INACTIVE AFTER DAC
HVIT	HAVE IT	ACTIVE INDICATED BYTE RECEIVED ON THE BUS - GENERATED BY DAC AND VALID TO THE END OF BYC; FORCED BY TE/, TED/, OR RDY/ TO PREVENT BYC
RCL	READ CLOCK	SENT TO COUNTER TO CLOCK THE BYTES FROM THE COUNTERS IN S3; DATA CHANGES TO NEXT LSB ON THE FALLING EDGE OF RCL

3) Talk Delay Generator

Inputs		
CK	CLOCK	FROM INTERNAL CLOCK
ATN/	ATTENTION	BUS GENERATED
MTA	MY TALK ADDRESS	FROM MY TALK ADDRESS LATCH
Outputs		
TE/	TALK ENABLE	ACTIVE FOR TALK STATE
TED	TALK ENABLE DELAY (A12-2)	SYNCHRONIZES BUS TO INTERNAL CLOCK FOR CORRECT TIMING

4) My Talk Address Latch

Inputs		
MA	MY ADDRESS	FROM MY ADDRESS DECODER
D7/-D6/	DATA 7-6	BUS GENERATED = [10]
DVAL	DATA VALID	FROM ACCEPTOR HANDSHAKE TIMING
BYC	BYTE CLOCK	FROM SOURCE HANDSHAKE TIMING
HVIT	HAVE IT	FROM SOURCE HANDSHAKE TIMING
LB	LAST BYTE	FROM OUTPUT DATA SEQUENCER
ABRT/	ABORT	FROM RESET CIRCUIT
TON	TALK ONLY MODE	S20-6
ECOL	END OF COLLECT	FROM COUNTER BOARD
Outputs		
RCE	READ CLOCK ENABLE	OUTPUT TO COUNTER BOARD TO ENABLE RCL
MTA	MY TALK ADDRESS	ACTIVE AFTER BUS COMMAND MTA; INACTIVE AFTER DTA OR UNT BUS COMMANDS; CLEARED ON LB AND HVIT

5) My Address Decoder

Inputs		
D1/-D5/	DATA 1-5	BUS GENERATED
S20-1	ADDRESS	BUS ADDRESS SELECT SWITCHES;
S20-5	SWITCHES	BINARY WEIGHTED - 1 to 16 NOTE: All switches "on" (address = 31) is not allowed
Outputs		
MA	MY ADDRESS	ACTIVE FOR (D1/-D5/) = (S20-1 TO S20-5)

6) Serial Poll Mode Latch

Inputs		
D1/-D7/	DATA 1-7	BUS GENERATED
DVAL	DATA VALID	FROM ACCEPTOR HANDSHAKE TIMING
ABRT	ABORT	FROM RESET CIRCUIT
Outputs		
SPM/	SERIAL POLL MODE	ACTIVE AFTER SPE COMMAND FROM THE BUS - D7-D2 = 001100 AND D1 = 01; INACTIVE AFTER SPD COMMAND — D7-D2 = 001100 AND D1-0

7) Service Request Logic

Inputs		
REM	REMOTE	FROM REMOTE LATCH
SPM	SERIAL POLL MODE	FROM SERIAL POLL MODE LATCH
TE/	TALK ENABLE	FROM TALK DELAY GENERATOR
ECOL	END OF COLLECT	FROM COUNTER BOARD FOR ANY STOP COLLECT
Outputs		
SRQ/	SERVICE REQUEST	ACTIVE AFTER EOC/ UNTIL TE/; IN REMOTE ONLY
SPR/	SERIAL POLL RESPONSE	ACTIVE IF SPM PRIOR TO TE/ AND SRQ TO GATE SERIAL POLL RESPONSE TO THE BUS

8) Output Data Sequencer and Gating

Inputs		
TE/	TALK ENABLE	FROM TALK DELAY GENERATOR
TKIT/	TAKE IT	FROM SOURCE HANDSHAKE TIMING
SPR/	SERIAL POLL RESPONSE	FROM SERVICE REQUEST LOGIC
SPM/	SERIAL POLL MODE	FROM SERIAL POLL MODE LATCH
BYC/	BYTE CLOCK	FROM SOURCE HANDSHAKE TIMING
RDY	READY	FROM SOURCE HANDSHAKE TIMING
RCYL	RECYCLE	RECYCLE MODE SELECTED S20-7
CR/FF	ASCII CR OR FF	SELECTS EITHER CARRIAGE RETURN OR FORM FEED AS A MESSAGE UNIT DELIMITER - S20-8
LSB	LEAST SIGNIFICANT BYTE	ACTIVE DURING AN LSB FROM THE COUNTER BOARD
A + B/	CTR A and Bnot	ACTIVE HIGH WHEN THE FIRST COUNTER IS BEING SENT AND LOW FOR OTHER COUNTERS. CHANGES ON THE FALLING EDGE OF LSB
BCD1	BINARY	FROM THE COUNTER BOARD
BCD2	CODED	DURING DATA OUTPUT, CONTAIN THE
BCD4	DIGITS	COUNT DATA SYNCHRONIZED TO BYC;
BCD8		SENT MOST SIGNIFICANT DIGIT FIRST
Outputs		
S3	STATE 3	ACTIVE FOR ALL STATES EXCEPT SPM, S4 OR S5; GATES BCD DATA WITH ASCII HEADER (3X HEX) IF RDY AND TE TO THE BUS
S4/	STATE 4	ACTIVE AFTER LSB TO GATE; MESSAGE UNIT DELIMITER TO THE BUS (SEPARATES COUNTER OUTPUTS)
S5/	STATE 5	ACTIVE AFTER S4 OF LAST COUNTER OUTPUT, GATES ASCII LINE FEED AND EOI TO THE BUS (END MESSAGE)
LB	LAST BYTE	ACTIVE AT THE END OF OUTPUT TO TERMINATE TALK MODE
EOI	END OR IDENTIFY	DRIVES BUS COMMAND LINE EOI (END MESSAGE)
ST5/	RESTARTS	PULSE SENT TO THE COUNTER BOARD DURING STATE 5 IF RECYCLE IS SELECTED

9) Device Clear

Inputs		
DVAL	DATA VALID	FROM ACCEPTOR HANDSHAKE TIMING
REM	REMOTE	FROM REMOTE LATCH
D1/-D7/	DATA 1-7	BUS GENERATED
Outputs		
DCL	DEVICE CLEAR	WHEN ENABLED SENDS A STOP PULSE TO THE COUNTER ON A DCL COMMAND FROM THE BUS D7-D1 = [0010100]

10) Remote Latch

Inputs		
CK	CLOCK	FROM INTERNAL CLOCK
RSET	RESET	FROM RESET CIRCUIT
MA	MY ADDRESS	FROM MY ADDRESS DECODER
DVAL	DATA VALID	FROM ACCEPTOR HANDSHAKE TIMING
D6/-D7/	DATA 6- 7	BUS GENERATED D7-D6 = [10 OR 01]
Outputs		
REM	REMOTE	ACTIVE AFTER HAVING RECEIVED MY LISTEN OR MY TALK ADDRESS FROM THE BUS; INACTIVE AFTER RSET

11) Reset Circuit

Inputs		
	POWER ON	ACTIVE AT POWER ON
IFC/	INTERFACE CLEAR	BUS GENERATED
TON	TALK ONLY	FROM S20-6
REN/	REMOTE ENABLE	BUS GENERATED
Outputs		
ABRT/	ABORT	ACTIVE AT POWER ON OR DURING IFC; CLEARS MY TALK ADDRESS AND SERIAL POLL MODE LATCHES
RSET/	RESET	ACTIVE AT POWER ON OR DURING REN. RESETS ALL HANDSHAKE CIRCUITS AND THE REMOTE LATCH; IF TON SELECTED, MONITORS REN/ TO PREVENT BUS CONFLICT WITH AN ACTIVE CONTROLLER

12) Internal Clock

THE CLOCK CIRCUIT GENERATES THE TIMING FOR PROPER OPERATION OF INTERNAL AND EXTERNAL CIRCUIT REQUIREMENTS

Positive Interval — GREATER THAN 3 μsec

Negative Interval — GREATER THAN 1 μsec

7.8 TYPICAL BUS INTERCHANGE

It is not the intent of this section to be a primer on how the GPIB controller must be programmed. Each of these has unique characteristics and must be studied in detail. There are also several tutorial publications available from Hewlett Packard, Teletronix and Fluke as well as the IEEE. The following descriptions illustrate how the 2072A with a 207x-01 interface will respond in the modes in which it will be most commonly used.

Serial Poll

This allows the controller to determine which device requires service. The 207x-01 will output a Service Request (SRQ) when it stops counting. The controller may then perform a Serial Poll (SPE) to determine who is requesting service. During the polling sequence, the controller will assign each of the devices to be polled Talk address, and then the device will put out a Status-byte. If the 207x-01 is requesting service it will output a 42_H, and remove its Service Request. If it was not the requesting device, then it outputs a status equal to 0. The controller completes the serial poll mode by doing a Serial Poll Disable (SPD). If the 207x-01 is the only possible source of the Service Request, the controller can choose to respond by Reading the data from the module; this will also clear its Service Request.

Source	7-bit Hex Code	ATN Status	Description
		Device Clear	
Controller	14	ATN Asserted	Will cause 2072A to terminate counting if jumper B installed in GPIB interface.
		Read Data	
Controller	3F	ATN Asserted	Unlisten all devices
Controller	35	ATN Asserted	Assign Listener at decimal address 27[3]
Controller	44	ATN Asserted	Assign Talker at decimal address 4[4]
2072A	30	ATN False	10^7 digit from counter A equals 0
2072A	30	ATN False	10^6 digit from counter A equals 0
2072A	38	ATN False	10^5 digit from counter A equals 8
2072A	31	ATN False	10^4 digit from counter A equals 1
2072A	36	ATN False	10^3 digit from counter A equals 6
2072A	32	ATN False	10^2 digit from counter A equals 2
2072A	39	ATN False	10^1 digit from counter A equals 9
2072A	37	ATN False	10^0 digit from counter A equals 7
2072A	0D[1]	ATN False	Carriage return
2072A	39	ATN False	10^7 digit from counter B equals 9
2072A	38	ATN False	10^6 digit from counter B equals 8
2072A	37	ATN False	10^5 digit from counter B equals 7
2072A	36	ATN False	10^4 digit from counter B equals 6
2072A	35	ATN False	10^3 digit from counter B equals 5
2072A	34	ATN False	10^2 digit from counter B equals 4
2072A	33	ATN False	10^1 digit from counter B equals 3
2072A	32	ATN False	10^0 digit from counter B equals 2
2072A	0D[1]	ATN False	Carriage return
2072A	0A[2]	ATN False	EOI Asserted, Line Feed

Note:
1. The carriage return indicating end-of-word may be switch selected to output a form feed (code 0C).
2. The line feed and EOI indicate to the controller that the 207x-01 presently talking is now finished sending data.
3. 27_{10} is the address of the device which is to receive the 2072A's data.
4. 4_{10} is the 2072A's address in this example with its channel A and B counters equal to 816297 and 98765432, respectively.

BASIC WARRANTY

Equipment manufactured by Canberra Industries, Inc. is warranteed against defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in the instruction manuals. During the warranty period, repairs or replacement will be made at Canberra's option on a return to factory basis. The transportation cost, including insurance to and from Canberra, is the responsibility of the Customer except for defects discovered within 30 days after receipt of equipment where shipping expense will be paid by Canberra to and from Canberra.

The customer must obtain an authorized customer service return number before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty.* In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment.

The Canberra Basic Warranty applies only to equipment manufactured by Canberra which is returned to the factory. If equipment must be repaired at the customer's site, the actual repair labor and parts will be provided at no charge during the warranty period. However, travel expenses to and from the customer's site, (travel time labor, and living expenses while on site), shall be paid by the customer unless an On-Site Warranty Option has been purchased. This option may only be purchased prior to shipment of the equipment to the customer.

The express warranties set forth herein are the only warranties with respect to the products, or any materials or components purchased from others and furnished by Canberra, and there are no other warranties, expressed or implied. The warranty of merchantibility is expressly limited as herein provided and all warranties of fitness are expressly disclaimed and excluded. Canberra shall have no liability for any special, indirect or consequential damages, whether from loss of production or otherwise, arising from any breach of warranty hereunder or defect or failure of any product or products sold hereunder.

EXCLUSIONS

Warranty service is contingent upon the proper use of all equipment and does not cover equipment which has been modified without Canberra's written approval or which has been subjected to unusual physical or electrical stress as determined by Canberra Service personnel. Canberra Industries shall be under no obligation to furnish warranty service (preventive or remedial): (1) if adjustment, repair or parts replacement is required because of accident, neglect, misuse, failure of electrical power, air conditioning, humidity control, transportation, or causes other than ordinary use; (2) if the equipment is maintained or repaired or if attempts to repair or service equipment are made by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by neutrons or heavy charged particles. Damage from these causes is readily identifiable as described in the manual accompanying each detector. Be windows are susceptible to mechanical damage and to corrosion from harsh or humid environments. Such damage is not covered by the warranty.

Although Canberra may frequently supply, as part of systems, equipment manufactured by other companies, the only warranty that shall apply to such non-Canberra equipment is that warranty offered by the original manufacturer, if any.

Canberra will, upon request, offer, as an option, warranty coverage for non-Canberra equipment such as computers and peripherals sold as part of a system supplied by Canberra. Quotations on this coverage may be obtained by contacting Canberra Customer Service or any of our sales staff.

SOFTWARE

Canberra warrants software media from defects discovered within 30 days after receipt.

Canberra assumes no responsibility for user-written programs or programs published as part of information exchange in Canberra periodicals.

Engineering assistance for software development is available and can be contracted through the Sales Department.

INSTALLATION

Installation of equipment purchased from Canberra shall be the sole responsibility of the customer unless the installation is specifically contracted for at the prevailing Canberra field service rates. To insure timely installation after receipt of equipment, it is recommended that installation be contracted for at the time the equipment is ordered.

ON-SITE WARRANTY OPTION

The On-Site Warranty Option provides for free on-site warranty work (Canberra pays all travel and living expenses) within the first 90 days after delivery of equipment to the customer. If installation is ordered from Canberra, the 90 day period commences upon completion of the initial installation. After the 90 day period, labor and materials used on site will still be covered by the basic warranty, but the customer shall pay for all travel expenses—travel time labor and living expenses incurred for any on-site service.

A maintenance contract may be purchased covering the period after the 90 days on-site warranty period, or after initial installation of the equipment. This is to be contracted through Canberra Customer Service.

REPAIRS

Any Canberra-manufactured instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. When returning instruments for repair, contact the Customer Service Department for shipping instructions and an Authorized Customer Service Return Number.

All correspondence concerning repairs should include the Model number and a description of the problem observed.

Once repaired, all equipment passes through our normal preshipment checkout procedure. Return shipping expense on out-of-warranty repairs will be charged to the customer.

For instruments out of warranty, the customer must supply a purchase order number for the repair before the item will be returned.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, immediately notify Canberra and the carrier making delivery, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in processing damage claims.

RETURN SHIPMENTS

Canberra Customer Service Department must be notified in advance if equipment is to be returned for any reason. Canberra can suggest the best means of shipping and will be able to expedite the shipment in case it is lost or delayed in transit.

The customer must obtain an authorized customer service return number before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty.* In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment. Care should be exercised in packing equipment for return. The customer is responsible for adequate packing to prevent damage in shipment. If the original shipping container is not available and the customer does not have the means to provide a suitable container, Canberra can provide a container for a fee.

Equipment should be returned to your area service center or to Canberra, Meriden. For shipment from outside the U.S., our shipping address is:

Canberra Industries, Inc.
c/o M.C.B. Customhouse Brokers, Inc.
Bradley International Airport
Air Cargo, Complex A
Windsor Locks, CT 06096 U.S.A.

SERVICE AND SERVICEABILITY

Canberra has gone to great lengths to insure that the instruments provided are functionally modular and therefore easy to service. In addition to modularity, Canberra has embarked on an extensive System Service Program to provide a totally responsive service capability. Complete Service Contracts with special arrangements for 24 hour response and weekend standby services are available from Canberra. For a detailed description of our Customer Service Program, please contact our Systems Service Department in Meriden, Connecticut, U.S.A.

REV	CHANGE	ECN	BY	DATE	APVD
	INITIAL RELEASE	3031	[illegible]	12/11/81	

DAISY CHAIN CONNECTORS
CONTROL IN = CI
CONTROL OUT = CO

DATA LATCH

BCD1
BCD2
BCD4
BCD8

A3 40174

R1 470Ω
R2 470Ω
R3 470Ω
R4 470Ω

D1
D2
D3
D4

C1 100 PF x 4

CI 1
CO 1
CI 2
CO 2
CI 3
CO 3
CI 4
CO 4

CI 5 — PRINT CLOCK IN
PRINT CLOCK OUT — CO 5

R5 4.7K
R6 10K
R19 4.7K
TP1
LS38 A1d
LS38 A1

R7 10K
LS38 A1b
4011 A11

DIGIT COUNTER
A4 40174

WORD COUNTER
A2b
A2a

FCLK
R8 4.7K
R9 4.7K
A8
C5 250 PF
0.01 μF
TP2

R10 4.7K
C18 100 PF
4069U
4049
4.7K R23

CI 8
CO 8
START

R11 100K
C7 100
ENABLE
R12 47K
D5
R14 C 4.7K
R15 4.7K
Q2 2N3904
Q3 2N3904
D
E
F

CI 7
CO 7
STOP

R13 4.7K
R22 4.7K
C7 100 PF
4049

R16 4.7K A
Q1 2N3904
B

CI 6
CO 6
HOLD

R17 10K
C8 390 PF
D5
R18 100K
A13 4069

A9 4001
A11 4001
4049
TP4
TP3
C2

A7b
A7a 4013
READOUT
TP5
SELECT SIGNIF
SELECT SIGNIF
S1
10K - 10M
+5

A7c 4001
A1a
A10
R20 10K
4001 A9d
A9a
4011 A11
C3
E3
E4

D3
R21 10K
R24
STP
RMTRS
RESET
CI 9
CO 9
RCL
STS
RCE

DISP. 1 — CONTROL IN 10 / CONTROL OUT 10
DISP. 2 — CI 11 / CO 11
DISP. 4 — CI 12 / CO 12
DISP 8 — CI 13 / CO 13
DISP. CLK. — CI 14 / CO 14

R23 - LAST DC
C18 - "
K LAST

CI 15
CO 15
GND
GND
+5V
C9 22 μF
C10 - C16 0.01 μF

0.01 μF bypass +5 & GND ONE FOR 3 IC
All DIODES IN914

NOTES

J4

DRAWN	K	DATE	FEB 81
CHKD	M		DEC 81
APPD MECH			
APPD ELEC			

2071
2072

INFC
DAISY CHAIN

CANBERRA

REV	CHANGE	ECN	BY	DATE	APPD
C	REVISED		JP	9-28-81	
D	REDRAWN TO D SIZE		WK	10-21-82	
	INITIAL RELEASE	3051	JP	12-11-84	
E	REVISED ADD A6-5/6	3060	RM	1-25-85	
F	ADDED NOMENCLATURE AR11775	3089	JP	2-26-85	
G	REV. SEE A/R 12610		HC	11-22-85	
H	REV. SEE AIR 13239		HC	11-17-86	

CONNECTOR J3

-12V 20
+12V 19
GND 18
RMTRS 17
GND 16
RCL 15
STF 14
STS 13
BCD1 12
BCD2 11
BCD4 10
BCD8 9
A/B 8
SHIELD 7
LSB 6
EOIL 5
RCE 4
EOIL 3
+5V 2
+5V 1

CLOCK

ACCEPTOR HANDSHAKE (LISTEN)

SOURCE HANDSHAKE (TALK)

RESET CIRCUIT

MY ADDRESS DECODER

ADDRESS COMPARATOR

REMOTE LATCH

MY TALK ADDRESS LATCH

SERVICE REQUEST LATCH

SERIAL POLL RESPONSE LATCH

TALK DELAY GENERATOR

OUTPUT DATA SEQUENCER

SERIAL POLL LATCH

DEVICE CLEAR

GPIB TRANCIEVERS

CONNECTOR GPIB

24	SIG GND
23	11 REF
22	10 REF
21	9 REF
20	8 REF
19	7 REF
18	6 REF
17	REN
16	DIO8
15	DIO7
14	DIO6
13	DIO5
12	SHIELD
11	ATN
10	SRQ
9	IFC
8	NDAC
7	NRFD
6	DAV
5	EOI
4	DIO4
3	DIO3
2	DIO2
1	DIO1

NOTES
1 ALL CMOS ARE "B" SUFFIX
2 UNLESS OTHERWISE NOTED: RESISTORS 100K
3 0.01μF BYPASS CAPS EVERY OTHER IC AND AT ○

2071 2072	DRAWN WK 10-21-82	GPIB INTERFACE	CANBERRA
	CHKD HC 12-2-81		
	APPR		DRAWING NO. B-18743 H
	MFG APPR		
	DO NOT TEMPLATE DRAW		SHT 1 OF 1

REV	STATUS	ECN	BY	DATE	AR
	INIT. RELEASE	8869	L	8-15-84	
A	REVISED - ADD ±12V FILTER	8991	RM	1-2-85	
B	REV. R62 10K WAS 5.1K PER AR 12771		HL	10-18-85	
C	REV'D SEE SHT 2 AR 13181		RJB	9/9/86	

+5V R19 R20 R21 220K R22 15K C7, 470pf C21 220pf CC 470 pf DD2.7 47/6 C54 R12 47K D23 R13 100K D2 W R15 R14 D3 R16 100K R89 D25 R88 10K R31 TP2 R33 C4 .68µf R66 6.8K R90 R17, 10MEG C5 150pf R18 RST 10K 2.7Ω R23 R24 D22 IN4003 R71 10K TP5 R67 510Ω 2.7Ω R27 R29 R34 4.7K R28 47K D6 D8 D9 R32 470 C9 330pf R30 47K D7 C7 470pf R62 10K D19 R59 51K C19 .1µf R60 1MEG C18 .1µf R58 100K R61, 2.7Ω C25 15µf 35V R57 3.3K D15 D16 C17 .01µf D17 IN5817 TYP (4)PL. D18 D5 R26 22K C11 47µf 6V C26,28-32,C33,34,38 .01µf C55 C56 C57 C58 L1 10µh L2 10µh. .1 22µf 15V. +12F -12F MPS8538 (2PL) MPS 8099 (2 PLS) Q1 Q2 Q3 Q4 T1 T2 A3 4013 A4 4049 A13 4011 A14 74LS38 A15 4081 A16 4069 A24 4538 A29 4538 A30 4049 A52 74LS02 A95 74LS02 A96 4001 A146 4001 A128 4011 A2 4069 J1 ENABLE

J3-17 EMTES
TEST
RESET A
RESET A
RESET B
RESET B
ENABLE
ECOL
ECOL
ENABLE
ATME
BTME
ACNTE
BCNTE
CNT
+5V
GND
+12V
-12V
TART
TOP
J3-13
J3-14
J3-3
J3-5
J3-7

FOR NOTES SEE SHEET 4

2072A	DRAWN E	DATE 10-15-81	SCHEMATIC DIAGRAM CONTROLLER 2072A
	CHKD KK	12-2-81	CANBERRA
	ENGR ELEC		

	INITIAL RELEASE 3869 L 8-84			
A	REVISED ADDTIZUFILTER	3991	RAM	1-2-85
B	REV. SEE SHT 1		HC	6-18-85
C	REV'D PER AR13181		RB	9/9/86

+5V
RN2 2.2K
A55 74LS196
74F00
A49 74LS390
A39 4001
A28 4011
A36 4011
A29 4013
A40 4069U
A59 7031
DATA
A23 A1
A22 A1
A21 A1
A20 B1
DECPT G8
A OF OUT B1
AX100 E1 C1
LDLH G7
ENABLE
R69 15K
R44 1K
Q11 2N3904
470PF C12
J101
ENB/OVF
AOUF D9
RN1 2.2K
A56 74F00
A50 74LS196
A49 74LS390
A98 7031
A97 4077
A39 4001
A40 4069U
A28 4011
A29 4013
B23 B1
B22 B1
B21 B1
B20 B1
LSB E7
B OF OUT B1
LDLH D1
BX100 E1 C1
AOUF A8
FOR NOTES SEE PAGE 4

2072A	DRAWN JC 10-13-81	SCHEMATIC DIAGRAM CHANNELS A & B. 2072A	CANBERRA
	CHK'D JK 12-2-81		
	APPD MECH		
	APPD ELEC		
	PROJ ADMIN		

	INITIAL RELEASE 3869 L 8-84			
A	REVISED -ADD ±12V FILTER	3991	RA	1-2-85
B	Rev. SEE SHT. 1 AR 12771		MC	6-11-85
C	REVISED SEE SHT 2 AR 13181		RJG	9/9/86

A23
A22
A21
A20
A DATA
B23
B22
B21
B20
B DATA
TEST
A/B̄
N/B̄
LDLH
DISPLAY SELECT S1
RCE
AX100
BX100
RCEB
RCE
RCL
A16-3
R97
R45
R46 47K
R49
R50
R51 100K
R52 100K
C13 150pf
D19 IN914
C14 .047uf
C15 .01µf
TP4
TP11
TP12
A37 4519
A38 4052
A8 4022
A23 4013
A12 4085
A17 4085
A32 555
A13 4011
A2 4069U
A4 4049
A16 (2) 4081
A25 4011
A30 4049
A52 4049
A4 4001
A26 4001
A39 4001
BCD8
BCD8A
BCD4
BCD2
BCD1
SCNRA
SCNRB
ST6
ST5
ST4
ST3
ST2
ST1
SCNC
DF
DECPT
LDLH
LSB
J3-9
J3-10
J3-11
J3-12
J3-15
J3-6

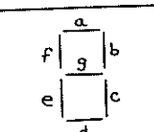
FOR NOTES SEE PAGE 4

2072A	DRAWN MC 10-9-84	SCHEMATIC DIAGRAM DATA MUX 2072A	CANBERRA	
	CHKD MC 12-2-84		DRAWING NO. B-20656	REV. C
	APPD MGR		SHT 3 OF 5	
	APPD ELEC			
	NEXT ASSY	SCALE NONE DO NOT TEMPLATE DRAWING		

B	REV. SEE SHT 1 AR 12771		HMC	6-8-85
C	REVISED SEE SHT 2 PER AR 13181		RJB	9/9/85

RMT OF X100

CNT AB MIN SEC



a
f
g
b
e
c
d

SEGMENTS

BACK LIGHT FOR LCD

LCD CONNECTIONS

(SEG) 10^5 — J2-25 51 f; J2-26 52 g; J1-19 2 e; J1-20 3 d; J1-17 4 c; J2-22 48 b; J2-24 50 a

(SEG) 10^4 — J2-2 46 f; J2-1 47 g; J1-15 6 e; J1-14 7 d; J1-13 8 c; J2-4 44 b; J2-3 45 a

(SEG) 10^3 — J2-6 42 f; J2-5 43 g; J1-11 10 e; J1-10 11 d; J1-8 13 c; J2-19 39 b; J2-20 40 a

(SEG) 10^2 — J2-17 37 f; J2-18 38 g; J1-21 14 e; J1-22 15 d; J1-23 16 c; J2-15 35 b; J2-16 36 a

(SEG) 10^1 — J2-13 33 f; J2-14 34 g; J1-24 19 e; J1-25 20 d; J1-26 21 c; J2-10 30 b; J2-12 32 a

(SEG) 10^0 — J2-7 f; J1-1 g; J1-5 22 e; J1-3 24 d; J1-2 25 c; J2-4 27 b; J2-8 28 a

TP6 — J1-18 1 BACK PLANE; J2-23 49 CNT; J2-21 41 OF; J2-11 31 X100

TP1

CNT; MIN; SEC

A30 4049 — OF

A27 4085 — X100

A26 4001 — X100

A16 — X100 TURN OFF

A25 4069U — X100

A16 4085 — DEC.PT

A28 4011 — B

A5 4001 — A

A15 4011

A5 4001

A17 ½ 4085

A5 4001

A1 555 — R65; R63 150K; R64 150K; C22 .01; C23 6.8µf

R55 10Ω

A21 SAME AS A22

A20 SAME AS A22

A19 SAME AS A18

A11 SAME AS A22

A7 SAME AS A18

A9 SAME AS A22

A10 SAME AS A22

A22 CD4056 BE

A4 IN4 18 STBE4 IN; STBE3; IN3; STBE2; IN2; STBE1 CD-4054BE IN; VEE

2.7Ω; 2.7Ω; 2.7Ω

+5V

NOTES:

1) HEX INDICATES INTERSHEET CONNETION.
   A1 1 — REF NUMBER. INDICATES TO WHAT SHT OR SHTS HEX IS FOUND AT. COORDINATES HEX IS FOUND AT.
2) A1 1 — BLOCK INDICATES CONNECTIONS ON SAME SHT. REF NUMBER. COORDINATES BLOCK IS FOUND AT.
3) INDICATES CONNECTOR ON PC. BRD.
4) THERE ARE NO 4 WAY TIES ON THIS SCHEMATIC.
5) → 51 INDICATES WIRE POINT.
6) UNMARKED RESISTORS ARE 100K.
7) UNMARKED DIODES ARE IN914.
8) BY PASS CAPS 0.01µf TWO PER BUS PATH.
9) LOGIC IS BCMOS EXCEPT AS NOTED.

IC REFERANCE CHART

NO.	TYPE IC	OPEN GATES	NO.	TYPE IC.	OPEN GATES
A1	555		A29	4013	b
A2	4069U		A30	4049	a
A3	4013	b	A31	N/C	
A4	4049	a c	A32	555	
A5	4001	c	A33	N/C	
A6	4081		A34	N/C	
A7	4054		A35	RED 60	
A8	4022		A36	N/C	
A9	4056		A37	4519	
A10	4056		A38	4052	
A11	4056		A39	4001	d
A12	4085		A40	4069U	b c f
A13	4011	a d	A41	N/C	
A14	74LS38	a	A42	N/C	
A15	4011		A43	N/C	
A16	4085		A44		
A17	4085		A45	74LS02	
A18	4054		A46		
A19	4054		A47	4077	
A20	4056		A48	7050	
A21	4056		A49	74LS390	
A22	4056		A50	74S196	
A23	4013		A51	N/C	
A24	4538		A52	4049	a
A25	4069U		A53	4077	
A26	4001	b	A54	7031	
A27	4035		A55	74S196	
A28	4011		A56	74F00	

LAST COMPONENT REF. NO.	
RESISTOR	R98
CAPACITOR	C32
DIODE	D18

2072A	DRAWN JE 10-16-85	SCHEMATIC DIAGRAM	CANBERRA
	CHKD JK 12-2-85	DISPLAY 2072A	
	APPD MECH		
	APPD ELEC		