

**DUAL COUNTER TIMER  
Model 2071A**

---

**Operator's Manual**

*IC*



# Table of Contents

	Page		Page
<b>1. INTRODUCTION</b>		<b>7. THEORY OF OPERATION</b>	
1.1 Introduction.....	1	7.1 Eight Decade Counting Channel .....	15
<b>2. SPECIFICATIONS</b>		7.2 Crystal Based Time Generator .....	17
2.1 Inputs .....	1	7.3 Preset Counter .....	17
2.2 Input/Output.....	2	7.4 Six Decade Liquid Crystal Display.....	17
2.3 Front Panel Controls.....	2	7.5 Control .....	17
2.4 Performance.....	2	7.6 Power Supply .....	18
2.5 Internal Controls .....	2	7.7 Daisy Chain Option .....	18
2.6 Power .....	2	7.8 GPIB Interace Option (Talker) .....	19
2.7 Physical .....	2	7.9 GPIB Option Functional Description .....	21
2.8 Option: 2071-01		7.10 Typical Bus Interchange .....	22
GPIB (IEEE 488) Interface .....	2		
2.9 Option: 2071-02			
Canberra NIM Daisy Chain Interface.....	3		
<b>3. CONTROLS AND CONNECTORS</b>			
3.1 Front Panel .....	4		
3.2 Rear Panel .....	5		
3.3 Jumper Options .....	5		
<b>4. OPERATION</b>			
4.1 Display Annunciators .....	7		
4.2 Preset .....	7		
4.3 Event Counter .....	7		
4.4 Time Counter .....	7		
4.5 Dual Counter .....	7		
4.6 Single/Recycle.....	7		
4.7 Reset.....	8		
4.8 System Operation .....	8		
4.9 Gate A and B.....	8		
4.10 Enable .....	8		
4.11 Overflow.....	8		
<b>5. DAISY CHAIN INTERACE</b>			
5.1 System Setup .....	9		
5.2 Printing System .....	9		
5.3 Computer Control .....	9		
5.4 Daisy Chain Jumper Options .....	9		
5.5 Typical Systems .....	10		
5.6 Using the Model 1488 Scanner .....	10		
5.7 Field Installation of the Daisy Chain Option .....	10		
5.8 Control In/Out Connectors .....	11		
<b>6. INTERACTION OF MODEL 2071A with the GPIB</b>			
6.1 General Description of GPIB.....	12		
6.2 GPIB Switches .....	12		
6.3 Systems without a Controller.....	12		
6.4 Interaction with a Controller .....	13		
6.5 Three Common Methods of Operation .....	13		
6.6 Field Installation of the GPIB Option .....	14		
6.7 Connector .....	15		
		<b>FIGURES</b>	
		3.1 Front Panel .....	4
		3.2 Rear Panel .....	5
		3.3 Internal Controls.....	6
		5.1 Daisy Chain Option Controls .....	10
		5.2 Control In/Out Connector Wiring .....	11
		6.1 GPIB Option Controls .....	12
		6.2 GPIB Connector Wiring .....	15
		7.1 Model 2071A Block Diagram .....	16
		7.2 GPIB Handshake Timing .....	20

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100

# Section 1.

## Introduction

---

The Canberra Model 2071A Dual Counter/Timer provides, in a single width NIM module, two eight decade counters, a crystal time base, and presetting logic. Normal operation is as a preset timer and event counter, or as a preset event counter and timer. However, the Model 2071A may also operate as a dual counter plus preset timer without display of the preset data.

Both count INputs accept fast negative NIM or positive pulses, jumper selectable. A discriminator is provided allowing positive inputs to be compatible with unipolar and bipolar linear signals or TTL logic pulses. The front panel positive DISCRiminator covers an input range of +100 mV to +10 V permitting selective counting, eliminating spurious counting from noise or other erroneous pulses.

The Model 2071A accommodates input counting rates of 100 million counts per second (100 MHz) for negative inputs and 25 million counts per second (25 MHz) for positive inputs.

The internal crystal time base provides increments of 0.01 seconds or 0.01 minutes, and live time gating at one microsecond resolution.

Display of either counter's content is accomplished with a six digit Liquid Crystal Display. The LCD includes eight annunciators which describe the display and dynamic state of the unit. Automatic x100 range shift provides an indication of the six most, or six least significant digits.

Preset control is accomplished with a three digit thumb-wheel switch providing a preset range from one to  $99 \times 10^6$  increments.

The SINGLE/RECYCLE mode switch provides a method to automatically place the unit or system back into the counting mode ten seconds or 100 microseconds, jumper selectable, after preset or termination of the count mode is reached.

Master-Slave system operation can be accomplished via the front or rear panel interconnection of the ENABLE signal, or by either of the two optional I/O interfaces.

The Canberra NIM Daisy Chain option provides interfacing to all Canberra printing counters, timers, and readout scanners. Standard with the NIM Daisy Chain option is a Read Out Buffer capability such that with any number of counting modules a total of only 100 microseconds dead time is required.

The alternate Canberra GPIB (IEEE-488) option provides interfacing to a GPIB bus, and allows a GPIB Controller to start, stop, and read out counting systems.

A convenient ENABLE output will allow the Model 2071A to start, stop, and reset single or multiple combinations of other Canberra Series 2000 counting modules.

For an accumulation of data in channel A, a jumper can be changed to prevent the resetting of channel A.

External connection to the A or B GATE inputs will permit gating of incoming pulses when in the preset count mode, and gating of the time base for channel A or B, jumper selectable, when in the preset time mode. In this mode the gate provides one microsecond resolution. Thus when a system busy signal is connected to this input, the Model 2071A will provide extremely accurate dead time corrections.

## Section 2.

### Specifications

---

#### 2.1 INPUTS

A and B IN - Front panel BNC connectors accept positive linear, TTL, or negative NIM fast logic signals, jumper selectable. Positive operation accepts unipolar, bipolar, or TTL signals; amplitude: 0 to +10 V, +12 V maximum; input amplitude must exceed the adjustable discriminator level for 20 nsec to be counted. Negative NIM fast logic amplitude: -0.6 V to -1.6 V; minimum width 4 nsec below -0.6 V; input rise and fall times: 1 nsec to 300 nsec;  $Z_{in} \approx 1$  k ohms

dc for positive signals and  $\approx 50$  ohms for negative signals. GATE B - Counting control for channel B or time channel, jumper selectable; with time gate selected, 1  $\mu$ sec time resolution can be obtained; shipped as channel B counting control. Amplitude: +4 to +5 V or open circuit allows counting; zero to +0.8 V inhibits counting;  $Z_{in} \approx 100$  k ohms to +5 V bus. When used as time gating, system busy can be used for accurate dead-time correction.

## 2.2 INPUT/OUTPUT

**GATE A/ENABLE** - Front panel BNC connector having a multifunction capability; GATE A or ENABLE, internally selected with jumper plug; shipped in ENABLE position.

**GATE A** - With respect to channel A, same as GATE B.

**ENABLE** - Bidirectional as input or output, open collector function, logic "0" OR; sinks 20 mA, sources from 4.7 k ohm to +5 V bus.

As an Output - Provides counting control to other 2071A, 2072A or compatible modules; 0 to +0.8 V enables counting, +4 V to +5 V disables counting.

As an Input - 0 to +0.8 V enables counting mode; +4 V to +5 V or open circuit disables counting mode.

**ENB/OVF** - Rear panel BNC connector having a multifunction capability, ENABLE or OVERFLOW; internally selected with a jumper plug; shipped in the OVF position.

**OVF** - Outputs a +5 V pulse coincident with the eighth decade reset; rise and fall times < 200 nsec; width 0.3  $\mu$ sec nominal; dc coupled; sinks 5 mA, sources 2.5 mA at 2.5 V; internal jumper selects channel A or B as source. Shipped in the channel A position.

**ENABLE** - Bidirectional as input or output, open collector function, logic "0" OR; sinks 20 mA, sources from 4.7 k ohm to +5 V bus.

As an Output - Provides counting control to other 2071A, 2072A or compatible modules; 0 to +0.8 V level enables counting, +4 V to +5 V disables counting.

As an Input - 0 to +0.8 V enables counting mode; +4 V to +5 V or open circuit disables counting mode.

## 2.3 FRONT PANEL CONTROLS

**START/STOP** - Two-position momentary toggle switch initiates or terminates a counting sequence.

**RESET** - Manual push-button resets both counters to zero.

**SINGLE/RECYCLE** - Two-position toggle switch selects single or recycle mode of operation upon reaching a preset condition.

**0.01 SEC/COUNT B/0.01 MIN** - Channel B time base or count selector; three-position toggle switch to select 0.01 seconds, 0.01 minutes, or the external B IN as the B counter and preset function. When time is selected, channel A counts external events through A IN. When Count B is selected, channel A counts time in 0.01 second intervals. An additional capability selected by internal jumpers provides a time preset, and event counting in channel A and B. In this case time is not available for display or readout.

**A/B DISPLAY SELECT** - Two-position toggle switch selects which counter's contents are displayed on the LCD.

**PRESET NM  $\times 10^P$**  - Three-digit thumbwheel switch for channel B preset. M is units, N is tens, P is the power of 10. N and M range from 0 to 9; P has a range of 0 to 6; N = M = 0 disables the Preset function.

## 2.4 PERFORMANCE

**CAPACITY** - Eight decades per channel, allowing  $10^8$  - 1 counts in each.

**COUNT RATE** - 100 MHz max., negative; 25 MHz positive.

**PULSE PAIR RESOLUTION** - 10 nanoseconds, negative; 40 ns positive.

**CRYSTAL TIME BASE ACCURACY** -  $\pm 0.0025\%$  over operating temperature range.

**TEMPERATURE OPERATING RANGE** - 0 to 50°C.

**PRESET COUNT CHANNEL** - Limited to 1 MHz count rate; pulse width minimum 300 nsec.

**INDICATORS** - Six digit Liquid Crystal Display with auto ( $\times 100$ ) shift for displaying six most-significant digits. Eight annunciators on LCD describe the display. These are: OF (overflow),  $\times 100$ , CNT, MIN, SEC, A, B, decimal point. Active counting is indicated by CNT, MIN, or SEC blinking. Leading zeroes are suppressed.

## 2.5 INTERNAL CONTROLS

**STANDARD JUMPERS** (When set, perform the following):

- Inhibit reset of channel A when starting. In this mode channel A accumulates counts and is reset only by the manual pushbutton.
- Select OVERFLOW or ENABLE as the function of the rear panel connector.
- Select OVERFLOW output from channel B instead of channel A.
- Permit counting in both channels. In this mode the module may still be preset on time, but the time cannot be read out.
- Allow a pulse on ENABLE INPUT to start the module.
- Change recycle time from 10 sec to 100  $\mu$ sec.
- Select GATE A or B to gate the time channel.
- Select GATE A or ENABLE as the function of the front panel connector.
- Select input A and B to accept positive linear and TTL, or negative NIM signals.

## 2.6 POWER

	2071A Alone	with -01	with -02
+12	120 mA	155 mA	123 mA
-12	200 mA	235 mA	203 mA
+24	35 mA	35 mA	35 mA
-24	0	0	0

## 2.7 PHYSICAL

**SIZE** - Standard single width NIM module; 3.43  $\times$  22.12 cm (1.35  $\times$  8.71 inches) per TID-20893 (rev. A)

**NET WEIGHT** - 0.94 kgs (2.0 lb.)

**SHIPPING WEIGHT** - 3.2 kgs (7.0 lb.)

## 2.8 OPTION: 2071-01

### GPIB (IEEE 488) INTERFACE

#### A. Features

- Asynchronous ASCII data transmission bit parallel, character serial
- Uniquely addressable, switch controlled
- Talk/Listen mode
- Talk Only mode
- Auto recycle minimizes readout dead time
- Field installable
- Form feed or carriage return at end of word

#### B. Description

The General Purpose Interface Bus links a Canberra NIM counting module into the IEEE 488 standard communications network. As a Listener, this interface receives Start, Stop, and Readout commands from a controller. As a Talker, it supplies its accumulated data to a peripheral device. A Talk Only mode provides a controllerless means for a single module to read out to a peripheral Listener. The Auto Recycle mode allows the selected module to place itself (and the rest of the Canberra counting system) back into the count mode at the conclusion of its readout, thus minimizing system dead time. A side panel cutout provides

access to Set or Verify a Talk/Listen Address, select Talk Only mode, enable Auto Recycle, or select Form Feed/Carriage Return at the end of a word. This interface is a single PC board with a connector that allows convenient field installation.

### C. Specifications

**SIGNALS** - The input/output signals on the GPIB connector are TTL compatible. True equals 0 to + 0.4 V, False equals + 2.5 to + 5 V.

**CONTROLS** - Side-panel cutout provides access to:

- Address select switches (5)
- Talk-Listen/Talk Only switch
- Auto Recycle switch
- FF/CR switch

Internal jumper enables Stop command response (DC 2).

**CONNECTOR** - Standard GPIB connector on rear panel.

**CONFORMITY** - Option 01 contains the following subset of capabilities (for explanation see IEEE-488 Standard) SH1, AH1, T1, TE0, L0, LE0, SR1, RL0, PP0, DT0, C0, DC0/DC2 selectable.

### D. General Description of GPIB

The General Purpose Interface Bus is a link or network by which system components communicate with each other. Each system participant performs at least one of three roles: Controller, Talker, or Listener.

A Controller manages bus communications primarily by directing or commanding which devices are to send data to other devices (Talker), or receive data from other devices (Listener) during an operational sequence. A controller may also be interrupted or it may command specific action between devices.

The GPIB consists of 16 lines which are grouped into three sets according to function; there are 8 data lines, 3 control lines, and 5 general management lines. The 8 data lines carry ASCII characters (bit parallel) asynchronously; the control lines provide a data transfer handshake compatible with both slow and fast devices; the bus management lines allow initialization, interrupts, and special controls.

### E. Cable

One Canberra Model C2071-2 GPIB Data/Control cable 0.6 m (2 feet) long is supplied for connection to the GPIB bus.

## 2.9 OPTION: 2071-02

### CANBERRA NIM DAISY CHAIN INTERFACE

#### A. Features

- Synchronous BCD data transmission bit parallel, character serial
- Readout sequence determined by interconnect order
- Field installable
- System control via individual Start, Stop, and Reset signals
- Compatibility with Canberra counters and scanners
- Read Out Buffer

### B. Description

The Canberra NIM Daisy Chain Interface Option provides the basic 2071A module with a readout/control capability compatible with previous Canberra data-acquisition series modules.

Read Out Buffering is available by moving jumper DD to position CC. This sets the Recycle time to 100 microseconds and only needs to be carried out on the 2071A selected as Master. Operating the Master, and hence the entire system, in the Recycle mode provides a minimal (100 microsecond) dead time buffered counting system.

The problem of data transfer from the eight digit 2071A to the standard six-digit system is handled by a toggle switch on the interface board. It selects either the six most-significant digits or the least-significant digits. Two digits are lost in either case.

Control signals, Start, Stop, and Reset are received only if the unit is to be a system slave. A master unit will generate Start, Stop, and Reset. This logic is under internal jumper control.

### C. Signals

**CONTROL IN** - Accepts Start, Stop, Reset, and Print pulses (5 V negative going from + 5 V level, rise time 500 nanoseconds maximum, width 1.0 microseconds minimum. Also HOLD command (dc level change from + 5 V to + 0.5 V maximum during printout) is accepted. Rear panel 15-pin "D" connector (Amphenol 17-10150).

**CONTROL OUT** - Provides Start, Stop, and Reset commands (5 V negative going pulses from + 5 V level, rise time 500 nanoseconds maximum, width 1.9 microseconds minimum). Data output information is presented in the form of Serial BCD (logic 1 = + 4 to + 5 V dc, logic 0 = 0 to + 0.5 V dc). This connector also provides the "next unit" Print command; eighth and successive Print command pulses are routed out via a logic gate. All control lines except Print command are wired directly between Control In and Control Out connectors. Rear panel 15-pin "D" connector (Amphenol 17-20150).

### D. Controls

**SIGNIFICANT DIGIT SWITCH** ( $10^7 - 10^2/10^5 - 10^0$ ) -  $10^7 - 10^2$  position selects readout of the six most significant digits of the eight-digit word.  $10^5 - 10^0$  position selects readout of the six least significant digits of the eight-digit word. Jumpers allow the Model 2071A to act as a system master or as a slave.

### E. Cable

One Canberra Model C1404-2 Data/Control cable 0.6 m (2 feet) long is supplied for connection to other Canberra data acquisition series modules.

# Section 3. Controls and Connectors

This section outlines the uses of the Model 2071A's controls and connectors. A complete listing of signal parameters will be found in Section 2, SPECIFICATIONS.

## 3.1 FRONT PANEL

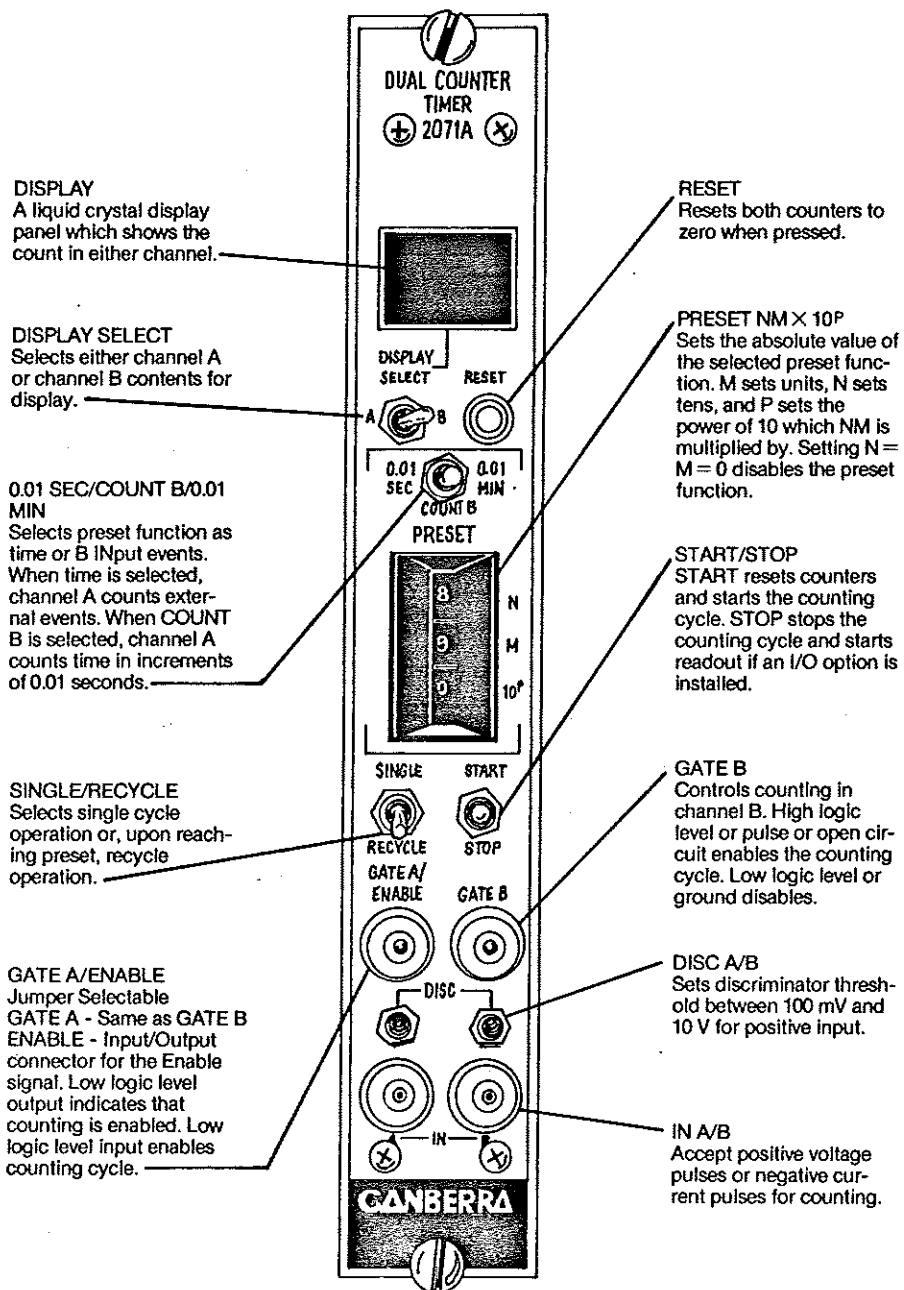


Figure 3.1  
Front Panel



### 3.2 REAR PANEL

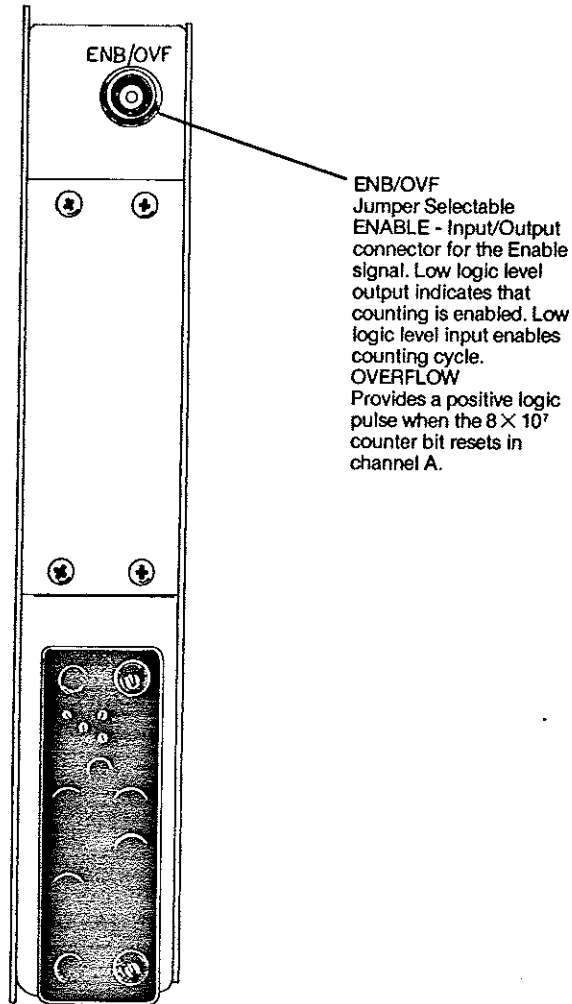


Figure 3.2  
Rear Panel

### 3.3 JUMPER OPTIONS

The Model 2071A jumpers are defined as follows:

Jumper	Function	Jumper	Function
A*	Allows the GATE B signal to enable counter B	W*	Allows ENABLE dc level to start and stop count
B	Prevents the GATE B signal from disabling counter B	Z	Allows ENABLE pulse's falling edge to start count
C*	Allows the GATE A signal to enable counter A	X	Disables LCD annunciator CNT for Dual Counting
D	Prevents the GATE A signal from disabling counter A	Y*	Enables LCD annunciator CNT
E*	Enables counting in channel A	1*	Enables LCD annunciator SEC
F*	Enables counting in channel B	2	Disables LCD annunciator SEC for Dual Counting
U	Enables Dual Counting	3*	Enables LCD annunciator MIN
G*	Allows the logic to reset channel A	4	Disables LCD annunciator MIN for Dual Counting
H	Prevents the logic from resetting channel A	5*	Enables channel A live time gating
J*	Channel A provides OVERFLOW signal	P	Enables channel B live time gating
K	Channel B provides OVERFLOW signal	6	Disables live time gating
N*	Enables preset select, time or counts	CC	Selects 100 $\mu$ sec recycle time
T	Enables only preset time for Dual Counting	DD*	Selects 10 sec recycle time
R	Selects front panel GATE A function		
S*	Selects front panel ENABLE function		

\*Indicates factory set position



# Section 4. Operation

The Model 2071A Dual Counter-Timer can be used as an event counter with a time preset, as a timer with a preset on a selected number of events, or, with internal jumper changes, as a dual counter preset on time. In the latter mode, time is not displayed or read out.

The unit will accept positive voltage logic pulses or negative current pulses (jumper selectable). Positive inputs are normally clamped to + 5 V and will see a nominal input impedance of 1k ohms. Negative inputs see a nominal 50 ohm input impedance.

## 4.1 DISPLAY ANNUNCIATORS

The liquid crystal display panel has, in addition to numerals to display counter contents, eight annunciators which describe the display's readout and the dynamic state of the unit.

- X100 Shows that the six most significant digits are being displayed.
- OF Shows that the displayed channel has overflowed and is counting up from zero again.
- CNT Shows that the selected channel is displaying counts. Blinks when the channel is active.
- A/B Shows which channel's contents are being displayed.
- MIN Shows that time, counted in minutes, is being displayed. Blinks when the channel is active.
- SEC Shows that time, counted in seconds, is being displayed. Blinks when active.

The eighth annunciator is a decimal point.

## 4.2 PRESET

The preset condition is set with the 0.01 SEC/COUNT B/0.01 MIN preset select switch and the three thumbwheel switches, N, M, and  $10^P$ . Selecting 0.01 SEC or 0.01 MIN will enable the unit to be used as an event counter with the time preset in increments of 0.01 seconds or 0.01 minutes (0.6 seconds). Setting  $N = M = 0$  disables the preset function.

Selecting COUNT B will enable the unit to be used as a timer with a preset on a number of counts. *CHA is the Timer - B gets counts.*

If the unit is to be changed to a dual counter, the time preset, either 0.01 seconds or 0.01 minutes, will be used but not displayed. *Internal Jumper*

The thumbwheel switches are used to select the number of preset units as chosen by the preset select switch. The M switch sets the units of the preset, the N switch sets the tens, and the  $10^P$  switch sets the power-of-ten multiplier.

For instance, if the switches are set to  $N = 1$ ,  $M = 0$ ,  $P = 3$  and the preset select switch is in the 0.01 SEC position, the time preset will equal  $10 \times 10^3$  hundredths of a second, or 100 seconds. If the select switch is in the 0.01 MIN position, the preset will equal  $10 \times 10^3$  hundredths of a minute, or 100 minutes. If the select switch is in the COUNT B position, the preset will equal  $10 \times 10^3$  counts, or 10 000 counts.

## 4.3 EVENT COUNTER

To use the Model 2071A as an event counter, INput A receives the external events to be counted. The 0.01 SEC/COUNT B/0.01 MIN switch must be placed in one of the time positions and the PRESET thumbwheel switches must be set for the desired time preset, as explained in section 4.2.

Pressing the START/STOP switch to START will start data accumulation. When the preset is reached, channel A will contain the total counts accumulated and channel B will contain the time during which the counts in channel A were accumulated. The time shown will equal the preset time.

To display the contents of either channel, move the DISPLAY SELECT switch to either A or B. Only one channel will be displayed at a time. The annunciators on the liquid crystal display will show either CNT (counts) or SEC or MIN (the selected time preset).

## 4.4 TIME COUNTER

To use the Model 2071A as a time counter, the channel B INput receives the external events to be counted and channel A records elapsed time in increments of 0.01 seconds.

In this mode, the preset select switch is placed in COUNT B and the PRESET switches can be set to stop the counting cycle at the selected number of counts. Channel A will show the time that it took to record the preset number of events.

## 4.5 DUAL COUNTER

By changing internal jumpers as outlined in Section 3.3.1, both channel A and channel B can count external events up to a preset time, either in 0.01 second or 0.01 minute increments as defined by the setting of the preset select switch and of the PRESET switches. In this mode, the time is not displayed or read out.

## 4.6 SINGLE/RECYCLE

With the SINGLE/RECYCLE switch in the SINGLE position, the counter, once started, will count to preset and stop. If the switch is moved to the RECYCLE position, the counter will count to preset, pause 10 seconds or 100  $\mu$ sec as selected by jumper CC/DD, clear the counters and start counting again. The recycle mode will continue until manually stopped, by setting the SINGLE/RECYCLE switch to SINGLE and pressing STOP.

#### 4.7 RESET

At any time, even during a count cycle, pressing the RESET button will clear both counters to zero. If a counting cycle is in progress, it will resume as soon as the RESET button is released.

In the RECYCLE mode, the counters are automatically reset at start-of-count. By changing an internal jumper, channel A automatic reset can be inhibited. In this mode, channel A can be reset only by pressing the RESET button. See Section 3.3.2.

The RESET button also functions as a display check. When the button is pressed, the display will show all "eights." Therefore, holding the button down will allow the operator to verify that the display is functioning correctly.

#### 4.8 SYSTEM OPERATION

Several of the Series 2000 counting modules can be configured in a Master/Slave relationship by connecting their ENABLE connectors in parallel with 93 ohm coaxial cable (type RG-62), using female-female-female "tee" connectors between the cable segments.

When the system is connected in this way, pressing START on one unit will start all units together.

The Master unit in the system is the one whose START button has been pressed, all other units are Slaves. Note that in this mode, the Slave presets are disabled. The Master unit's preset will control the entire system. Pressing STOP on the Master will stop all units together.

Either of the input/output options may also be used to set the system up in the Master/Slave mode. See Sections 5 and 6 for details.

#### 4.9 GATE A AND B

The GATE A function is available on the front panel GATE A/ENABLE connector. The factory set internal jumper must be moved from the ENABLE position to the GATE A position to allow GATE A inputs. See Section 3.3.8.

The GATE connectors accept positive logic pulses or a dc level to enable counting in either channel. Internal jumpers may be moved to disable the function for either channel or both channels. See Sections 3.3.4 and 3.3.5.

A logic high signal (+4 to +5 V) or an open input will enable counting; a logic low signal (0 to +0.8 V) will disable counting.

The gating signal gates the crystal-controlled time base, giving a gating time resolution of 1  $\mu$ sec. Using channel A as the event counter and channel B as the timer counter, a system-busy signal may be connected to the GATE A input to disable counting and the timer for accurate dead time correction. By moving an internal jumper, Time gating can be done with GATE B or can be defeated; see Section 3.3.3.

#### 4.10 ENABLE

The ENABLE function is available on both the front and rear panel. The front panel GATE A/ENABLE connector is

factory set to the ENABLE position. To select the front panel GATE A function, see Section 3.3.8. The rear panel ENB/OVF (ENABLE or OVERFLOW) connector is factory set to the OVERFLOW position. To select rear panel ENABLE function, see Section 3.3.7.

The ENABLE connector provides a logic low output (0 to 0.8 V) when the unit is enabled for counting. This output can be used to signal another unit that the Model 2071A is active. For instance, when using the Model 2071A as the Master unit in the Master/Slave System outlined in Section 4.8.

The ENABLE connector can also receive a logic low pulse to enable the Model 2071A for counting. For instance, as a Slave unit in the Master/Slave System.

To increase the Enable line's flexibility, an internal jumper (W) has been provided. If this jumper is moved to the Z position (see Section 3.3.12), the falling edge of an input pulse on the ENABLE connector will start the unit's counting cycle.

When the unit is started in this way, it is the Master unit in the system. The Enable line will be held low by this unit until its preset is reached, thus enabling all other units in the system.

If the Model 2071-02 Daisy Chain Interface is installed, it will not be necessary to use the Enable line. The Interface has all necessary signals to start and stop the unit.

If the Model 2071-01 GPIB Interface is installed, the Enable line will be used if the entire system is to start and stop at the same time. If the GPIB Controller is to address each unit separately, the Enable line will be used only if each individually addressed unit is the Master unit in separate sub-systems.

An internal jumper can be moved to change the front panel ENABLE function to GATE A. See Section 3.3.8.

#### 4.11 OVERFLOW

The OVERFLOW function is available at the rear panel ENB/OVF (ENABLE or OVERFLOW) connector which is factory set to the OVERFLOW position.

The rear panel OVERFLOW connector provides a positive logic pulse every time that channel A exceeds its count capacity ( $10^8$  counts). This signal can be connected to the input of another counter to extend the counting capacity of the system.

If the Model 2071A is used in the dual counter mode, the OVERFLOW signal can be connected to the B INPUT, instead of another counter, to extend the counting capacity of the system.

An internal jumper can be changed to allow the overflow of channel B to generate the OVERFLOW signal. See Section 3.3.6.

# Section 5.

## Daisy Chain Interface

---

The Model 2071-02 Daisy Chain Interface option provides both data input/output and system control. It is compatible with all existing Canberra Daisy Chain Systems.

The CONTROL IN and CONTROL OUT connectors present all Bus commands, with the exception of the Print clock, in parallel to all units in the system. The Print clock is presented serially to one unit at a time.

Since the Model 2071A is an eight-digit counter and the Daisy Chain System is capable of recording only six digits, a switch has been included on the Interface Board to select output of either the six most significant digits ( $10^2 - 10^7$ ) or the six least significant digits ( $10^0 - 10^5$ ). Refer to Figure 5.1 for switch location.

The nature of the data collection being performed will define which six digits to include in the data output. The unit is shipped with the switch in the six least significant digits ( $10^0 - 10^5$ ) position.

### 5.1 SYSTEM SETUP

A system of up to 50 data input modules and one scanner are connected with Model C-1404 cables. One 60 cm (two foot) cable is included with each Model 2071-02.

The CONTROL OUT connector of each unit is connected to the CONTROL IN connector of the next unit in the system. The last unit in the system is connected back to the scanner.

The system Master unit is defined as the one on which the START control is pressed. All other units are then Slave units.

When the Master unit is started, it generates a System Start command on the Daisy Chain Bus, which starts all Slave units at the same time.

When any unit reaches its preset, it stops and generates a System Stop command on the Bus. All units will stop at the same time.

In the SINGLE count mode, the system will run through one data collection cycle and stop when preset is reached.

In the RECYCLE count mode, the system will start, stop when any unit reaches its preset, pause ten seconds or 100 microseconds (jumper selectable, see Section 3.3.11), clear all counters, and start counting again.

### 5.2 PRINTING SYSTEM

If a Model 2088 Printer Scanner (RS232), or a Model 2089 Serial Scanner-Printer is connected in the system, the data collected by each unit can be printed out. A Model 9182 EIA to 20 mA Current Loop Adaptor can be connected to the 2088 for 20 mA current loop operation.

Standard with the NIM Daisy Chain option is a read out buffer. By taking advantage of the buffer circuitry, system dead time can be reduced. In a Recycle Mode, the buffer allows the unit to be placed back into the counting mode after the data has been latched into the readout buffer. After 10 seconds or 100 microseconds, jumper selectable, counting resumes and read out begins. During the readout time, the display will not be updated, but correct counting will go on. As with most buffers, counting time must be longer than readout time.

The first unit in the system to print out will be the one connected to the Scanner's CONTROL OUT connector. The second unit to print out will be the one connected to the first unit. The last unit to print out will be the one connected to the Scanner's CONTROL IN connector.

### 5.3 COMPUTER CONTROL

The Model 2088 Printer Scanner can be used to allow a computer to control the system. Refer to the Model 2088's manual for details on computer system operation.

### 5.4 DAISY CHAIN JUMPER OPTIONS

The Daisy Chain option board has four jumpers which will allow the user to tailor the option for specific applications. Three of these jumpers are 4.7k ohm resistors; the fourth is a 2.7 ohm resistor. Refer to Figure 5.1 for jumper locations.

1. Jumper A allows the Enable pulse's rising edge or the Model 2071A's control logic to generate the Daisy Chain Bus STOP command.

In the B position, this unit will not generate the STOP command.

2. Jumper C allows the Enable pulse's falling edge or the Model 2071A's control logic to generate the Daisy Chain Bus START command.

In the D position, this unit will not generate the START command.

3. Jumper E allows the Enable pulse's falling edge or the Model 2071A's control logic to generate the Daisy Chain Bus RESET command.

In the F position, this unit will not generate the RESET command.

4. Jumper G allows the Model 2071A's front panel RESET control to generate the Daisy Chain Bus RESET command.

In the H position, manual Reset will not generate the RESET command.

Please be aware that these jumpers do not need to be changed to be changed to make this unit a Slave unit. Slave status is normally defined by system operation.

If any or all of these jumpers were to be changed to their optional positions, this unit would be permanently defined as a Slave unit. It would never become a system Master unit until the jumpers were changed back to their usual setting.

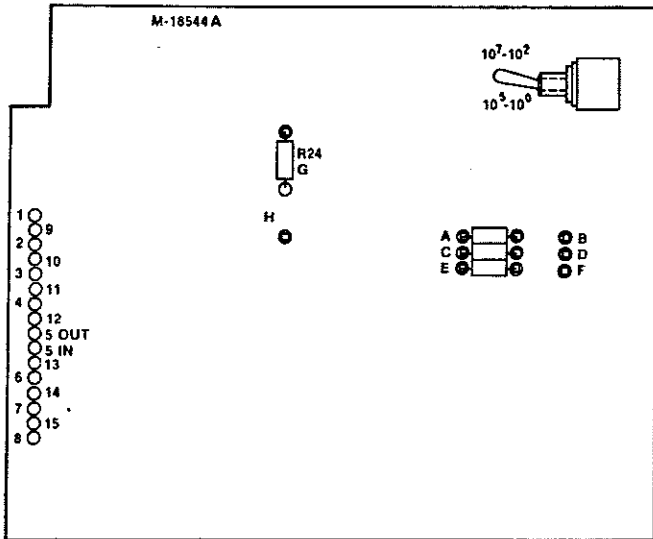
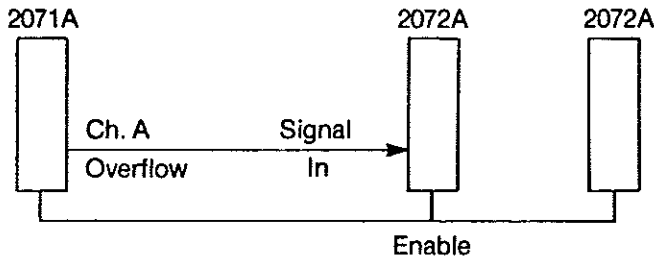


Figure 5.1  
Daisy Chain Option Controls

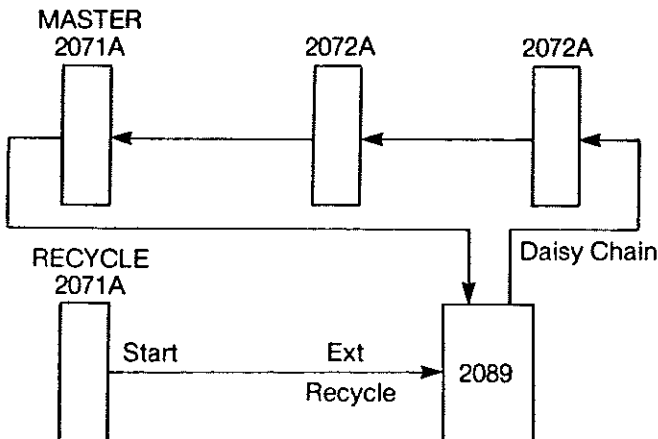
### 5.5 TYPICAL SYSTEMS

The following figures show some of the possible system setups.

1. Multi-input system with preset time and ability to count overflow from channel A of the 2071A.

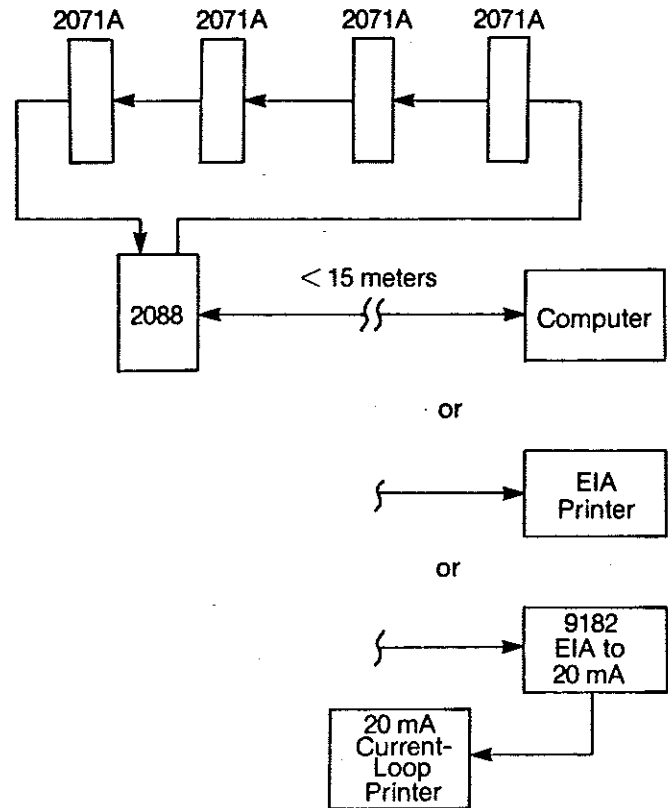


2. Multi-input 100 MHz Daisy Chain Printing System - preset controlled by master 2071A, recycle time controlled by 2071A. Printout from 2089 printer lists preset time and contents of 5 counters.



Note: The Model 2071A will require a factory modification (SERF) in order to operate with the Model 2089 External Recycle.

3. Multi-input 100 MHz Daisy Chain system with individual preset time for each counter. Slaves must reach preset before master. For this system, slaves are defined by changing the -02 option's internal jumpers (See Section 5.4).



### 5.6 USING THE MODEL 1488 SCANNER

If a Model 1488 Scanner is to be used instead of the Model 2088, the 1488 PRINT MODE switch must be set to PROMPT.

In the DELAYED mode, the HOLD command is not normally asserted until after the TTY motor-start time out, which will not allow proper data buffering.

For proper operation in the DELAYED mode, open the 1488 and look for a 10 ohm resistor soldered to points A-B (refer to schematic B-12177). Unsolder the resistor from points A-B and solder it to points A-C. This will cause prompt generation of the HOLD command on receipt of the Daisy Chain's STOP pulse.

The 1488's FORMAT switch must be set to LINE. Setting the switch to CONTINUOUS will cause incorrect data to be read out.

### 5.7 FIELD INSTALLATION OF THE DAISY CHAIN OPTION

The Daisy Chain Interface option consists of: four stand-offs, four lockwashers, 12 Phillips-head screws, the rear panel control connector plate, and the interface board.


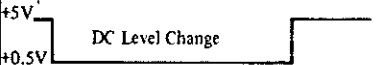
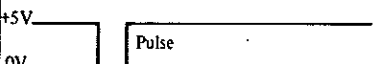
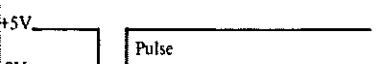
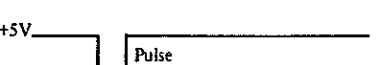

To install the option, first remove both side covers, each of which is held in place by five Phillips-head screws. Then:

1. If they are not already installed, install the four standoffs in the four holes in the unit's printed circuit board.
2. The standoffs are to be placed on the component side of the board and fastened to the board with one lockwasher and one screw each.
3. Carefully place the interface board in the unit so that the line of small circular connectors is at the rear of the board.
4. With the interface board's four mounting holes lined up with the four standoffs, press the board gently down to mate the interboard connectors.

The interface board should mate smoothly with the unit's connector. If any resistance is felt, the connector is not properly aligned; lift the interface board up a little and realign the four mounting holes with the standoffs before pressing down again.

5. Fasten the interface board to the standoffs with four screws, one in each corner of the interface board.
6. Mount the control connector plate on the rear panel with the four remaining screws.
7. Carefully align the ribbon cable's pins with the sockets of J4 at the rear of the interface board.
8. Press the cable's pins firmly down into the connectors until the cable is flush with the tops of the connectors.
9. Place S1, the six-digit select switch, in the desired position.
10. Before replacing the side covers, check the installation for proper operation.

## 5.8 CONTROL IN/OUT CONNECTORS

PIN No.	FUNCTION	SIGNAL DESCRIPTION
1	BCD Data "1"	Logic 1 = +4V, Logic 0 = 0V
2	BCD Data "2"	Logic 1 = +4V, Logic 0 = 0V
3	BCD Data "4"	Logic 1 = +4V, Logic 0 = 0V
4	BCD Data "8"	Logic 1 = +4V, Logic 0 = 0V
5*	Print Clock	
6	System Hold	
7	System Stop	
8	System Start	
9	System Reset	
10	Display BCD "1"	Logic 1 = 0V, Logic 0 = +4V
11	Display BCD "2"	Logic 1 = 0V, Logic 0 = +4V
12	Display BCD "4"	Logic 1 = 0V, Logic 0 = +4V
13	Display BCD "8"	Logic 1 = 0V, Logic 0 = +4V
14	Display Clock	
15	Ground	

**Figure 5.2**  
Control In/Out Connector Wiring

### NOTES:

All data and control lines except Print Clock line (pin 5) are internally wired directly between corresponding pins of the CONTROL IN and CONTROL OUT connectors.

The Print Clock pulse train from the Data Scanner will appear on pin 5 of the CONTROL OUT connector after module has finished printing its data contents.

The signals on pins 10 through 14 are not used by this unit.

# Section 6.

## Interaction of Model 2071A With the GPIB

### 6.1 GENERAL DESCRIPTION OF GPIB

The General Purpose Interface Bus is a link or network by which system components communicate with each other. Each system participant performs at least one of three roles: Controller, Talker, or Listener.

A Controller manages bus communications primarily by directing or commanding which devices are to send data to other devices (Talker), or receive data from other devices (Listener) during an operational sequence. A Controller may also be interrupted or it may command specific action between devices.

The GPIB consists of 16 lines which are grouped into three sets according to function; there are 8 data lines, 3 control lines, and 5 general management lines. The 8 data lines carry ASCII characters (bit parallel) asynchronously; the control lines provide a data transfer handshake compatible with both slow and fast devices. The bus management lines allow initialization, interrupts, and special controls.

### 6.2 GPIB SWITCHES

The eight-section DIP switch on the option board is accessible through the hole in the unit's side cover. The switches should be set to the desired positions before putting the unit in a NIM Bin. Refer to Figure 6.1.

The first five switches, counting from the top, are used to set the unit's GPIB address. Each switch is labeled with its value and with ZERO and ONE. The address is the sum of

all switches that are in the one position. An address of 31 (all switches in the ONE position) is illegal; it is reserved for the GPIB command UNTALK.

The sixth switch is labeled TALK ONLY. Refer to Section 6.3 for its uses.

The seventh switch is labeled RECYCLE. In the ON position, the unit will clear after readout and start counting again. In the OFF position, the unit is in the single cycle mode.

The eighth switch is labeled FF/CR. In the FF position, the message unit delimiter is sent out as an ASCII Form Feed. In the CR position, the delimiter is sent out as a Carriage Return. The choice of delimiter depends on the peripheral device being used.

### 6.3 SYSTEMS WITHOUT A CONTROLLER

The Model 2071A can operate in the Talk Only ON mode, which is used when data from a single module is to be passed directly to a single peripheral Listener device, such as a GPIB Printer. In this case a Controller is not required, but the printer must be in the Listen mode. Not all GPIB printers will operate in this mode.

In Talk Only ON mode, the 2071A will transmit its data to the listener as soon as 2071A data acquisition is stopped (by STOP or reaching Preset).

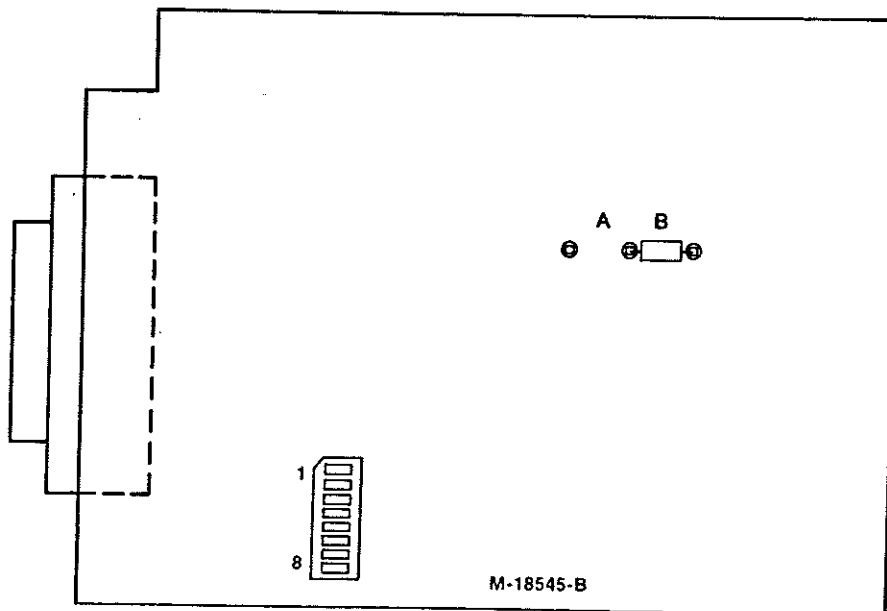


Figure 6.1  
GPIB Option Controls



## 6.4 INTERACTION WITH A CONTROLLER

Communication with a Controller requires 2071-01's TALK ONLY switch to be off. The Controller must assert REN (Remote Enable) during the entire communication. If REN is disabled, the 2071-01 will be reset. The first requisite is for the Controller to cause the 2071A to be placed in its Remote mode. It does this by transmitting on the GPIB, MTA, (My Talk Address) or MLA (My Listen Address), with ATN (Attention) asserted. MTA or MLA must agree with the five-bit address setting on the 2071A. The following MTA or MLA would be sent if the address setting was 5.

	DI07	DI06	DI05	DI04	DI03	DI02	DI01
MTA	1	0	0	0	1	0	1
MLA	0	1	0	0	1	0	1

If MTA is sent, the unit goes into its Remote mode and transmits all of its data (19 bytes). If MLA is sent, the 2071A does not respond further than placing itself into the Remote mode. Once in the Remote mode, the unit is able to generate an SRQ (Service Request) or respond to a DC (Device Clear). Disabling REN causes the 2071A to leave the Remote mode.

A typical counting sequence would begin with the operator pressing START on a 2071A that is connected to the GPIB. After reaching a preset, the 2071A will generate SRQ. The Controller would then, via a Serial Poll, determine the device requiring readout. Then send the proper MTA to read the data by way of a Read Data Interchange (Section 7.10). If the module is in the Recycle mode (switch on GPIB interface set to Recycle), the counters will be reset after readout and the counting cycle will begin again.

Note that there are two Recycle switches, one on the unit's front panel, and one on the GPIB interface card. The front panel switch allows the user 10 seconds to manually copy the display (or just view it) between cycles. When the 2071A is connected to the GPIB, the front panel switch is normally set to Single, and the GPIB interface switch set to Recycle. The recycle time will now depend on the devices on the bus with which the module must interact.

The time required to read data from a Model 2071A is determined by the sum of the response times of the Computer/Controller and 2071A. The 2071A responds to each query or handshake request within seven microseconds. This means the 2071A requires a maximum of 14 microseconds for each byte outputted. The 19-byte readout consumes 266 microseconds of 2071A synchronizing time. A readout to one Controller was measured at 12.5 milliseconds. This equates to 644 microseconds to accept data and generate handshake responses per byte, or a ratio of Controller to 2071A of 46 to 1. It is apparent that the Controller is the major contributor to readout time.

Some additional capabilities are:

### a. Controller Start

Since modules are independent, the Controller can start each module by performing a READ DATA Interchange (see Section 7.10). With a counter stopped and in a GPIB recycle mode, the completion of a READ DATA Interchange will cause it to clear and start counting. The controller can individually address each module for this sequence.

### b. Controller Stop

The Controller can send a Universal DEVICE CLEAR out on the bus, and all modules will stop counting. Individual modules cannot be addressed with this command, and it will not clear the modules, only stop them. If internal jumper B is moved to A, the module will ignore the DEVICE CLEAR command (see Figure 6.1).

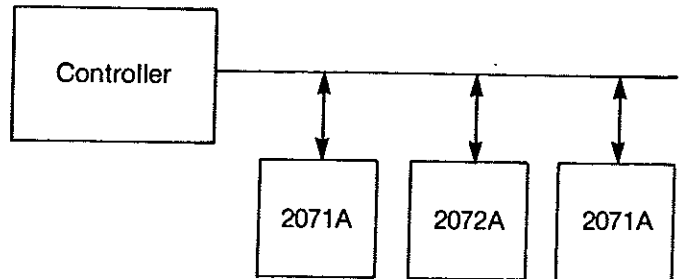
### c. Read Out While Counting

The Controller can read out each individual 2071A or 2072A while it is counting by performing a READ DATA Interchange (see Section 7.10). In this case the module will be read out and will not clear, but continue counting. A point to remember here is that a module will clear itself only if it is restarted by:

1. A manual front panel START.
2. A manual front panel RESET.
3. An ENABLE signal input.
4. Being in a front panel RECYCLE mode and stopped either by reaching preset or by receiving a Device Clear from the Controller.
5. Being in a GPIB Recycle mode, stopped by reaching preset or receiving a Device Clear from the Controller, then read out by a READ DATA Interchange.

## 6.5 THREE COMMON METHODS OF OPERATION:

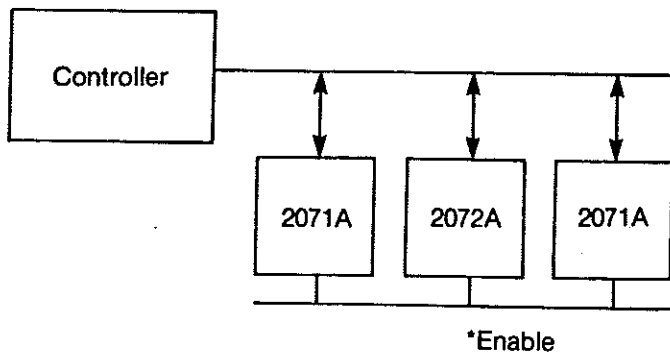
### A. Controller completely controls modules.



Sequence:

1. Controller performs READ DATA Interchange to start the modules. Each one must be addressed individually by the Controller. Thus, in this case, a simultaneous start is not possible. Data read out the first time is information left by previous operations.
2. Controller sends a DEVICE CLEAR, when desired, to stop all counters. Individual addressing is not possible with this command. All counters will simultaneously stop.
3. Controller again addresses each module with a READ DATA Interchange. Since they are in the Recycle mode (they would not have started in the first step if they weren't) each one clears, and restarts after reading out.

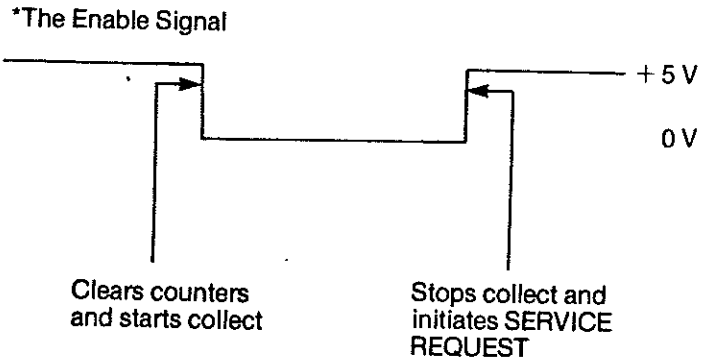
**B. Controller acts only as a readout device.**



**Sequence:**

1. ENABLE input/outputs on all modules are connected.
2. The START switch on one 2071A is pushed (this defines it as the Master).
3. All modules are stopped when the master reaches its preset.
4. Each module sends a SERVICE REQUEST when it stops if it was first commanded to REMOTE by the Controller.
5. The Controller addresses each module and reads it out.
6. If the Master is in the front panel RECYCLE mode, upon being read out it will enable the system to start counting again. All modules will have been cleared by the leading edge of the ENABLE signal. Normally the Master would be interrogated last so that it does not start the system until all other units have been read out.

3. When the preset on the Master 2071A is reached, it stops all modules, and each one generates a service request on the GPIB Bus. The Controller now interrogates each module. It should address the Master 2071A last, since this module is in the recycle mode and would start the system again once it is read out.



The modules on which the START switch is not pushed will ignore their presets and be controlled by the ENABLE signal. The Master module is defined as the module that has been started first, either manually or by being addressed from the Controller. Its preset will determine the presets for all other 2071As and 2072As.

**6.6 FIELD INSTALLATION OF THE GPIB OPTION**

The GPIB Interface option consists of: four standoffs, four lockwashers, 12 Phillips-head screws, a rear panel cover plate marked J102, and the interface board.

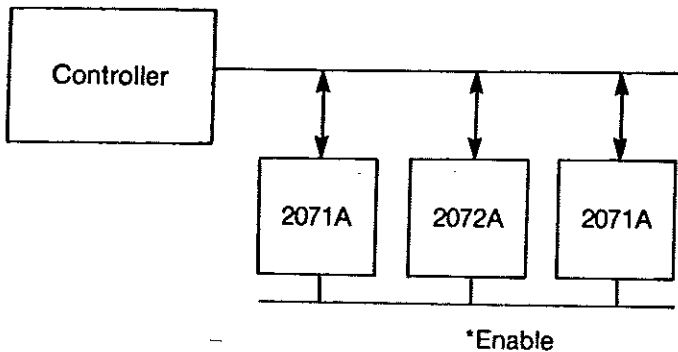
To install the option, first remove both side covers, each of which is held in place by five Phillips-head screws. Then:

1. If they are not already installed, install the four standoffs in the four holes in the unit's printed circuit board.
2. The standoffs are to be placed on the component side of the board and fastened to the board with one lockwasher and one screw each.
3. Carefully place the interface board in the unit so that the large connector at the rear of the board is flush with the rear panel.
4. With the interface board's four mounting holes lined up with the four standoffs, press the board gently down to mate the interboard connectors.

The interface board should mate smoothly with the unit's connector. If any resistance is felt, the connector is not properly aligned; lift the interface up a little and realign the four mounting holes with the standoffs before pressing down again.

5. Fasten the interface board to the standoffs with four screws, one in each corner of the interface board.
6. Place the J102 cover plate on the unit's rear panel and fasten it in place with the remaining four screws.
7. Before replacing the side covers, check the installation for proper operation.

**C. Controller initiates simultaneous start by addressing the master module.**



**Sequence:**

1. ENABLE input/outputs on all modules are connected.
2. Controller addresses first 2071A and reads it out. This defines it as the Master. Because it is in the GPIB Recycle mode it reads out, clears, and starts collecting. Since the ENABLE ports are connected, the other 2071A and 2072A modules clear and simultaneously start collecting. The Single/Recycle switch on each of their GPIB interface cards and front panel must be in the SINGLE mode.

# 1. INTRODUCTION

The Canberra Model 207x-03 EIA Interface provides readout, start, and stop of the Models 2071, 2071A, 2072, and 2072A counters by an EIA-compatible printer, terminal, or computer.

Multiple 207x modules, each with an 207x-03 option, can be chained together. This allows the terminal or computer to control or read out modules either individually or all at once, making possible multiple Master/Slave operation or multiplexed independent experiments.

## 1.1. Mode Selection

A cutout on the 2071A or 2072A's side panel provides access to DIP switches for:

- EIA Single/Recycle Operation
- Enable/Disable generation of Form Feeds, Line Feeds, Spaces and Carriage Returns in readout
- Select Baud Rate

- Select Operating Mode: Single Unit or Chain Mode
- Select Unit Status (chain mode): Master or Slave

## 1.2. Control Commands

Commands from a terminal or computer include:

- Start, Stop, and Reset of the module.
- Readout of module when stopped, during counting cycle, or during storage to the 207x-03's internal buffer for future readout.
- Change readout format: leading zero suppression, CR after each number, variable pause after each character and/or CR, and delayed response to readout command.
- Address one module or all modules on EIA chain.
- Select XON/XOFF software handshake.

# 2. INTERNAL CONTROLS

The ten-section DIP switch on the option board is accessible through the opening in the unit's left side cover.

Table 2.1 DIP Switch Functions

SWITCH	FUNCTION
SW1	RECYCLE/SINGLE CYCLE
SW2	FF
SW3	LF
SW4	CR
SW5	SP
SW6	BAUD 2 :
SW7	BAUD 1 : See Table 2.2
SW8	BAUD 0 :
SW9	ECHO/MASTER ENABLE
SW10	EIA CHAIN/SINGLE UNIT

## 2.1. Switch Setup

The following list describes the function of each of the ten DIP switches. An asterisk (\*) indicates the factory setting for each switch.

### SW1

OFF\* Selects Single Cycle mode. When unit stops counting it will read out, but not start up again unless the Front Panel SINGLE/RECYCLE is in the RECYCLE position.  
ON – Selects Recycle mode. When unit stops counting, it

will read out, clear, and start counting. Front Panel RECYCLE cannot be selected while in this mode.

### SW2

OFF\* No Form feeds generated during readout.  
ON – Form feeds generated during readout.

### SW3

ON\* Line feeds generated during readout.  
OFF – No Line feeds generated during readout.

### SW4

ON\* Carriage Returns generated during readout.  
OFF – No Carriage Returns generated during readout.

### SW5

ON\* Spaces generated during readout.  
OFF – No Spaces generated during readout.

### SW6-SW8

Switches SW6-SW8 set the baud rate (Table 2.2)

Table 2.2 Baud Rate Settings

Baud	SW6	SW7	SW8
19200	ON	ON	ON
9600	ON	ON	OFF
4800	ON	OFF	ON
2400	ON	OFF	OFF
1200	OFF	ON	ON



600	OFF	ON	OFF
300*	OFF	OFF	ON
150	OFF	OFF	OFF

#### SW9

OFF\* In EIA Chain mode (SW10 ON) unit not a master. In Single Mode, characters sent to the 207x-03 are not echoed back.

ON – In EIA Chain mode, unit is master (select SW9 ON in Unit # 1 only). In Single Mode, characters sent to the 207x-03 board from the computer are echoed back to the computer.

#### SW10

OFF\* Selects Single Unit mode of operation, no chain operation allowed.

ON – Selects EIA Chain mode of operation, all units in chain must have this switch ON.

### 3. OPERATION



## 6.7 CONNECTOR

A 24-pin standard GPIB connector (J102) is mounted on the rear panel. It carries the following signals:

Pin	Signal	Description
1	DIO1	Data I/O 1
2	DIO2	Data I/O 2
3	DIO3	Data I/O 3
4	DIO4	Data I/O 4
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready for Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	Shield	To earth ground
13	DIO5	Data I/O 5
14	DIO6	Data I/O 6
15	DIO7	Data I/O 7
16	DIO8	Data I/O 8
17	REN	Remote Enable
18		Twisted pair with pin 6
19		Twisted pair with pin 7
20		Twisted pair with pin 8
21		Twisted pair with pin 9
22		Twisted pair with pin 10
23		Twisted pair with pin 11
24		Signal Ground

Figure 6.2  
GPIB Connector Wiring

All GPIB signals are negative-true TTL compatible:

True = 0 to 0.4 V;

False = 2.5 to 5 V.

## Section 7. Theory of Operation

The Model 2071A includes two identical eight-decade counter channels, a crystal-based time generator, an eight-decade preset counter, a six-decade liquid crystal display, optional readout to a Canberra Daisy Chain Scanner or to a GPIB (IEEE 488) system, suitable control logic, and the power supply.

### 7.1 EIGHT DECADE COUNTING CHANNEL

Each of the identical counting channels has an input circuit which accepts positive voltage or negative current logic pulses on the same input connector (jumper selectable). Negative current-pulses see a 50 ohm impedance while the positive voltage-pulses see a nominal 1k ohm impedance.

With the A input jumper in the AP position, positive voltage signals are fed to the inverting input (pin 3) of comparator A58. A voltage divider consisting of R37, R42, and R43 along with clamping diodes D11 and D12 protect A58 from positive or negative over-voltages. When the positive input signal exceeds the threshold level set at A58-3 by R35 and front panel DISC A (RV2), A58-7 goes from  $\approx 5V$  to ground. This signal is fed through D10 to A56. Double counting with slow rise times is prevented by the feedback network consisting of R56, C20, and C21.

With the A Input jumper in the AN position, negative current input pulses are received by the 47 ohm terminating resistor R81 which develops a voltage drop fed to the base of Q8. When the voltage drop exceeds the threshold voltage set on Q9 base by R38 and R39, Q8 turns off and Q9 turns on. This brings Q9 collector and A56 input from  $\approx 2.5V$  to ground. Components D35, D34, R86 and D24 protect Q8 and Q9 from positive or negative overvoltages.

Operation of Channel B is identical to that of channel A.

Multiplexing counts or time ticks to the counter is carried out by A56 (74F00). Two gates are used by each counting channel. The first decade, which is required to count at 100 MHz, is a 74S196. The second, counting at 10 MHz maximum, is half of a 74LS390. The remaining six decades reside in a LS7031. The 7031 contains six counting decades, latches, and multiplexing logic to read out the six decades plus the data of the two decades ahead. Additionally, it contains logic to recognize leading zeroes and overflow conditions. Thus, in a simple 40-pin IC, a single 14-pin IC, plus half of 16-pin IC, we have an eight decade counter with readout multiplexing.

A counting sequence is initiated with a reset pulse setting all eight decades to zero. Either external events or time ticks are gated to the clock input of the 74S196. The eight bit of the 74S196 clocks the 74LS390, and in turn the eight bit of the 74LS390 clocks the 7031 input decade.

To read the contents for display or read out the counter, data is transferred to latches within the 7031 by means of the Load Latch pulse. The next part of the sequence is to generate a Scan Reset which places the most significant digit (in BCD format) on the four data output lines. As each succeeding digit is required, a Scan Clock pulse is applied to the 7031 which places the next less significant digit on the data output lines. Because the display consists of six digits and the counter capacity is eight, at the time the  $10^5$  counter decade 8 bit resets, A29 is toggled to the one state.

The signal out of the 7031 "D6" is this bit ( $8 \times 10^5$ ), and the output of A29 is called "X100". X100 true causes the X100 display annunciator to turn on and causes a two-digit shift in the data displayed.

The BCD data out of the 7031 is immediately passed through A53, a quad Exclusive-NOR gate. Its function is to either invert or not invert the data. The internal leading zero logic determines this and Blank Out is the signal. The utilization of this function is by the LCD display drivers. When they see a binary 15 they respond by displaying a blank. A BCD zero out of the 7031, if it is an insignificant (leading) zero, is then covered to binary 15 by inversion and is blanked on the display.

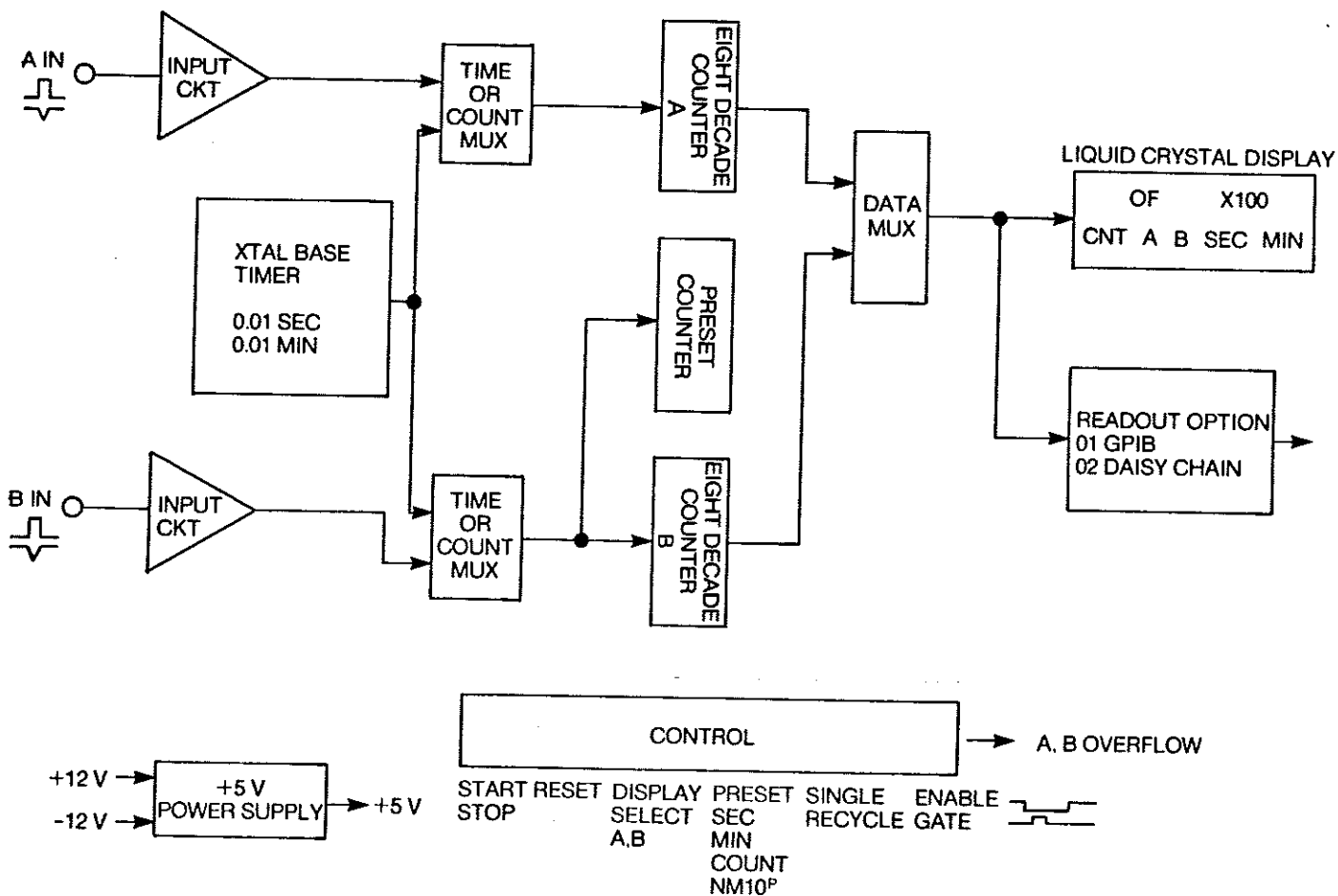


Figure 7.1  
Model 2071A Block Diagram



## 7.2 CRYSTAL BASED TIME GENERATOR

The required 0.01 second and 0.01 minute time ticks originate from a 12 MHz crystal oscillator circuit (OSC1). This frequency is divided by 12 in A33. The resulting one MHz may be gated (jumper selected) by the GATE signal as it passes through A13. This provides the unit a capability for measuring Live Time with a one microsecond resolution. The one MHz is then applied to a prescaler (A35) which provides a divide by  $10^4$  and gives a 0.01 sec output. Dividing the 0.01 sec by 60 (A34) provides the 0.01 min output. The selected time signal may be seen at TP8.

## 7.3 PRESET COUNTER

The eight-decade preset counter with three-digit control consists of a six-decade programmable prescaler plus a two decade down-counter. The three digit thumbwheel switch, labeled NM10P provides the eight decades of control. The P switch, with range zero through six, gives direct control over the prescaler (A51). A setting of zero means the input pulses are passed directly through. A setting of six results in the input prescaled (divided) by  $10^6$ . The N and M switches provide the start number for the two decade down-counter (A42, A43). In operation, the N and M decades are loaded with their preset numbers while the unit is not enabled to count. Once enabled, the N and M switches have no control; presets N and M will not be changed at any time, doing so during Enable True is not recommended. Setting both N and M to zero satisfies an eight-input NOR gate (A31) which disables the borrow from the two down counters, which normally occurs when preset is reached. Therefore,  $N = M = 0$  turns the preset function off. It should be noted also that the contents of A51, A42, and A43 are not available for readout.

## 7.4 SIX DECADE LIQUID CRYSTAL DISPLAY

The six-decade liquid crystal display (LCD) has each digit driven by a seven-segment LCD driver IC. With this scheme all digits are driven in parallel (that is, all ON segments are turned on at the same time). The requirement to turn a segment on is that an rms voltage be applied between the backplane and particular segment that is greater than the ON threshold for the LCD. This is accomplished by applying a square wave to the backplane and another to each segment. In-phase square waves result in zero rms (OFF) and  $180^\circ$  out-of-phase results in an rms of 5 V (ON). The type 4056 driver consists of a four-bit latch, a seven-segment decoder and an exclusive-OR array to select the proper phase of the signal applied to each segment.

The same clock (A32) used to strobe the data from the 7031s also provides the approximately 25 Hz square-wave display clock. In addition to the six digits, any of eight annunciators can be shown to describe the data being displayed. "CNT" is displayed when counts from an external source are selected for display. When time is selected, the annunciator "SEC" (seconds) or "MIN" (minutes) will be on. Seconds or Minutes are displayed with a maximum resolution of 0.01 units, therefore a decimal point annunciator is employed, further describing the information displayed. Because the data source may be from the A channel or B channel, A and B annunciators are provided. When the magnitude of the number exceeds six digits ( $10^6 - 1$ ) a X100

annunciator is enabled and the displayed data is shifted so that the display is  $10^7$  to  $10^2$ , the six most significant digits. It should be noted that loosing two digits means a display error ranging from 0.01% to zero. GPIB readout data includes the full eight digits. The remaining annunciator "OF" (overflow) turns on when the counter reaches  $10^8$  counts and remains on until data is reset.

The annunciators are driven by three 4054 four-signal segment drivers. These include latches and exclusive-OR arrays to develop the display-signal phasing required. Combinatorial logic consisting of gates A5, A15, A16, A17, A25, A26, A27, A28 determine which annunciators are on. Additionally A1, a slow oscillator, causes CNT, MIN, or SEC to blink during active counting.

The circuit to obtain data from each of the 7031s is essentially the same for readout or display. The selection of data from either the A channel or B channel is accomplished by multiplexer A37, whose data selection is controlled by the front panel Display Select switch and A23. A 23 is needed so that the data can be changed remotely in readout, allowing readout of both channels.

An oscillator (A32) running at about 50 Hz (divided by the other half of A23, to 25 Hz for the display clock) supplies the 7031 scan clock and an 8-stage Johnson counter (A8). The eight outputs of the Johnson counter are synchronous with the 7031 Digit Strobes and hence, the 7031 output data. The Johnson counter outputs strobe the data into the display LCD drivers. Also the first (TP11) or third (TP12) strobe generates a scan reset. This maintains synchronization and generates the X100 display data shift. Scan reset with the first strobe allows a display of  $10^5 - 10^0$ . Scan reset with the third strobe allows a display of X100 or  $10^7 - 10^2$ . This is accomplished by sending the first and third strobe pulses through A38, a dual multiplexer controlled by X100 signals from the A counter and B counter. In readout, the A32 oscillator is replaced by read clocks from the readout option. This is accomplished by half of A12.

## 7.5 CONTROL

The block diagram area labeled Control provides interactive control with all the blocks on the diagram. The prime control capabilities are to place the unit into the count enabled mode, determine which counter counts external events, and various jumper controlled options.

The signal ENABLE, brought to a front panel or rear panel BNC connector, is the count enable function. A low is the true state indicating counting is enabled. This is a bi-directional signal path which allows an external master unit to enable both channels for an externally determined time. The preset logic has no function in this slave mode of operation. The logic sequences in this mode are that once the ENABLE level has been pulled low by the master, a 10 microsecond reset pulse is generated (TP5) and sent to both A and B channels. This means a 10 microsecond dead time is incurred at the beginning of a measurement period. The timer logic, however, is not affected by this; thus time is measured from the beginning edge of ENABLE with only a two to three microsecond propagation delay error.

A Model 2071A may be either a master or slave with no jumper or control changes. Determination of master or slave status is dependent on whether or not the START switch has been pressed. The START switch causes one-half of A3 to be set. It, in turn, drives the ENABLE line low through A14-11. At this point any other units receiving the ENABLE signal are enabled to count as slaves. After the 10 microsecond reset period has elapsed, both counting channels and the preset channel are allowed to accumulate data.

The presence of a Daisy Chain option results in a slightly different concept of master and slave. This option provides interconnected START, STOP, and RESET signals to all units in the system. The preset control N, M, 10<sup>P</sup> must be set to N = M = 0 for a unit to operate as a slave. The ENABLE signal is not used (not connected between units). In this case the unit whose START switch was pressed (not necessarily the master unit) causes the Daisy Chain START pulse to toggle A3 to the one state via signal ST5 in each module.

Termination of counting occurs when the master reaches preset. This occurs on the simultaneous occurrence of borrow from both preset down-counters (A42 and A43), seen as a negative pulse at TP2. Pressing the STOP switch also terminates counting. The master unit then generates the STOP signal to the remainder of the system, terminating the experiment.

Determination of whether a channel counts time or external events is normally based on the preset selector, 0.01 SEC/COUNT/0.01 MIN, position. A preset of either time position results in that time interval being accumulated in channel B. Channel A will then accumulate external events through the A INput connector. Selecting a preset of counts causes external events through the B INput connector to be accumulated in channel B. The A channel will accumulate 0.01 second time intervals.

The GATE input signals normally control counting in channel A or channel B. Pulling the signal low, from an external source, will prevent any accumulation while held low. If the particular experiment requires one or the other channel only to be time gated, internal jumpers (5, P, and 6) provide control with the GATE signal. Normally in position 5, which results in the GATE A signal controlling the 1 MHz clock used to generate the time signals. This means live time can be accumulated with a resolution approaching one microsecond. To enable GATE B instead of GATE A, change this jumper to position P. To disable the Live Time gating, change this jumper to position 6.

An additional jumper-controlled operating mode is available. The mode allows an experiment to be carried out counting external events in both channel A and B and presetting the experiment with time. To accomplish this, move jumper F to U, move jumper N to T. For proper operation a preset of 0.01 SEC or 0.01 MIN is required. Note that the time information is not available for display or readout. In this special mode the display annunciators will not be correct until additional jumpers are changed. Move jumper 1 to 2, and move jumper 3 to 4 to make the display correct.

The Recycle operating circuit consists of the dual monostable A24. Its function is to restart the module approximately 10 seconds after termination of counting. When Recycle is enabled, A24 fires at the end of the count period (Enable goes false). After 10 seconds, the counters A, B, and Preset are reset to zero, counting restarted, and the experiment is carried out again. When Recycle is off (Single), A24 is held reset and the cycle does not start again. A recycle time of 100  $\mu$ seconds is selectable by moving jumper DD to position CC.

Manual data reset is accomplished by pressing the front panel RESET button. Data will be held reset while the button is pressed. To account for switch bounce, a final 10 microsecond reset is applied on release by A24 (pin 7). The application where manual reset is necessary is when jumper G is removed and jumper H installed. Now channel A is not reset with channel B, but only by the manual RESET button, allowing the A data word to accumulate continuously during succeeding count periods.

## 7.6 POWER SUPPLY

An inverter concept is applied to supply the five volts used by the module logic. Power supplied by the bin +12 V and -12 V buses is converted to ac by the oscillator made up of T1, Q3, Q4, and C17. Oscillation is in the 60 to 70 kHz range. The output of the secondary (T1 terminals 1, 2, and 3) is full-wave rectified by D17 and D18 providing the +5 V for the logic. T2 supplies feedback to the input of T1 (terminal 5), proportional to the output loading and ripple. As the load increases (and the ripple), current is added to the normal T1 input so that the ripple is reduced, compensating for changes in loading.

Short circuit protection is provided by the circuit consisting of Q1, Q2, and their associated bias resistors and capacitors. Q2 is normally on, Q1 off. Q2 collector current passes through R57 to the bases of Q3 and Q4 where, in conjunction with the output phasing of T1 secondary (terminals 7 and 8), oscillation is maintained. When current through R61 is on the order of 200 mA, or more, sufficient voltage is dropped to turn Q1 on, causing Q2 to turn off, effectively stopping the oscillator. Neither Q3 nor Q4 can be on; causing the 5 V secondary to go to zero. At the same time the IR drop through R61 goes to zero allowing Q1 to turn off, Q2 to turn on and the supply to start up. As long as the current loading is excessive, the circuit will be protected by alternately turning off and on.

## 7.7 DAISY CHAIN OPTION

The Daisy Chain Option allows a user to choose a type of readout or no readout at all depending on his needs. This option provides the ability to interface with existing Canberra counting modules and scanners with one limitation. Old Canberra counters were all six-decade devices so that the readout capability is also six digits. The new eight-decade counter option includes a switch to select which six digits are to read out. The six least significant digits will be selected if the user knows his experiment will not result in more than 10<sup>6</sup>-1 events counted. The six most significant digits can be selected when the experiment's results include numbers greater than 10<sup>6</sup>. This readout selection results in loss of the 10<sup>0</sup> and 10<sup>1</sup> data digits and the attendant error in the data.

The option provides interconnection for five control signals, four data-bits, and ground on two 15-pin connectors.

The control signals and their functions are:

1. **START:** a bidirectional negative-going pulse swinging from + 5 V to ground with a minimum width of 1  $\mu$ sec. The signal causes the counter it is applied to initiate a counting cycle.
2. **STOP:** a bidirectional negative-going pulse going from + 5 V to ground with a minimum width of 1.5  $\mu$ sec. The signal causes the counter it is applied to terminate a counting cycle, and the scanner it is applied to initiate a readout cycle.
3. **RESET:** a bidirectional negative-going pulse going from + 5 V to ground with a minimum width of 1  $\mu$ sec. The signal causes the counter it is applied to clear the data in its accumulators.
4. **HOLD:** a negative level at ground potential; + 5 V when false. This signal, generated by a scanner, disables the counter display-update function and enables the readout function.
5. **PRINT CLOCK:** a negative-going pulse going from + 5 V to ground with a minimum width of 3  $\mu$ sec. The signal originates at the scanner module and is used to request each BCD data character. The counting module, after receiving its required number of print clocks, passes succeeding ones on to the next module. This signal is the only one not wired in parallel to both 15-pin control connectors.

The four data bits swing between + 5 V and ground, are high true, and have 1, 2, 4, 8 weights. The signals are diode-isolated from the bus so that any module can cause a true level regardless of the others.

Readout begins with the HOLD signal going true as a result of the STOP pulse generated by any module in the system. HOLD (level) generated by the system scanner, received by the Daisy Chain interface, causes the Read Clock Enable (RCE) level to be sent to the counter logic. This results in initialization of the logic placing the most significant data digit ( $10^7$ ) on the data lines to the interface. After about 10  $\mu$ sec to allow for data propagation through the CMOS logic, the Readout flip-flop A7 is set (TP5 goes high). This removes the clear level applied to the Digit Counter (A4) and enables the fast clock (FCLK-A8) to advance the Digit Counter twice. This occurs before any Print Clocks arrive from the Scanner module. If the six least significant digits have been selected ( $10^5 - 10^0$  switch position), the first two fast clocks are also sent to the module as Read Clock (RCL) pulses. This advances the counter's output data from  $10^7$  to  $10^5$ . When the six most significant digits are selected ( $10^7$  to  $10^2$  switch position) the first two fast clocks are not sent to the module and the  $10^7$  data digit remains on the data lines to the option. When the scanner is ready for the first digit, a Print Clock pulse is sent. The leading edge loads the data into A3 (Data Latch). At the trailing edge, the next data digit is sent from the module to the option board. As the Scanner requires each additional digit, a Print Clock is sent requesting it, whereupon the leading edge loads the latch (A3) and the trailing edge causes the next digit data be presented to the latch. The seventh Print Clock causes gate A9c to be satisfied resetting the Digital Counter and the Data Latch.

The Fast Clock is allowed to generate two pulses placing the  $10^5$  data digit of the second data word on the data lines to the option. The two-bit Word Counter A2 keeps track of which word is being sent. After the second word has been sent, all succeeding Print Clocks are sent out to the next module via A1-8.

The bidirectional control signals START, STOP and RESET are received and/or generated as follows:

If the START switch is pressed, the ENABLE signal is sent to the option. An edge detector (A5a and A5b) generates a pulse to Q2 which generates the START pulse and sends it out to the remaining modules in the system. A START pulse sent from an external module is sent through the option to the main logic as ST5 where it toggles A3, setting the unit into the count mode.

The same edge-detector which causes the START pulse is also applied to Q3, which sends a RESET pulse to the other modules. Also pressing the front panel RESET button causes a RESET signal to be sent out to the external modules for as long as the button is pressed.

Pressing the STOP switch terminates the counting mode and causes a positive pulse (ECOL) to be sent to the option. It is applied to Q1, causing the STOP signal to be sent to the modules in the system. A received STOP signal, inverted twice, is sent directly to the main logic as STP where it clears A3, taking the unit out of the count mode.

Four jumpers have been included in the form of three 4.7k ohm resistors to Q1, Q2, Q3, and a 2.7 ohm in the RESET circuit. This gives the user some flexibility in choosing whether a given module should generate START, STOP, and RESET in a particular application.

## 7.8 GPIB INTERFACE OPTION (Talker)

This option provides the ability to read out the module data to the IEEE-488 interface bus. The system uses a byte-serial, bit-parallel format, with bidirectional lines for both data flow and addressing. The system employs a 16-line bus allowing interconnection of up to 15 instruments. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight lines transmit data and eight transmit handshake timing and control. Maximum accumulative length of cable in a system cannot exceed two meters (6.5 feet) per device or 20 meters (65 feet) per system, whichever is shorter. Data is transmitted as a series of seven-bit bytes in ASCII code. The eighth data line (parity bit) is not used since this option does not have parity generation capability.

The logic levels on the bus are negative TTL; that is, True = 0 V to +0.4 V dc, False = +2.5 V to +5V dc.

Bus signal nomenclature:

DIO8	data bit	Parity	ATN	Attention
DIO7	data bit	64	SRQ	Service Request
DIO6	data bit	32	IFC	Interface Clear
DIO5	data bit	16	NDAC	Not Data Accepted
DIO4	data bit	8	NRFD	Not Ready for Data
DIO3	data bit	4	DAV	Data Valid
DIO2	data bit	2	EOI	End Or Identify
DIO1	data bit	1	REN	Remote Enable

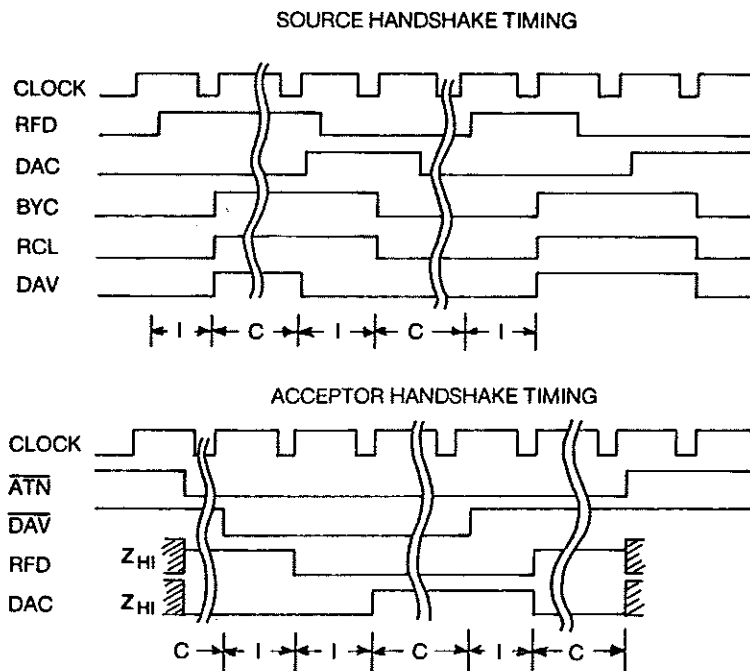
Control functions via eight-position DIP switch, accessible through a hole in the side cover, are as follows:

- 1-5. Talk Address Decode (1, 2, 4, 8, 16): Five switches set up in binary format provide the instrument a talk address range of from zero to 30. Address 31 is illegal.
- 6. TON (Talk Only): When selected, the capability is provided for a single device (Talker) to send data to a listener without the need for a controller. When a controller is in the system, the TON switch must be off.
- 7. RCYL (Recycle): On provides the capability for the interface to restart the counter at the end of the read-out cycle. It would be used by the master module in the counter system and its address would be the largest (ie, read out last). This minimizes readout dead time.
- 8. CR/FF (Carriage Return/Form Feed): Allows selection of message unit delimiter; selection usually based on needs of peripheral device printing the hard copy. ON provides CR; OFF provides FF.

For data transfer, a 3-line handshake sequence involving NRFD, DAV, and NDAC is used. The Source checks that NRFD is false, DAC is false, then puts the character information onto the data lines.

After data settling time, source generates DAV indicating valid data on the bus. The Acceptor sets NRFD true because it is taking the data. When it has taken the data it sets NDAC false. The source recognizes its character has been received when all listeners have set their NDAC false. The source sets DAV false and changes the data to the new character after it recognizes NRFD false and NDAC true again. Data is transmitted asynchronously at a rate determined by the slowest device, Source or Acceptor.

The 2071A monitors the Attention Line (ATN) to determine if the data on the bus' Data Lines is to be interpreted as commands (e.g., Talk Address, Listen Address, etc). When the line is false, the 2071A is in the Data Mode and can output its data.



I = Interface-2071A Response Time: 7 microseconds, maximum.  
 C = Controller Response Time: No limit. Varies with Controller.  
 True logic convention signals described in GPIB OPTION FUNCTIONAL DESCRIPTION  
 Source generates DAV  
 Acceptor generates RFD and DAC

Figure 7.2  
 GPIB Handshake Timing

## 7.9 GPIB OPTION FUNCTIONAL DESCRIPTION

The following twelve functions, identifiable on the GPIB Interface schematic, are described in terms of the function inputs and outputs with brief descriptions of the output functions.

<b>1) Acceptor handshake timing</b> <b>Inputs</b> CK        CLOCK                FROM INTERNAL CLOCK RSET/    RESET                FROM RESET LOGIC DAV/     DATA VALID        BUS GENERATED ATN/     ATTENTION            BUS GENERATED <b>Outputs</b> RFD     READY FOR DATA    ACTIVE WHEN READY TO RECEIVE THE NEXT BYTE FROM THE BUS DAC     DATA ACCEPT      ACTIVE AFTER DECODED BYTE HAS BEEN ACCEPTED BY THE MODULE DVAL    DATA VALID        ACTIVE FOR ONE CLOCK PERIOD DURING STABLE AND VALID DATA - STROBES ALL MODULE DECODERS AND LATCHES			<b>Outputs</b> SRO/    SERVICE REQUEST    ACTIVE AFTER EOC/ UNTIL TE/ IN REMOTE ONLY SPR/    SERIAL POLL RESPONSE    ACTIVE IF SPM PRIOR TO TE/ AND SRO TO GATE SERIAL POLL RESPONSE TO THE BUS
<b>2) Source handshake timing</b> <b>Inputs</b> CK        CLOCK                FROM INTERNAL CLOCK RSET/    RESET                FROM RESET LOGIC DAC     DATA ACCEPT        BUS GENERATED RFD     READY FOR DATA    BUS GENERATED TE      TALK ENABLE        FROM TALK DELAY GENERATOR TED     TALK ENABLE DELAY    FROM TALK DELAY GENERATOR S3      STATE 3              FROM OUTPUT DATA SEQUENCER <b>Outputs</b> BYC/    BYTE CLOCK        GENERATED TO SYNCHRONIZE INTERNAL CIRCUITS ON EACH OUTPUT BYTE RDY/    READY              INACTIVE DURING THE PERIOD WHEN STATE AND BYTE CHANGES ARE OCCURRING - GOES INACTIVE ON DAC; ACTIVE ON THE RISING EDGE OF NEXT CK AFTER BYC GOES INACTIVE TKIT/   TAKE IT            GENERATES DATA VALID TO THE BUS - GOES ACTIVE AFTER A DELAY TIME (ALLOWING DATA TO SETTLE) AND RFD; INACTIVE AFTER DAC HWIT    HAVE IT            ACTIVE INDICATED BYTE RECEIVED ON THE BUS - GENERATED BY DAC AND VALID TO THE END OF BYC; FORCED BY TE/, TED/, OR RDY/ TO PREVENT BYC SENT TO COUNTER TO CLOCK THE BYTES FROM THE COUNTERS IN S3; DATA CHANGES TO NEXT LSB ON THE FALLING EDGE OF RCL RCL     READ CLOCK        FROM THE COUNTERS IN S3; DATA CHANGES TO NEXT LSB ON THE FALLING EDGE OF RCL			<b>8) Output Data Sequencer and Gating</b> <b>Inputs</b> TE/      TALK ENABLE        FROM TALK DELAY GENERATOR TKIT/    TAKE IT              FROM SOURCE HANDSHAKE TIMING SPR/    SERIAL POLL RESPONSE    FROM SERVICE REQUEST LOGIC SPM/    SERIAL POLL MODE LATCH    FROM SERIAL POLL MODE LATCH BYC/    BYTE CLOCK        FROM SOURCE HANDSHAKE TIMING RDY     READY              FROM SOURCE HANDSHAKE TIMING RCYL    RECYCLE            RECYCLE MODE SELECTED S20-7 CR/FF   ASCII CR OR FF    SELECTS EITHER CARRIAGE RETURN OR FORM FEED AS A MESSAGE UNIT DELIMITER - S20-8 LSB     LEAST SIGNIFICANT BYTE    ACTIVE DURING AN LSB FROM THE COUNTER BOARD A + B/   CTR A and Bnot    ACTIVE HIGH WHEN THE FIRST COUNTER IS BEING SENT AND LOW FOR OTHER COUNTERS; CHANGES ON THE FALLING EDGE OF LSB BCD1    BINARY              FROM THE COUNTER BOARD BCD2    CODED              DURING DATA OUTPUT; CONTAIN THE COUNT DATA SYNCHRONIZED TO BYC; BCD4    DIGITS             SENT MOST SIGNIFICANT DIGIT FIRST BCD8 <b>Outputs</b> S3      STATE 3            ACTIVE FOR ALL STATES EXCEPT SPM, S4 OR S5; GATES BCD DATA WITH ASCII HEADER (3X HEX) IF RDY AND TE TO THE BUS S4/     STATE 4            ACTIVE AFTER LSB TO GATE; MESSAGE UNIT DELIMITER TO THE BUS (SEPARATES COUNTER OUTPUTS) S5/     STATE 5            ACTIVE AFTER S4 OF LAST COUNTER OUTPUT; GATES ASCII LINE FEED AND EOI TO THE BUS (END MESSAGE) LB      LAST BYTE           ACTIVE AT THE END OF OUTPUT TO TERMINATE TALK MODE EO1     END OR IDENTIFY    DRIVES BUS COMMAND LINE EO1 (END MESSAGE) ST5/    RESTARTS           PULSE SENT TO THE COUNTER BOARD DURING STATE 5 IF RECYCLE IS SELECTED
<b>3) Talk Delay Generator</b> <b>Inputs</b> CK        CLOCK                FROM INTERNAL CLOCK ATN/    ATTENTION            BUS GENERATED MTA     MY TALK ADDRESS    FROM MY TALK ADDRESS LATCH <b>Outputs</b> TE/     TALK ENABLE        ACTIVE FOR TALK STATE TED     TALK ENABLE DELAY (A12-2)    SYNCHRONIZES BUS TO INTERNAL CLOCK FOR CORRECT TIMING			
<b>4) My Talk Address Latch</b> <b>Inputs</b> MA      MY ADDRESS        FROM MY ADDRESS DECODER D7/-D6/ DATA 7-8    BUS GENERATED = [10] DVAL    DATA VALID        FROM ACCEPTOR HANDSHAKE TIMING BYC     BYTE CLOCK        FROM SOURCE HANDSHAKE TIMING HWIT    HAVE IT            FROM SOURCE HANDSHAKE TIMING LB      LAST BYTE           FROM OUTPUT DATA SEQUENCER ABRT/   ABORT              FROM RESET CIRCUIT TON     TALK ONLY MODE    S20-6 ECOL    END OF COLLECT    FROM COUNTER BOARD <b>Outputs</b> RCE     READ CLOCK        OUTPUT TO COUNTER BOARD TO ENABLE RCL MTA     MY TALK ADDRESS    ACTIVE AFTER BUS COMMAND MTA: INACTIVE AFTER DTA OR UNT BUS COMMANDS; CLEARED ON LB AND HWIT			
<b>5) My Address Decoder</b> <b>Inputs</b> D1/-D5/ DATA 1-5    BUS GENERATED S20-1   ADDRESS            BUS ADDRESS SELECT SWITCHES: S20-5   SWITCHES        BINARY WEIGHTED - 1 to 16 NOTE: All switches "on" (address = 31) is not allowed <b>Outputs</b> MA      MY ADDRESS        ACTIVE FOR (D1/-D5/) = (S20-1 TO S20-5)			
<b>6) Serial Poll Mode Latch</b> <b>Inputs</b> D1/-D7/ DATA 1-7    BUS GENERATED DVAL    DATA VALID        FROM ACCEPTOR HANDSHAKE TIMING ABRT    ABORT              FROM RESET CIRCUIT <b>Outputs</b> SPM/    SERIAL POLL MODE    ACTIVE AFTER SPE COMMAND FROM THE BUS - D7-D2 = 001100 AND D1 = 01, INACTIVE AFTER SPD COMMAND - D7-D2 = 001100 AND D1-0			
<b>7) Service Request Logic</b> <b>Inputs</b> REM     REMOTE              FROM REMOTE LATCH SPM     SERIAL POLL MODE    FROM SERIAL POLL MODE LATCH TE/     TALK ENABLE        FROM TALK DELAY GENERATOR ECOL    END OF COLLECT    FROM COUNTER BOARD FOR ANY STOP COLLECT			
<b>9) Device Clear</b> <b>Inputs</b> DVAL    DATA VALID        FROM ACCEPTOR HANDSHAKE TIMING REM     REMOTE              FROM REMOTE LATCH D1/-D7/ DATA 1-7    BUS GENERATED <b>Outputs</b> DCL     DEVICE CLEAR        WHEN ENABLED SENDS A STOP PULSE TO THE COUNTER ON A DCL COMMAND FROM THE BUS D7-D1 = [0010100]			
<b>10) Remote Latch</b> <b>Inputs</b> CK        CLOCK                FROM INTERNAL CLOCK RSET     RESET                FROM RESET CIRCUIT MA      MY ADDRESS        FROM MY ADDRESS DECODER DVAL    DATA VALID        FROM ACCEPTOR HANDSHAKE TIMING D6/-D7/ DATA 6-7    BUS GENERATED D7-D6 = [10 OR 01] <b>Outputs</b> REM     REMOTE              ACTIVE AFTER HAVING RECEIVED MY LISTEN OR MY TALK ADDRESS FROM THE BUS; INACTIVE AFTER RSET			
<b>11) Reset Circuit</b> <b>Inputs</b> IFC/     POWER ON            ACTIVE AT POWER ON TON     INTERFACE CLEAR    BUS GENERATED REN/    TALK ONLY           FROM S20-6 REMOTE ENABLE    BUS GENERATED <b>Outputs</b> ABRT/   ABORT              ACTIVE AT POWER ON OR DURING IFC; CLEARS MY TALK ADDRESS AND SERIAL POLL MODE LATCHES RSET/    RESET              ACTIVE AT POWER ON OR DURING REN; RESETS ALL HANDSHAKE CIRCUITS AND THE REMOTE LATCH; IF TON SELECTED, MONITORS REN/ TO PREVENT BUS CONFLICT WITH AN ACTIVE CONTROLLER			
<b>12) Internal Clock</b> THE CLOCK CIRCUIT GENERATES THE TIMING FOR PROPER OPERATION OF INTERNAL AND EXTERNAL CIRCUIT REQUIREMENTS Positive Interval — GREATER THAN 3 μsec Negative Interval — GREATER THAN 1 μsec			

### 7.10 TYPICAL BUS INTERCHANGE

It is not the intent of this section to be a primer on how the GPIB controller must be programmed. Each of these have unique characteristics and must be studied in detail. There are also several tutorial publications available from Hewlett Packard, Teletronix and Fluke as well as the IEEE. The following descriptions illustrate how the 2071A will respond in the modes that it will be most commonly used.

#### Serial Poll

This allows the controller to determine which device requires service. The 2071A will output a Service Request

(SRQ) when it stops counting. The controller may then perform a Serial Poll (SPE) to determine who is requesting service. During the polling sequence, the controller will assign each of the devices to be polled Talk address, and then the device will put out a Status-byte. If the 2071A is requesting service it will output a 42<sub>H</sub>, and remove its Service Request. If it was not the requesting device, then it outputs a status equal to 0. The controller completes the serial poll mode by doing a Serial Poll Disable (SPD). If the 2071A is the only possible source of the Service Request, the controller can choose to respond by Reading the data from the module; this will also clear its Service Request.

<u>Source</u>	<u>7-bit Hex Code</u>	<u>ATN Status</u>	<u>Description</u>
<b>Device Clear</b>			
Controller	14	ATN Asserted	Will cause 2071A to terminate counting if jumper B installed in GPIB interface.
<b>Read Data</b>			
Controller	3F	ATN Asserted	Unlisten all devices
Controller	35	ATN Asserted	Assign Listener at decimal address 27 <sup>3</sup>
Controller	44	ATN Asserted	Assign Talker at decimal address 4 <sup>4</sup>
2071A	30	ATN False	10 <sup>7</sup> digit from counter A equals 0
2071A	30	ATN False	10 <sup>6</sup> digit from counter A equals 0
2071A	38	ATN False	10 <sup>5</sup> digit from counter A equals 8
2071A	31	ATN False	10 <sup>4</sup> digit from counter A equals 1
2071A	36	ATN False	10 <sup>3</sup> digit from counter A equals 6
2071A	32	ATN False	10 <sup>2</sup> digit from counter A equals 2
2071A	39	ATN False	10 <sup>1</sup> digit from counter A equals 9
2071A	37	ATN False	10 <sup>0</sup> digit from counter A equals 7
2071A	0D <sup>1</sup>	ATN False	Carriage return
2071A	39	ATN False	10 <sup>7</sup> digit from counter B equals 9
2071A	38	ATN False	10 <sup>6</sup> digit from counter B equals 8
2071A	37	ATN False	10 <sup>5</sup> digit from counter B equals 7
2071A	36	ATN False	10 <sup>4</sup> digit from counter B equals 6
2071A	35	ATN False	10 <sup>3</sup> digit from counter B equals 5
2071A	34	ATN False	10 <sup>2</sup> digit from counter B equals 4
2071A	33	ATN False	10 <sup>1</sup> digit from counter B equals 3
2071A	32	ATN False	10 <sup>0</sup> digit from counter B equals 2
2071A	0D <sup>1</sup>	ATN False	Carriage return
2071A	0A <sup>2</sup>	ATN False	EOI Asserted, Line Feed

#### Note:

1. The carriage return indicating end-of-word may be switch selected to output a form feed (code 0C).
2. The line feed and EOI indicate to the controller that the 2071A presently talking is now finished sending data.
3. 27<sub>10</sub> is the address of the device which is to receive the 2071A's data.
4. 4<sub>10</sub> is the 2071A's address in this example with its channel A and B counters equal to 816297 and 98765432, respectively.

**BASIC WARRANTY**

Equipment manufactured by Canberra Industries, Inc. is warranted against defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in the instruction manuals. During the warranty period, repairs or replacement will be made at Canberra's option on a return to factory basis. The transportation cost, including insurance, to and from Canberra, is the responsibility of the Customer except for defects discovered within 30 days after receipt of equipment where shipping expense will be paid by Canberra to and from Canberra.

The customer must obtain an authorized customer service return number before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty.* In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment.

The Canberra Basic Warranty applies only to equipment manufactured by Canberra which is returned to the factory. If equipment must be repaired at the customer's site, the actual repair labor and parts will be provided at no charge during the warranty period. However, travel expenses to and from the customer's site, (travel time labor, and living expenses while on site), shall be paid by the customer unless an On-Site Warranty Option has been purchased. This option may only be purchased prior to shipment of the equipment to the customer.

The express warranties set forth herein are the only warranties with respect to the products, or any materials or components purchased from others and furnished by Canberra, and there are no other warranties, expressed or implied. The warranty of merchantability is expressly limited as herein provided and all warranties of fitness are expressly disclaimed and excluded. Canberra shall have no liability for any special, indirect or consequential damages, whether from loss of production or otherwise, arising from any breach of warranty hereunder or defect or failure of any product or products sold hereunder.

**EXCLUSIONS**

Warranty service is contingent upon the proper use of all equipment and does not cover equipment which has been modified without Canberra's written approval or which has been subjected to unusual physical or electrical stress as determined by Canberra Service personnel. Canberra Industries shall be under no obligation to furnish warranty service (preventive or remedial): (1) if adjustment, repair or parts replacement is required because of accident, neglect, misuse, failure of electrical power, air conditioning, humidity control, transportation, or causes other than ordinary use; (2) if the equipment is maintained or repaired or if attempts to repair or service equipment are made by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by warm-up or by neutrons or heavy charged particles. Damage from these causes is readily identifiable as described in the manual accompanying each detector.

Although Canberra may frequently supply, as part of systems, equipment manufactured by other companies, the only warranty that shall apply to such non-Canberra equipment is that warranty offered by the original manufacturer, if any.

Canberra will, upon request, offer, as an option, warranty coverage for non-Canberra equipment such as computers and peripherals sold as part of a system supplied by Canberra. Quotations on this coverage may be obtained by contacting Canberra Customer Service or any of our sales staff.

**SOFTWARE**

Canberra warrants software media from defects discovered within 30 days after receipt.

Canberra assumes no responsibility for user-written programs or programs published as part of information exchange in Canberra periodicals.

Engineering assistance for software development is available and can be contracted through the Sales Department.

**INSTALLATION**

Installation of equipment purchased from Canberra shall be the sole responsibility of the customer unless the installation is specifically contracted for at the prevailing Canberra field service rates. To insure timely

installation after receipt of equipment, it is recommended that installation be contracted for at the time the equipment is ordered.

**ON-SITE WARRANTY OPTION**

The On-Site Warranty Option provides for free on-site warranty work (Canberra pays all travel and living expenses) within the first 90 days after delivery of equipment to the customer. If installation is ordered from Canberra, the 90 day period commences upon completion of the initial installation. After the 90 day period, labor and materials used on site will still be covered by the basic warranty, but the customer shall pay for all travel expenses—travel time labor and living expenses incurred for any on-site service.

A maintenance contract may be purchased covering the period after the 90 days on-site warranty period, or after initial installation of the equipment. This is to be contracted through Canberra Customer Service.

**REPAIRS**

Any Canberra-manufactured instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. When returning instruments for repair, contact the Customer Service Department for shipping instructions and an Authorized Customer Service Return Number.

All correspondence concerning repairs should include the Model number and a description of the problem observed.

Once repaired, all equipment passes through our normal preshipment checkout procedure. Return shipping expense on out-of-warranty repairs will be charged to the customer.

For instruments out of warranty, the customer must supply a purchase order number for the repair before the item will be returned.

**SHIPPING DAMAGE**

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, immediately notify Canberra and the carrier making delivery, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in processing damage claims.

**Due to the delicate nature of cooled detectors [Ge(Li) and Si(Li)], Canberra requires that delivery to and from air freight terminals be handled with special care. Do not ship such Detectors without first obtaining advice from our Traffic Department.**

**RETURN SHIPMENTS**

Canberra Customer Service Department must be notified in advance if equipment is to be returned for any reason. Canberra can suggest the best means of shipping and will be able to expedite the shipment in case it is lost or delayed in transit.

The customer must obtain an authorized customer service return number before returning any equipment to the Canberra factory. *Compliance with this provision by the customer shall be a condition of this warranty.* In giving shipping instructions, Canberra shall not be deemed to have assumed any responsibility or liability in connection with the shipment.

Equipment should be returned to your area service center or to Canberra, Meriden. For shipment from outside the U.S., our shipping address is:

Kamino Air Transport, Inc.  
JFK International Airport, New York  
FOR: CANBERRA INDUSTRIES, INC.  
Meriden, Connecticut 06450 U.S.A.

**SERVICE AND SERVICEABILITY**

Canberra has gone to great lengths to insure that the instruments provided are functionally modular and therefore easy to service. In addition to modularity, Canberra has embarked on an extensive System Service Program to provide a totally responsive service capability. Complete Service Contracts with special arrangements for 24 hour response and weekend standby services are available from Canberra. For a detailed description of our Customer Service Program, please contact our Systems Service Department in Meriden, Connecticut, U.S.A.

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100



**DUAL COUNTER TIMER**  
**Model 2071A**

---

**Operator's Manual**

# Table of Contents

	Page		Page
<b>1. INTRODUCTION</b>		<b>7. THEORY OF OPERATION</b>	
1.1 Introduction.....	1	7.1 Eight Decade Counting Channel.....	15
<b>2. SPECIFICATIONS</b>		7.2 Crystal Based Time Generator.....	17
2.1 Inputs.....	1	7.3 Preset Counter.....	17
2.2 Input/Output.....	2	7.4 Six Decade Liquid Crystal Display.....	17
2.3 Front Panel Controls.....	2	7.5 Control.....	17
2.4 Performance.....	2	7.6 Power Supply.....	18
2.5 Internal Controls.....	2	7.7 Daisy Chain Option.....	18
2.6 Power.....	2	7.8 GPIB Interace Option (Talker).....	19
2.7 Physical.....	2	7.9 GPIB Option Functional Description.....	21
2.8 Option: 2071-01		7.10 Typical Bus Interchange.....	22
GPIB (IEEE 488) Interface.....	2		
2.9 Option: 2071-02			
Canberra NIM Daisy Chain Interface.....	3		
<b>3. CONTROLS AND CONNECTORS</b>			
3.1 Front Panel.....	4		
3.2 Rear Panel.....	5		
3.3 Jumper Options.....	5		
<b>4. OPERATION</b>			
4.1 Display Annunciators.....	7		
4.2 Preset.....	7		
4.3 Event Counter.....	7		
4.4 Time Counter.....	7		
4.5 Dual Counter.....	7		
4.6 Single/Recycle.....	7		
4.7 Reset.....	8		
4.8 System Operation.....	8		
4.9 Gate A and B.....	8		
4.10 Enable.....	8		
4.11 Overflow.....	8		
<b>5. DAISY CHAIN INTERACE</b>			
5.1 System Setup.....	9		
5.2 Printing System.....	9		
5.3 Computer Control.....	9		
5.4 Daisy Chain Jumper Options.....	9		
5.5 Typical Systems.....	10		
5.6 Using the Model 1488 Scanner.....	10		
5.7 Field Installation of the Daisy Chain Option.....	10		
5.8 Control In/Out Connectors.....	11		
<b>6. INTERACTION OF MODEL 2071A</b>			
with the GPIB			
6.1 General Description of GPIB.....	12		
6.2 GPIB Switches.....	12		
6.3 Systems without a Controller.....	12		
6.4 Interaction with a Controller.....	13		
6.5 Three Common Methods of Operation.....	13		
6.6 Field Installation of the GPIB Option.....	14		
6.7 Connector.....	15		
		<b>FIGURES</b>	
		3.1 Front Panel.....	4
		3.2 Rear Panel.....	5
		3.3 Internal Controls.....	6
		5.1 Daisy Chain Option Controls.....	10
		5.2 Control In/Out Connector Wiring.....	11
		6.1 GPIB Option Controls.....	12
		6.2 GPIB Connector Wiring.....	15
		7.1 Model 2071A Block Diagram.....	16
		7.2 GPIB Handshake Timing.....	20

## Section 1. Introduction

The Canberra Model 2071A Dual Counter/Timer provides, in a single width NIM module, two eight decade counters, a crystal time base, and presetting logic. Normal operation is as a preset timer and event counter, or as a preset event counter and timer. However, the Model 2071A may also operate as a dual counter plus preset timer without display of the preset data.

Both count INputs accept fast negative NIM or positive pulses, jumper selectable. A discriminator is provided allowing positive inputs to be compatible with unipolar and bipolar linear signals or TTL logic pulses. The front panel positive DISCriminator covers an input range of +100 mV to +10 V permitting selective counting, eliminating spurious counting from noise or other erroneous pulses.

The Model 2071A accommodates input counting rates of 100 million counts per second (100 MHz) for negative inputs and 25 million counts per second (25 MHz) for positive inputs.

The internal crystal time base provides increments of 0.01 seconds or 0.01 minutes, and live time gating at one microsecond resolution.

Display of either counter's content is accomplished with a six digit Liquid Crystal Display. The LCD includes eight annunciators which describe the display and dynamic state of the unit. Automatic x100 range shift provides an indication of the six most, or six least significant digits.

Preset control is accomplished with a three digit thumb-wheel switch providing a preset range from one to  $99 \times 10^4$  increments.

The SINGLE/RECYCLE mode switch provides a method to automatically place the unit or system back into the counting mode ten seconds or 100 microseconds, jumper selectable, after preset or termination of the count mode is reached.

Master-Slave system operation can be accomplished via the front or rear panel interconnection of the ENABLE signal, or by either of the two optional I/O interfaces.

The Canberra NIM Daisy Chain option provides interfacing to all Canberra printing counters, timers, and readout scanners. Standard with the NIM Daisy Chain option is a Read Out Buffer capability such that with any number of counting modules a total of only 100 microseconds dead time is required.

The alternate Canberra GPIB (IEEE-488) option provides interfacing to a GPIB bus, and allows a GPIB Controller to start, stop, and read out counting systems.

A convenient ENABLE output will allow the Model 2071A to start, stop, and reset single or multiple combinations of other Canberra Series 2000 counting modules.

For an accumulation of data in channel A, a jumper can be changed to prevent the resetting of channel A.

External connection to the A or B GATE inputs will permit gating of incoming pulses when in the preset count mode, and gating of the time base for channel A or B, jumper selectable, when in the preset time mode. In this mode the gate provides one microsecond resolution. Thus when a system busy signal is connected to this input, the Model 2071A will provide extremely accurate dead time corrections.

## Section 2. Specifications

### 2.1 INPUTS

A and B IN - Front panel BNC connectors accept positive linear, TTL, or negative NIM fast logic signals, jumper selectable. Positive operation accepts unipolar, bipolar, or TTL signals: amplitude: 0 to +10 V, +12 V maximum; input amplitude must exceed the adjustable discriminator level for 20 nsec to be counted. Negative NIM fast logic amplitude: -0.6 V to -1.6 V; minimum width 4 nsec below -0.6 V; input rise and fall times: 1 nsec to 300 nsec;  $Z_{in} = 1$  k ohms

dc for positive signals and  $\approx 50$  ohms for negative signals. GATE B - Counting control for channel B or time channel, jumper selectable; with time gate selected, 1  $\mu$ sec time resolution can be obtained; shipped as channel B counting control. Amplitude: +4 to +5 V or open circuit allows counting; zero to +0.8 V inhibits counting;  $Z_{in} = 100$  k ohms to +5 V bus. When used as time gating, system busy can be used for accurate dead-time correction.

## 2.2 INPUT/OUTPUT

**GATE A/ENABLE** - Front panel BNC connector having a multifunction capability; GATE A or ENABLE, internally selected with jumper plug; shipped in ENABLE position.

**GATE A** - With respect to channel A, same as GATE B.  
**ENABLE** - Bidirectional as input or output, open collector function, logic "0" OR; sinks 20 mA, sources from 4.7 k ohm to +5 V bus.

As an Output - Provides counting control to other 2071A, 2072A or compatible modules; 0 to +0.8 V enables counting, +4 V to +5 V disables counting.

As an Input - 0 to +0.8 V enables counting mode; +4 V to +5 V or open circuit disables counting mode.

**ENB/OVF** - Rear panel BNC connector having a multifunction capability, ENABLE or OVERFLOW; internally selected with a jumper plug; shipped in the OVF position.

**OVF** - Outputs a +5 V pulse coincident with the eighth decade reset; rise and fall times < 200 nsec; width 0.3  $\mu$ sec nominal; dc coupled; sinks 5 mA, sources 2.5 mA at 2.5 V; internal jumper selects channel A or B as source. Shipped in the channel A position.

**ENABLE** - Bidirectional as input or output, open collector function, logic "0" OR; sinks 20 mA, sources from 4.7 k ohm to +5 V bus.

As an Output - Provides counting control to other 2071A, 2072A or compatible modules; 0 to +0.8 V level enables counting, +4 V to +5 V disables counting.

As an Input - 0 to +0.8 V enables counting mode; +4 V to +5 V or open circuit disables counting mode.

## 2.3 FRONT PANEL CONTROLS

**START/STOP** - Two-position momentary toggle switch initiates or terminates a counting sequence.

**RESET** - Manual push-button resets both counters to zero.

**SINGLE/RECYCLE** - Two-position toggle switch selects single or recycle mode of operation upon reaching a preset condition.

**0.01 SEC/COUNT B/0.01 MIN** - Channel B time base or count selector; three-position toggle switch to select 0.01 seconds, 0.01 minutes, or the external B IN as the B counter and preset function. When time is selected, channel A counts external events through A IN. When Count B is selected, channel A counts time in 0.01 second intervals. An additional capability selected by internal jumpers provides a time preset, and event counting in channel A and B. In this case time is not available for display or readout.

**A/B DISPLAY SELECT** - Two-position toggle switch selects which counter's contents are displayed on the LCD.

**PRESET NM  $\times 10^P$**  - Three-digit thumbwheel switch for channel B preset. M is units, N is tens, P is the power of 10. N and M range from 0 to 9; P has a range of 0 to 6; N = M = 0 disables the Preset function.

## 2.4 PERFORMANCE

**CAPACITY** - Eight decades per channel, allowing  $10^8 - 1$  counts in each.

**COUNT RATE** - 100 MHz max., negative; 25 MHz positive.

**PULSE PAIR RESOLUTION** - 10 nanoseconds, negative; 40 ns positive.

**CRYSTAL TIME BASE ACCURACY** -  $\pm 0.0025\%$  over operating temperature range.

**TEMPERATURE OPERATING RANGE** - 0 to 50°C.

**PRESET COUNT CHANNEL** - Limited to 1 MHz count rate; pulse width minimum 300 nsec.

**INDICATORS** - Six digit Liquid Crystal Display with auto (x100) shift for displaying six most-significant digits. Eight annunciators on LCD describe the display. These are: OF (overflow), x100, CNT, MIN, SEC, A, B, decimal point. Active counting is indicated by CNT, MIN, or SEC blinking. Leading zeroes are suppressed.

## 2.5 INTERNAL CONTROLS

**STANDARD JUMPERS** (When set, perform the following):

- Inhibit reset of channel A when starting. In this mode channel A accumulates counts and is reset only by the manual pushbutton.
- Select OVERFLOW or ENABLE as the function of the rear panel connector.
- Select OVERFLOW output from channel B instead of channel A.
- Permit counting in both channels. In this mode the module may still be preset on time, but the time cannot be read out.
- Allow a pulse on ENABLE INPUT to start the module.
- Change recycle time from 10 sec to 100  $\mu$ sec.
- Select GATE A or B to gate the time channel.
- Select GATE A or ENABLE as the function of the front panel connector.
- Select input A and B to accept positive linear and TTL, or negative NIM signals.

## 2.6 POWER

2071A Alone	with -01	with -02
+12 120 mA	155 mA	123 mA
-12 200 mA	235 mA	203 mA
+24 35 mA	35 mA	35 mA
-24 0	0	0

## 2.7 PHYSICAL

**SIZE** - Standard single width NIM module; 3.43  $\times$  22.12 cm (1.35  $\times$  8.71 inches) per TID-20893 (rev. A)

**NET WEIGHT** - 0.94 kgs (2.0 lb.)

**SHIPPING WEIGHT** - 3.2 kgs (7.0 lb.)

## 2.8 OPTION: 2071-01

### GPB (IEEE 488) INTERFACE

#### A. Features

- Asynchronous ASCII data transmission bit parallel, character serial
- Uniquely addressable, switch controlled
- Talk/Listen mode
- Talk Only mode
- Auto recycle minimizes readout dead time
- Field installable
- Form feed or carriage return at end of word

#### B. Description

The General Purpose Interface Bus links a Canberra NIM counting module into the IEEE 488 standard communications network. As a Listener, this interface receives Start, Stop, and Readout commands from a controller. As a Talker, it supplies its accumulated data to a peripheral device. A Talk Only mode provides a controllerless means for a single module to read out to a peripheral Listener. The Auto Recycle mode allows the selected module to place itself (and the rest of the Canberra counting system) back into the count mode at the conclusion of its readout, thus minimizing system dead time. A side panel cutout provides

access to Set or Verify a Talk/Listen Address, select Talk Only mode, enable Auto Recycle, or select Form Feed/Carriage Return at the end of a word. This interface is a single PC board with a connector that allows convenient field installation.

#### C. Specifications

**SIGNALS** - The input/output signals on the GPIB connector are TTL compatible. True equals 0 to + 0.4 V, False equals + 2.5 to + 5 V.

**CONTROLS** - Side-panel cutout provides access to:

- Address select switches (5)
- Talk-Listen/Talk Only switch
- Auto Recycle switch
- FF/CR switch

Internal jumper enables Stop command response (DC 2).

**CONNECTOR** - Standard GPIB connector on rear panel.

**CONFORMITY** - Option 01 contains the following subset of capabilities (for explanation see IEEE-488 Standard) SH1, AH1, T1, TE0, L0, LE0, SR1, RL0, PP0, DT0, C0, DC0/DC2 selectable.

#### D. General Description of GPIB

The General Purpose Interface Bus is a link or network by which system components communicate with each other. Each system participant performs at least one of three roles: Controller, Talker, or Listener.

A Controller manages bus communications primarily by directing or commanding which devices are to send data to other devices (Talker), or receive data from other devices (Listener) during an operational sequence. A controller may also be interrupted or it may command specific action between devices.

The GPIB consists of 16 lines which are grouped into three sets according to function; there are 8 data lines, 3 control lines, and 5 general management lines. The 8 data lines carry ASCII characters (bit parallel) asynchronously; the control lines provide a data transfer handshake compatible with both slow and fast devices; the bus management lines allow initialization, interrupts, and special controls.

#### E. Cable

One Canberra Model C2071-2 GPIB Data/Control cable 0.6 m (2 feet) long is supplied for connection to the GPIB bus.

#### 2.9 OPTION: 2071-02

##### CANBERRA NIM DAISY CHAIN INTERFACE

#### A. Features

- Synchronous BCD data transmission bit parallel, character serial
- Readout sequence determined by interconnect order
- Field installable
- System control via individual Start, Stop, and Reset signals
- Compatibility with Canberra counters and scanners
- Read Out Buffer

#### B. Description

The Canberra NIM Daisy Chain Interface Option provides the basic 2071A module with a readout/control capability compatible with previous Canberra data-acquisition series modules.

Read Out Buffering is available by moving jumper DD to position CC. This sets the Recycle time to 100 microseconds and only needs to be carried out on the 2071A selected as Master. Operating the Master, and hence the entire system, in the Recycle mode provides a minimal (100 microsecond) dead time buffered counting system.

The problem of data transfer from the eight digit 2071A to the standard six-digit system is handled by a toggle switch on the interface board. It selects either the six most-significant digits or the least-significant digits. Two digits are lost in either case.

Control signals, Start, Stop, and Reset are received only if the unit is to be a system slave. A master unit will generate Start, Stop, and Reset. This logic is under internal jumper control.

#### C. Signals

**CONTROL IN** - Accepts Start, Stop, Reset, and Print pulses (5 V negative going from + 5 V level, rise time 500 nanoseconds maximum, width 1.0 microseconds minimum. Also HOLD command (dc level change from + 5 V to + 0.5 V maximum during printout) is accepted. Rear panel 15-pin "D" connector (Amphenol 17-10150).

**CONTROL OUT** - Provides Start, Stop, and Reset commands (5 V negative going pulses from + 5 V level, rise time 500 nanoseconds maximum, width 1.9 microseconds minimum). Data output information is presented in the form of Serial BCD (logic 1 = + 4 to + 5 V dc, logic 0 = 0 to + 0.5 V dc). This connector also provides the "next unit" Print command; eighth and successive Print command pulses are routed out via a logic gate. All control lines except Print command are wired directly between Control In and Control Out connectors. Rear panel 15-pin "D" connector (Amphenol 17-20150).

#### D. Controls

**SIGNIFICANT DIGIT SWITCH** ( $10^7 - 10^2/10^4 - 10^0$ ) -  $10^7 - 10^2$  position selects readout of the six most significant digits of the eight-digit word.  $10^4 - 10^0$  position selects readout of the six least significant digits of the eight-digit word. Jumpers allow the Model 2071A to act as a system master or as a slave.

#### E. Cable

One Canberra Model C1404-2 Data/Control cable 0.6 m (2 feet) long is supplied for connection to other Canberra data acquisition series modules.

## Section 3. Controls and Connectors

This section outlines the uses of the Model 2071A's controls and connectors. A complete listing of signal parameters will be found in Section 2, SPECIFICATIONS.

### 3.1 FRONT PANEL

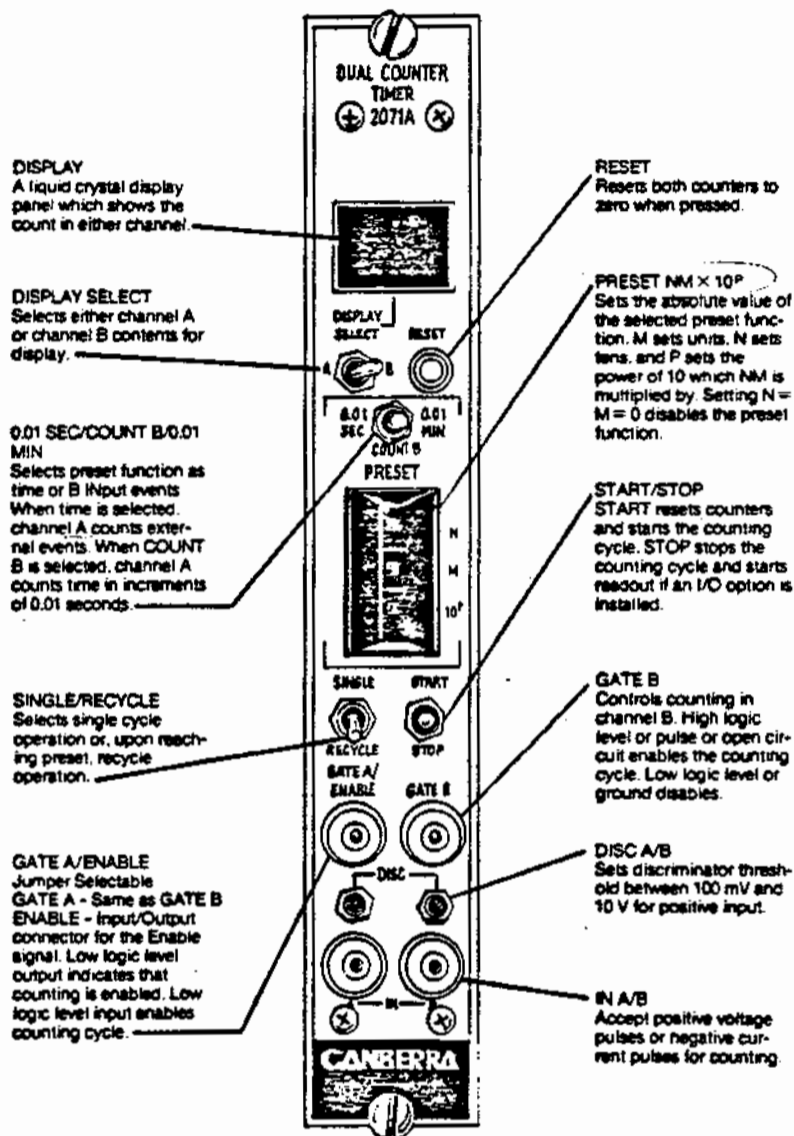
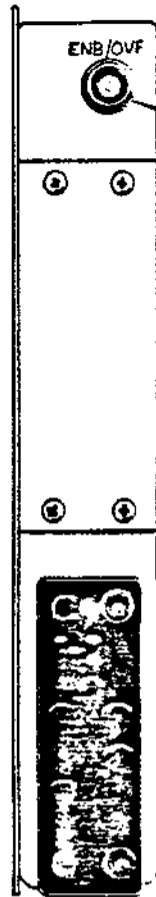


Figure 3.1  
Front Panel

### 3.2 REAR PANEL



ENB/OVF  
 Jumper Selectable  
 ENABLE - Input/Output  
 connector for the Enable  
 signal. Low logic level  
 output indicates that  
 counting is enabled. Low  
 logic level input enables  
 counting cycle.  
 OVERFLOW  
 Provides a positive logic  
 pulse when the  $8 \times 10^7$   
 counter bit resets in  
 channel A.

Figure 3.2  
 Rear Panel

### 3.3 JUMPER OPTIONS

The Model 2071A jumpers are defined as follows:

Jumper	Function	Jumper	Function
A*	Allows the GATE B signal to enable counter B	W*	Allows ENABLE dc level to start and stop count
B	Prevents the GATE B signal from disabling counter B	Z	Allows ENABLE pulse's falling edge to start count
C*	Allows the GATE A signal to enable counter A	X	Disables LCD annunciator CNT for Dual Counting
D	Prevents the GATE A signal from disabling counter A	Y*	Enables LCD annunciator CNT
E*	Enables counting in channel A	1*	Enables LCD annunciator SEC
F	Enables counting in channel B	2	Disables LCD annunciator SEC for Dual Counting
U	Enables Dual Counting	3*	Enables LCD annunciator MIN
G*	Allows the logic to reset channel A	4	Disables LCD annunciator MIN for Dual Counting
H	Prevents the logic from resetting channel A	5*	Enables channel A live time gating
J*	Channel A provides OVERFLOW signal	P	Enables channel B live time gating
K	Channel B provides OVERFLOW signal	6	Disables live time gating
N*	Enables preset select. time or counts	CC	Selects 100 $\mu$ sec recycle time
T	Enables only preset time for Dual Counting	DD*	Selects 10 sec recycle time
R	Selects front panel GATE A function		
S*	Selects front panel ENABLE function		

\*Indicates factory set position

Jumper	Function
EE	Selects rear panel ENABLE function
FF*	Selects rear panel OVERFLOW function
AP*	Selects positive A input
AN	Selects negative A input
BP*	Selects positive B input
BN	Selects negative B input

\*Indicates factory set position.

- To enable the Unit as a dual counter:  
move jumper F to position U  
move jumper 1 to position 2  
move jumper 3 to position 4  
move jumper N to position T
- To disable logic reset of channel A and use manual reset only:  
move jumper G to position H
- To change live time gating:  
move jumper 5 to position 6 to disable  
move jumper 5 to position P to change from channel A to channel B
- To disable the gate signal to channel A:  
move jumper C to position D
- To disable the gate signal to channel B:  
move jumper A to position B
- To change the Overflow output from channel A to channel B:  
move jumper J to position K
- To change rear panel OVERFLOW to ENABLE:  
move jumper FF to position EE
- To change front panel ENABLE to GATE A:  
move jumper S to position R
- To change A Input from positive to negative (NIM) input:  
move jumper AP to position AN
- To change B Input from positive to negative (NIM) input:  
move jumper BP to position BN
- To change recycle time from 10 seconds to 100 microseconds:  
move jumper DD to position CC
- To allow the falling edge of the ENABLE input pulse to place the Unit in count:  
move diode W to position Z:  
be sure to orient the diode with the band toward the bottom of the board

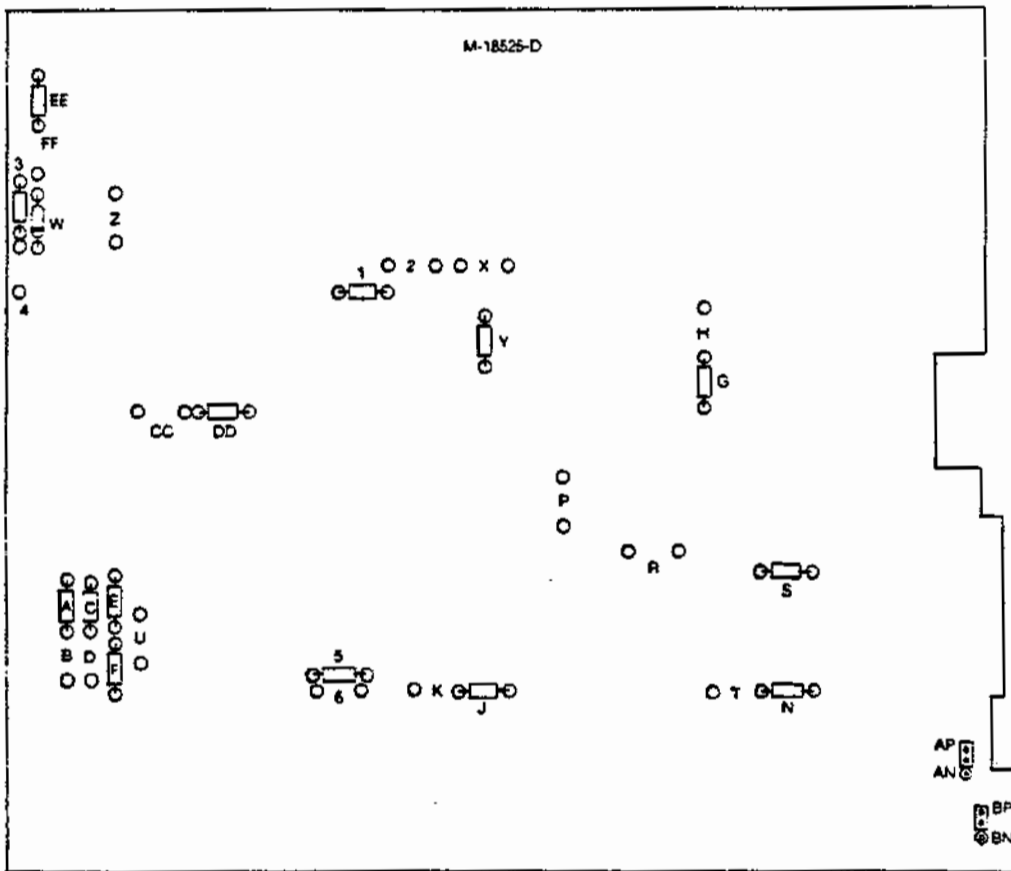


Figure 3.3  
Internal Jumpers



## Section 4. Operation

The Model 2071A Dual Counter-Timer can be used as an event counter with a time preset, as a timer with a preset on a selected number of events, or, with internal jumper changes, as a dual counter preset on time. In the latter mode, time is not displayed or read out.

The unit will accept positive voltage logic pulses or negative current pulses (jumper selectable). Positive inputs are normally clamped to + 5 V and will see a nominal input impedance of 1k ohms. Negative inputs see a nominal 50 ohm input impedance.

### 4.1 DISPLAY ANNUNCIATORS

The liquid crystal display panel has, in addition to numerals to display counter contents, eight annunciators which describe the display's readout and the dynamic state of the unit.

- X100** Shows that the six most significant digits are being displayed.
- OF** Shows that the displayed channel has overflowed and is counting up from zero again.
- CNT** Shows that the selected channel is displaying counts. Blinks when the channel is active.
- A/B** Shows which channel's contents are being displayed.
- MIN** Shows that time, counted in minutes, is being displayed. Blinks when the channel is active.
- SEC** Shows that time, counted in seconds, is being displayed. Blinks when active.

The eighth annunciator is a decimal point.

### 4.2 PRESET

The preset condition is set with the 0.01 SEC/COUNT B/0.01 MIN preset select switch and the three thumbwheel switches, N, M, and  $10^P$ . Selecting 0.01 SEC or 0.01 MIN will enable the unit to be used as an event counter with the time preset in increments of 0.01 seconds or 0.01 minutes (0.6 seconds). Setting  $N = M = 0$  disables the preset function.

Selecting COUNT B will enable the unit to be used as a timer with a preset on a number of counts.

If the unit is to be changed to a dual counter, the time preset, either 0.01 seconds or 0.01 minutes, will be used but not displayed.

The thumbwheel switches are used to select the number of preset units as chosen by the preset select switch. The M switch sets the units of the preset, the N switch sets the tens, and the  $10^P$  switch sets the power-of-ten multiplier.

For instance, if the switches are set to  $N = 1$ ,  $M = 0$ ,  $P = 3$  and the preset select switch is in the 0.01 SEC position, the time preset will equal  $10 \times 10^3$  hundredths of a second, or 100 seconds. If the select switch is in the 0.01 MIN position, the preset will equal  $10 \times 10^3$  hundredths of a minute, or 100 minutes. If the select switch is in the COUNT B position, the preset will equal  $10 \times 10^3$  counts, or 10 000 counts.

### 4.3 EVENT COUNTER

To use the Model 2071A as an event counter, INput A receives the external events to be counted. The 0.01 SEC/COUNT B/0.01 MIN switch must be placed in one of the time positions and the PRESET thumbwheel switches must be set for the desired time preset, as explained in section 4.2.

Pressing the START/STOP switch to START will start data accumulation. When the preset is reached, channel A will contain the total counts accumulated and channel B will contain the time during which the counts in channel A were accumulated. The time shown will equal the preset time.

To display the contents of either channel, move the DISPLAY SELECT switch to either A or B. Only one channel will be displayed at a time. The annunciators on the liquid crystal display will show either CNT (counts) or SEC or MIN (the selected time preset).

### 4.4 TIME COUNTER

To use the Model 2071A as a time counter, the channel B INput receives the external events to be counted and channel A records elapsed time in increments of 0.01 seconds.

In this mode, the preset select switch is placed in COUNT B and the PRESET switches can be set to stop the counting cycle at the selected number of counts. Channel A will show the time that it took to record the preset number of events.

### 4.5 DUAL COUNTER

By changing internal jumpers as outlined in Section 3.3.1, both channel A and channel B can count external events up to a preset time, either in 0.01 second or 0.01 minute increments as defined by the setting of the preset select switch and of the PRESET switches. In this mode, the time is not displayed or read out.

### 4.6 SINGLE/RECYCLE

With the SINGLE/RECYCLE switch in the SINGLE position, the counter, once started, will count to preset and stop. If the switch is moved to the RECYCLE position, the counter will count to preset, pause 10 seconds or 100  $\mu$ sec as selected by jumper CC/DD, clear the counters and start counting again. The recycle mode will continue until manually stopped, by setting the SINGLE/RECYCLE switch to SINGLE and pressing STOP.

#### 4.7 RESET

At any time, even during a count cycle, pressing the RESET button will clear both counters to zero. If a counting cycle is in progress, it will resume as soon as the RESET button is released.

In the RECYCLE mode, the counters are automatically reset at start-of-count. By changing an internal jumper, channel A automatic reset can be inhibited. In this mode, channel A can be reset only by pressing the RESET button. See Section 3.3.2.

The RESET button also functions as a display check. When the button is pressed, the display will show all "eights." Therefore, holding the button down will allow the operator to verify that the display is functioning correctly.

#### 4.8 SYSTEM OPERATION

Several of the Series 2000 counting modules can be configured in a Master/Slave relationship by connecting their ENABLE connectors in parallel with 93 ohm coaxial cable (type RG-62), using female-female-female "tee" connectors between the cable segments.

When the system is connected in this way, pressing START on one unit will start all units together.

The Master unit in the system is the one whose START button has been pressed, all other units are Slaves. Note that in this mode, the Slave presets are disabled. The Master unit's preset will control the entire system. Pressing STOP on the Master will stop all units together.

Either of the input/output options may also be used to set the system up in the Master/Slave mode. See Sections 5 and 6 for details.

#### 4.9 GATE A AND B

The GATE A function is available on the front panel GATE A/ENABLE connector. The factory set internal jumper must be moved from the ENABLE position to the GATE A position to allow GATE A inputs. See Section 3.3.8.

The GATE connectors accept positive logic pulses or a dc level to enable counting in either channel. Internal jumpers may be moved to disable the function for either channel or both channels. See Sections 3.3.4 and 3.3.5.

A logic high signal (+4 to +5 V) or an open input will enable counting; a logic low signal (0 to +0.8 V) will disable counting.

The gating signal gates the crystal-controlled time base, giving a gating time resolution of 1  $\mu$ sec. Using channel A as the event counter and channel B as the timer counter, a system-busy signal may be connected to the GATE A input to disable counting and the timer for accurate dead time correction. By moving an internal jumper, Time gating can be done with GATE B or can be defeated; see Section 3.3.3.

#### 4.10 ENABLE

The ENABLE function is available on both the front and rear panel. The front panel GATE A/ENABLE connector is

factory set to the ENABLE position. To select the front panel GATE A function, see Section 3.3.8. The rear panel ENB/OVF (ENABLE or OVERFLOW) connector is factory set to the OVERFLOW position. To select rear panel ENABLE function, see Section 3.3.7.

The ENABLE connector provides a logic low output (0 to 0.8 V) when the unit is enabled for counting. This output can be used to signal another unit that the Model 2071A is active. For instance, when using the Model 2071A as the Master unit in the Master/Slave System outlined in Section 4.8.

The ENABLE connector can also receive a logic low pulse to enable the Model 2071A for counting. For instance, as a Slave unit in the Master/Slave System.

To increase the Enable line's flexibility, an internal jumper (W) has been provided. If this jumper is moved to the Z position (see Section 3.3.12), the falling edge of an input pulse on the ENABLE connector will start the unit's counting cycle.

When the unit is started in this way, it is the Master unit in the system. The Enable line will be held low by this unit until its preset is reached, thus enabling all other units in the system.

If the Model 2071-02 Daisy Chain Interface is installed, it will not be necessary to use the Enable line. The Interface has all necessary signals to start and stop the unit.

If the Model 2071-01 GPIB Interface is installed, the Enable line will be used if the entire system is to start and stop at the same time. If the GPIB Controller is to address each unit separately, the Enable line will be used only if each individually addressed unit is the Master unit in separate sub-systems.

An internal jumper can be moved to change the front panel ENABLE function to GATE A. See Section 3.3.8.

#### 4.11 OVERFLOW

The OVERFLOW function is available at the rear panel ENB/OVF (ENABLE or OVERFLOW) connector which is factory set to the OVERFLOW position.

The rear panel OVERFLOW connector provides a positive logic pulse every time that channel A exceeds its count capacity ( $10^4$  counts). This signal can be connected to the input of another counter to extend the counting capacity of the system.

If the Model 2071A is used in the dual counter mode, the OVERFLOW signal can be connected to the B INput, instead of another counter, to extend the counting capacity of the system.

An internal jumper can be changed to allow the overflow of channel B to generate the OVERFLOW signal. See Section 3.3.6.

## Section 5. Daisy Chain Interface

The Model 2071-02 Daisy Chain Interface option provides both data input/output and system control. It is compatible with all existing Canberra Daisy Chain Systems.

The CONTROL IN and CONTROL OUT connectors present all Bus commands, with the exception of the Print clock, in parallel to all units in the system. The Print clock is presented serially to one unit at a time.

Since the Model 2071A is an eight-digit counter and the Daisy Chain System is capable of recording only six digits, a switch has been included on the Interface Board to select output of either the six most significant digits ( $10^7 - 10^2$ ) or the six least significant digits ( $10^5 - 10^0$ ). Refer to Figure 5.1 for switch location.

The nature of the data collection being performed will define which six digits to include in the data output. The unit is shipped with the switch in the six least significant digits ( $10^0 - 10^5$ ) position.

### 5.1 SYSTEM SETUP

A system of up to 50 data input modules and one scanner are connected with Model C-1404 cables. One 60 cm (two foot) cable is included with each Model 2071-02.

The CONTROL OUT connector of each unit is connected to the CONTROL IN connector of the next unit in the system. The last unit in the system is connected back to the scanner.

The system Master unit is defined as the one on which the START control is pressed. All other units are then Slave units.

When the Master unit is started, it generates a System Start command on the Daisy Chain Bus, which starts all Slave units at the same time.

When any unit reaches its preset, it stops and generates a System Stop command on the Bus. All units will stop at the same time.

In the SINGLE count mode, the system will run through one data collection cycle and stop when preset is reached.

In the RECYCLE count mode, the system will start, stop when any unit reaches its preset, pause ten seconds or 100 microseconds (jumper selectable, see Section 3.3.11), clear all counters, and start counting again.

### 5.2 PRINTING SYSTEM

If a Model 2088 Printer Scanner (RS232), or a Model 2089 Serial Scanner-Printer is connected in the system, the data collected by each unit can be printed out. A Model 9182 EIA to 20 mA Current Loop Adaptor can be connected to the 2088 for 20 mA current loop operation.

Standard with the NIM Daisy Chain option is a read out buffer. By taking advantage of the buffer circuitry, system dead time can be reduced. In a Recycle Mode, the buffer allows the unit to be placed back into the counting mode after the data has been latched into the readout buffer. After 10 seconds or 100 microseconds, jumper selectable, counting resumes and read out begins. During the readout time, the display will not be updated, but correct counting will go on. As with most buffers, counting time must be longer than readout time.

The first unit in the system to print out will be the one connected to the Scanner's CONTROL OUT connector. The second unit to print out will be the one connected to the first unit. The last unit to print out will be the one connected to the Scanner's CONTROL IN connector.

### 5.3 COMPUTER CONTROL

The Model 2088 Printer Scanner can be used to allow a computer to control the system. Refer to the Model 2088's manual for details on computer system operation.

### 5.4 DAISY CHAIN JUMPER OPTIONS

The Daisy Chain option board has four jumpers which will allow the user to tailor the option for specific applications. Three of these jumpers are 4.7k ohm resistors; the fourth is a 2.7 ohm resistor. Refer to Figure 5.1 for jumper locations.

1. Jumper A allows the Enable pulse's rising edge or the Model 2071A's control logic to generate the Daisy Chain Bus STOP command.

In the B position, this unit will not generate the STOP command.

2. Jumper C allows the Enable pulse's falling edge or the Model 2071A's control logic to generate the Daisy Chain Bus START command.

In the D position, this unit will not generate the START command.

3. Jumper E allows the Enable pulse's falling edge or the Model 2071A's control logic to generate the Daisy Chain Bus RESET command.

In the F position, this unit will not generate the RESET command.

4. Jumper G allows the Model 2071A's front panel RESET control to generate the Daisy Chain Bus RESET command.

In the H position, manual Reset will not generate the RESET command.

Please be aware that these jumpers do not need to be changed to make this unit a Slave unit. Slave status is normally defined by system operation.

If any or all of these jumpers were to be changed to their optional positions, this unit would be permanently defined as a Slave unit. It would never become a system Master unit until the jumpers were changed back to their usual setting.

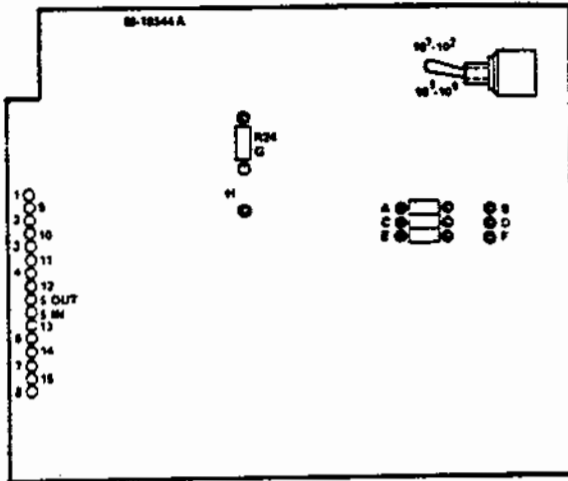
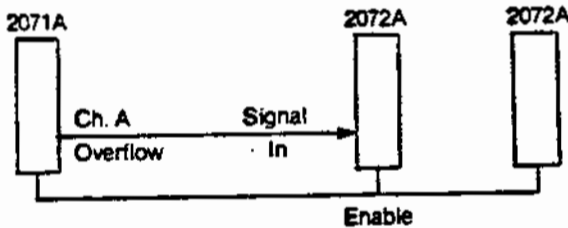


Figure 5.1  
Daisy Chain Option Controls

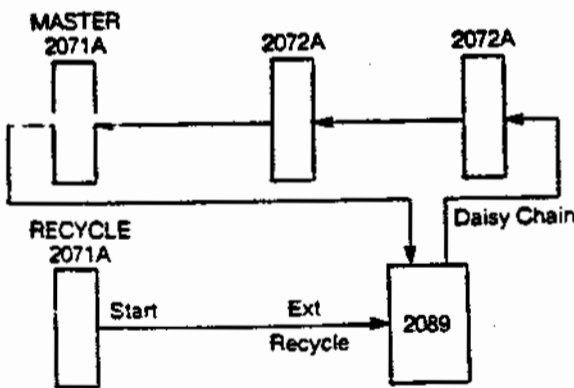
### 5.5 TYPICAL SYSTEMS

The following figures show some of the possible system setups.

1. Multi-input system with preset time and ability to count overflow from channel A of the 2071A.

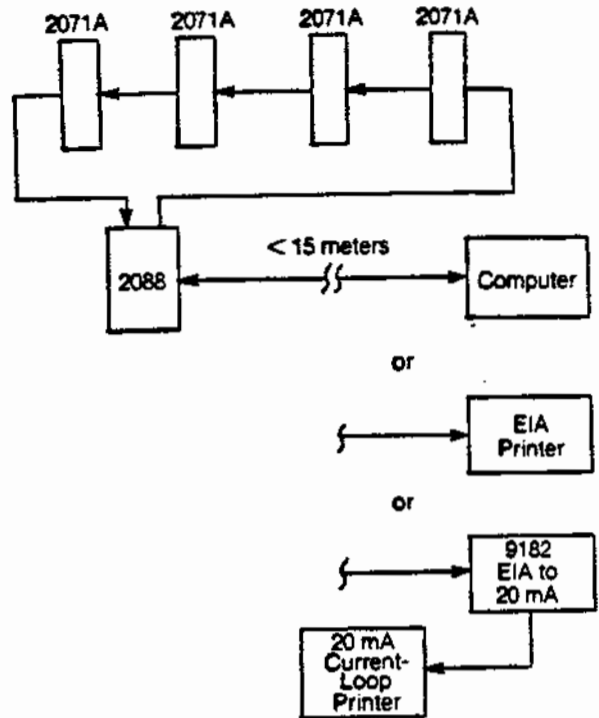


2. Multi-input 100 MHz Daisy Chain Printing System - preset controlled by master 2071A, recycle time controlled by 2071A. Printout from 2089 printer lists preset time and contents of 5 counters.



Note: The Model 2071A will require a factory modification (SERF) in order to operate with the Model 2089 External Recycle.

3. Multi-input 100 MHz Daisy Chain system with individual preset time for each counter. Slaves must reach preset before master. For this system, slaves are defined by changing the -02 option's internal jumpers (See Section 5.4).



### 5.6 USING THE MODEL 1488 SCANNER

If a Model 1488 Scanner is to be used instead of the Model 2088, the 1488 PRINT MODE switch must be set to PROMPT.

In the DELAYED mode, the HOLD command is not normally asserted until after the TTY motor-start time out, which will not allow proper data buffering.

For proper operation in the DELAYED mode, open the 1488 and look for a 10 ohm resistor soldered to points A-B (refer to schematic B-12177). Unsolder the resistor from points A-B and solder it to points A-C. This will cause prompt generation of the HOLD command on receipt of the Daisy Chain's STOP pulse.

The 1488's FORMAT switch must be set to LINE. Setting the switch to CONTINUOUS will cause incorrect data to be read out.

### 5.7 FIELD INSTALLATION OF THE DAISY CHAIN OPTION

The Daisy Chain interface option consists of: four stand-offs, four lockwashers, 12 Phillips-head screws, the rear panel control connector plate, and the interface board.

To install the option, first remove both side covers, each of which is held in place by five Phillips-head screws. Then:

1. If they are not already installed, install the four standoffs in the four holes in the unit's printed circuit board.
2. The standoffs are to be placed on the component side of the board and fastened to the board with one lockwasher and one screw each.
3. Carefully place the interface board in the unit so that the line of small circular connectors is at the rear of the board.
4. With the interface board's four mounting holes lined up with the four standoffs, press the board gently down to mate the interboard connectors.
 

The interface board should mate smoothly with the unit's connector. If any resistance is felt, the connector is not properly aligned; lift the interface board up a little and realign the four mounting holes with the standoffs before pressing down again.
5. Fasten the interface board to the standoffs with four screws, one in each corner of the interface board.
6. Mount the control connector plate on the rear panel with the four remaining screws.
7. Carefully align the ribbon cable's pins with the sockets of J4 at the rear of the interface board.
8. Press the cable's pins firmly down into the connectors until the cable is flush with the tops of the connectors.
9. Place S1, the six-digit select switch, in the desired position.
10. Before replacing the side covers, check the installation for proper operation.

## 5.8 CONTROL IN/OUT CONNECTORS

PIN No.	FUNCTION	SIGNAL DESCRIPTION
1	BCD Data "1"	Logic 1 = +4V, Logic 0 = 0V
2	BCD Data "2"	Logic 1 = +4V, Logic 0 = 0V
3	BCD Data "4"	Logic 1 = +4V, Logic 0 = 0V
4	BCD Data "8"	Logic 1 = +4V, Logic 0 = 0V
5*	Print Clock	+5V 0V Pulse Train
6	System Hold	+5V +0.5V DC Level Change
7	System Stop	+5V 0V Pulse
8	System Start	+5V 0V Pulse
9	System Reset	+5V 0V Pulse
10	Display BCD "1"	Logic 1 = 0V, Logic 0 = +4V
11	Display BCD "2"	Logic 1 = 0V, Logic 0 = +4V
12	Display BCD "4"	Logic 1 = 0V, Logic 0 = +4V
13	Display BCD "8"	Logic 1 = 0V, Logic 0 = +4V
14	Display Clock	+5V 0V Pulse Train +12V
15	Ground	

Figure 5.2  
Control In/Out Connector Wiring

### NOTES:

All data and control lines except Print Clock line (pin 5) are internally wired directly between corresponding pins of the CONTROL IN and CONTROL OUT connectors.

The Print Clock pulse train from the Data Scanner will appear on pin 5 of the CONTROL OUT connector after module has finished printing its data contents.

The signals on pins 10 through 14 are not used by this unit.

## Section 6. Interaction of Model 2071A With the GPIB

### 6.1 GENERAL DESCRIPTION OF GPIB

The General Purpose Interface Bus is a link or network by which system components communicate with each other. Each system participant performs at least one of three roles: Controller, Talker, or Listener.

A Controller manages bus communications primarily by directing or commanding which devices are to send data to other devices (Talker), or receive data from other devices (Listener) during an operational sequence. A Controller may also be interrupted or it may command specific action between devices.

The GPIB consists of 16 lines which are grouped into three sets according to function; there are 8 data lines, 3 control lines, and 5 general management lines. The 8 data lines carry ASCII characters (bit parallel) asynchronously; the control lines provide a data transfer handshake compatible with both slow and fast devices. The bus management lines allow initialization, interrupts, and special controls.

### 6.2 GPIB SWITCHES

The eight-section DIP switch on the option board is accessible through the hole in the unit's side cover. The switches should be set to the desired positions before putting the unit in a NIM Bin. Refer to Figure 6.1.

The first five switches, counting from the top, are used to set the unit's GPIB address. Each switch is labeled with its value and with ZERO and ONE. The address is the sum of

all switches that are in the one position. An address of 31 (all switches in the ONE position) is illegal; it is reserved for the GPIB command UNTALK.

The sixth switch is labeled TALK ONLY. Refer to Section 6.3 for its uses.

The seventh switch is labeled RECYCLE. In the ON position, the unit will clear after readout and start counting again. In the OFF position, the unit is in the single cycle mode.

The eighth switch is labeled FF/CR. In the FF position, the message unit delimiter is sent out as an ASCII Form Feed. In the CR position, the delimiter is sent out as a Carriage Return. The choice of delimiter depends on the peripheral device being used.

### 6.3 SYSTEMS WITHOUT A CONTROLLER

The Model 2071A can operate in the Talk Only ON mode, which is used when data from a single module is to be passed directly to a single peripheral Listener device, such as a GPIB Printer. In this case a Controller is not required, but the printer must be in the Listen mode. Not all GPIB printers will operate in this mode.

In Talk Only ON mode, the 2071A will transmit its data to the listener as soon as 2071A data acquisition is stopped (by STOP or reaching Preset).

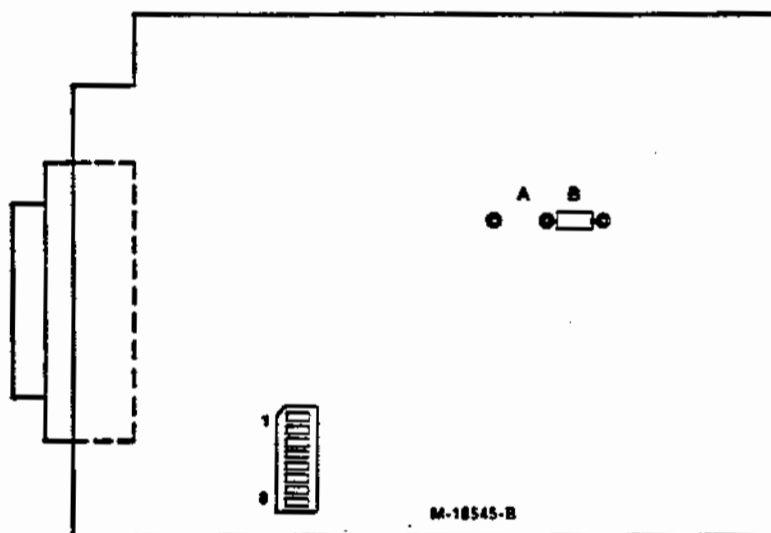


Figure 6.1  
GPIB Option Controls

#### 6.4 INTERACTION WITH A CONTROLLER

Communication with a Controller requires 2071-01's TALK ONLY switch to be off. The Controller must assert REN (Remote Enable) during the entire communication. If REN is disabled, the 2071-01 will be reset. The first requisite is for the Controller to cause the 2071A to be placed in its Remote mode. It does this by transmitting on the GPIB, MTA, (My Talk Address) or MLA (My Listen Address), with ATN (Attention) asserted. MTA or MLA must agree with the five-bit address setting on the 2071A. The following MTA or MLA would be sent if the address setting was 5.

	DI07	DI06	DI05	DI04	DI03	DI02	DI01
MTA	1	0	0	0	1	0	1
MLA	0	1	0	0	1	0	1

If MTA is sent, the unit goes into its Remote mode and transmits all of its data (19 bytes). If MLA is sent, the 2071A does not respond further than placing itself into the Remote mode. Once in the Remote mode, the unit is able to generate an SRQ (Service Request) or respond to a DC (Device Clear). Disabling REN causes the 2071A to leave the Remote mode.

A typical counting sequence would begin with the operator pressing START on a 2071A that is connected to the GPIB. After reaching a preset, the 2071A will generate SRQ. The Controller would then, via a Serial Poll, determine the device requiring readout. Then send the proper MTA to read the data by way of a Read Data Interchange (Section 7.10). If the module is in the Recycle mode (switch on GPIB interface set to Recycle), the counters will be reset after readout and the counting cycle will begin again.

Note that there are two Recycle switches, one on the unit's front panel, and one on the GPIB interface card. The front panel switch allows the user 10 seconds to manually copy the display (or just view it) between cycles. When the 2071A is connected to the GPIB, the front panel switch is normally set to Single, and the GPIB interface switch set to Recycle. The recycle time will now depend on the devices on the bus with which the module must interact.

The time required to read data from a Model 2071A is determined by the sum of the response times of the Computer/Controller and 2071A. The 2071A responds to each query or handshake request within seven microseconds. This means the 2071A requires a maximum of 14 microseconds for each byte outputted. The 19-byte readout consumes 266 microseconds of 2071A synchronizing time. A readout to one Controller was measured at 12.5 milliseconds. This equates to 644 microseconds to accept data and generate handshake responses per byte, or a ratio of Controller to 2071A of 46 to 1. It is apparent that the Controller is the major contributor to readout time.

Some additional capabilities are:

##### a. Controller Start

Since modules are independent, the Controller can start each module by performing a READ DATA Interchange (see Section 7.10). With a counter stopped and in a GPIB recycle mode, the completion of a READ DATA Interchange will cause it to clear and start counting. The controller can individually address each module for this sequence.

##### b. Controller Stop

The Controller can send a Universal DEVICE CLEAR out on the bus, and all modules will stop counting. Individual modules cannot be addressed with this command, and it will not clear the modules, only stop them. If internal jumper B is moved to A, the module will ignore the DEVICE CLEAR command (see Figure 6.1).

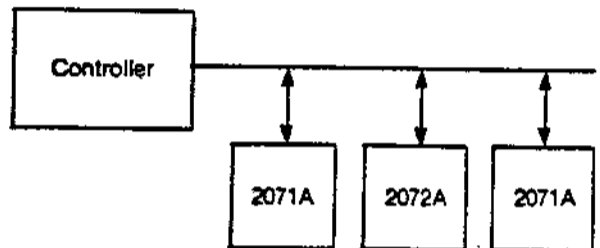
##### c. Read Out While Counting

The Controller can read out each individual 2071A or 2072A while it is counting by performing a READ DATA Interchange (see Section 7.10). In this case the module will be read out and will not clear, but continue counting. A point to remember here is that a module will clear itself only if it is restarted by:

1. A manual front panel START.
2. A manual front panel RESET.
3. An ENABLE signal input.
4. Being in a front panel RECYCLE mode and stopped either by reaching preset or by receiving a Device Clear from the Controller.
5. Being in a GPIB Recycle mode, stopped by reaching preset or receiving a Device Clear from the Controller, then read out by a READ DATA Interchange.

#### 6.5 THREE COMMON METHODS OF OPERATION:

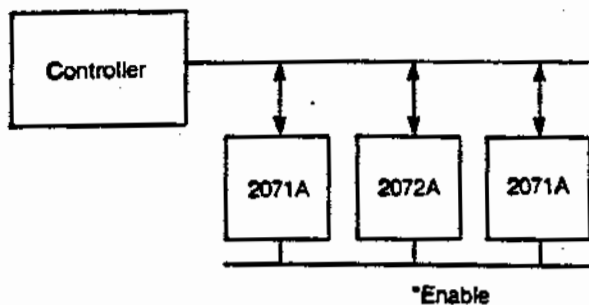
##### A. Controller completely controls modules.



Sequence:

1. Controller performs READ DATA Interchange to start the modules. Each one must be addressed individually by the Controller. Thus, in this case, a simultaneous start is not possible. Data read out the first time is information left by previous operations.
2. Controller sends a DEVICE CLEAR, when desired, to stop all counters. Individual addressing is not possible with this command. All counters will simultaneously stop.
3. Controller again addresses each module with a READ DATA Interchange. Since they are in the Recycle mode (they would not have started in the first step if they weren't) each one clears, and restarts after reading out.

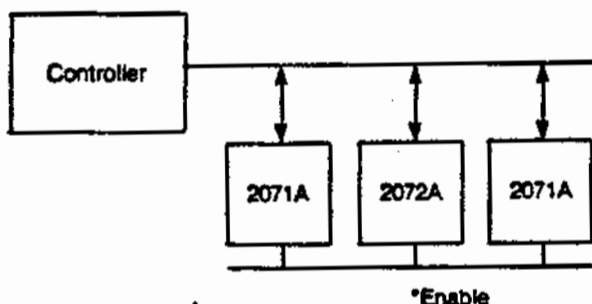
**B. Controller acts only as a readout device.**



**Sequence:**

1. ENABLE input/outputs on all modules are connected.
2. The START switch on one 2071A is pushed (this defines it as the Master).
3. All modules are stopped when the master reaches its preset.
4. Each module sends a SERVICE REQUEST when it stops if it was first commanded to REMOTE by the Controller.
5. The Controller addresses each module and reads it out.
6. If the Master is in the front panel RECYCLE mode, upon being read out it will enable the system to start counting again. All modules will have been cleared by the leading edge of the ENABLE signal. Normally the Master would be interrogated last so that it does not start the system until all other units have been read out.

**C. Controller initiates simultaneous start by addressing the master module.**

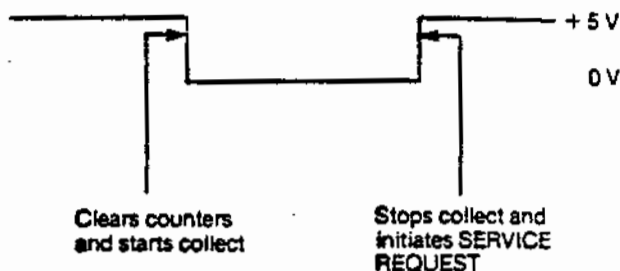


**Sequence:**

1. ENABLE input/outputs on all modules are connected.
2. Controller addresses first 2071A and reads it out. This defines it as the Master. Because it is in the GPIB Recycle mode it reads out, clears, and starts collecting. Since the ENABLE ports are connected, the other 2071A and 2072A modules clear and simultaneously start collecting. The Single/Recycle switch on each of their GPIB interface cards and front panel must be in the SINGLE mode.

3. When the preset on the Master 2071A is reached, it stops all modules, and each one generates a service request on the GPIB Bus. The Controller now interrogates each module. It should address the Master 2071A last, since this module is in the recycle mode and would start the system again once it is read out.

**\*The Enable Signal**



The modules on which the START switch is not pushed will ignore their presets and be controlled by the ENABLE signal. The Master module is defined as the module that has been started first, either manually or by being addressed from the Controller. Its preset will determine the presets for all other 2071As and 2072As.

**6.5 FIELD INSTALLATION OF THE GPIB OPTION**

The GPIB Interface option consists of: four standoffs, four lockwashers, 12 Phillips-head screws, a rear panel cover plate marked J102, and the interface board.

To install the option, first remove both side covers, each of which is held in place by five Phillips-head screws. Then:

1. If they are not already installed, install the four standoffs in the four holes in the unit's printed circuit board.
2. The standoffs are to be placed on the component side of the board and fastened to the board with one lockwasher and one screw each.
3. Carefully place the interface board in the unit so that the large connector at the rear of the board is flush with the rear panel.
4. With the interface board's four mounting holes lined up with the four standoffs, press the board gently down to mate the interboard connectors.

The interface board should mate smoothly with the unit's connector. If any resistance is felt, the connector is not properly aligned; lift the interface up a little and realign the four mounting holes with the standoffs before pressing down again.

5. Fasten the interface board to the standoffs with four screws, one in each corner of the interface board.
6. Place the J102 cover plate on the unit's rear panel and fasten it in place with the remaining four screws.
7. Before replacing the side covers, check the installation for proper operation.



## 6.7 CONNECTOR

A 24-pin standard GPIB connector (J102) is mounted on the rear panel. It carries the following signals:

Pin	Signal	Description
1	DIO1	Data I/O 1
2	DIO2	Data I/O 2
3	DIO3	Data I/O 3
4	DIO4	Data I/O 4
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready for Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	Shield	To earth ground
13	DIO5	Data I/O 5
14	DIO6	Data I/O 6
15	DIO7	Data I/O 7
16	DIO8	Data I/O 8
17	REN	Remote Enable
18		Twisted pair with pin 6
19		Twisted pair with pin 7
20		Twisted pair with pin 8
21		Twisted pair with pin 9
22		Twisted pair with pin 10
23		Twisted pair with pin 11
24		Signal Ground

Figure 6.2  
GPIB Connector Wiring

All GPIB signals are negative-true TTL compatible:

True = 0 to 0.4 V;

False = 2.5 to 5 V.

## Section 7. Theory of Operation

The Model 2071A includes two identical eight-decade counter channels, a crystal-based time generator, an eight-decade preset counter, a six-decade liquid crystal display, optional readout to a Canberra Daisy Chain Scanner or to a GPIB (IEEE 488) system, suitable control logic, and the power supply.

### 7.1 EIGHT DECADE COUNTING CHANNEL

Each of the identical counting channels has an input circuit which accepts positive voltage or negative current logic pulses on the same input connector (jumper selectable). Negative current-pulses see a 50 ohm impedance while the positive voltage-pulses see a nominal 1k ohm impedance.

With the A input jumper in the AP position, positive voltage signals are fed to the inverting input (pin 3) of comparator A58. A voltage divider consisting of R37, R42, and R43 along with clamping diodes D11 and D12 protect A58 from positive or negative over-voltages. When the positive input signal exceeds the threshold level set at A58-3 by R35 and front panel DISC A (RV2), A58-7 goes from  $\approx 5$  V to ground. This signal is fed through D10 to A56. Double counting with slow rise times is prevented by the feedback network consisting of R56, C20, and C21.

With the A input jumper in the AN position, negative current input pulses are received by the 47 ohm terminating resistor R81 which develops a voltage drop fed to the base of Q8. When the voltage drop exceeds the threshold voltage set on Q9 base by R38 and R39, Q8 turns off and Q9 turns on. This brings Q9 collector and A56 input from  $\approx 2.5$  V to ground. Components D35, D34, R86 and D24 protect Q8 and Q9 from positive or negative overvoltages.

Operation of Channel B is identical to that of channel A.

Multiplexing counts or time ticks to the counter is carried out by A56 (74F00). Two gates are used by each counting channel. The first decade, which is required to count at 100 MHz, is a 74S196. The second, counting at 10 MHz maximum, is half of a 74LS390. The remaining six decades reside in a LS7031. The 7031 contains six counting decades, latches, and multiplexing logic to read out the six decades plus the data of the two decades ahead. Additionally, it contains logic to recognize leading zeroes and overflow conditions. Thus, in a simple 40-pin IC, a single 14-pin IC, plus half of 16-pin IC, we have an eight decade counter with readout multiplexing.

A counting sequence is initiated with a reset pulse setting all eight decades to zero. Either external events or time ticks are gated to the clock input of the 74S196. The eight bit of the 74S196 clocks the 74LS390, and in turn the eight bit of the 74LS390 clocks the 7031 input decade.

To read the contents for display or read out the counter, data is transferred to latches within the 7031 by means of the Load Latch pulse. The next part of the sequence is to generate a Scan Reset which places the most significant digit (in BCD format) on the four data output lines. As each succeeding digit is required, a Scan Clock pulse is applied to the 7031 which places the next less significant digit on the data output lines. Because the display consists of six digits and the counter capacity is eight, at the time the  $10^8$  counter decade 8 bit resets, A29 is toggled to the one state.

The signal out of the 7031 "D6" is this bit ( $8 \times 10^5$ ), and the output of A29 is called "X100". X100 true causes the X100 display annunciator to turn on and causes a two-digit shift in the data displayed.

The BCD data out of the 7031 is immediately passed through A53, a quad Exclusive-NOR gate. Its function is to either invert or not invert the data. The internal leading zero logic determines this and Blank Out is the signal. The utilization of this function is by the LCD display drivers. When they see a binary 15 they respond by displaying a blank. A BCD zero out of the 7031, if it is an insignificant (leading) zero, is then covered to binary 15 by inversion and is blanked on the display.

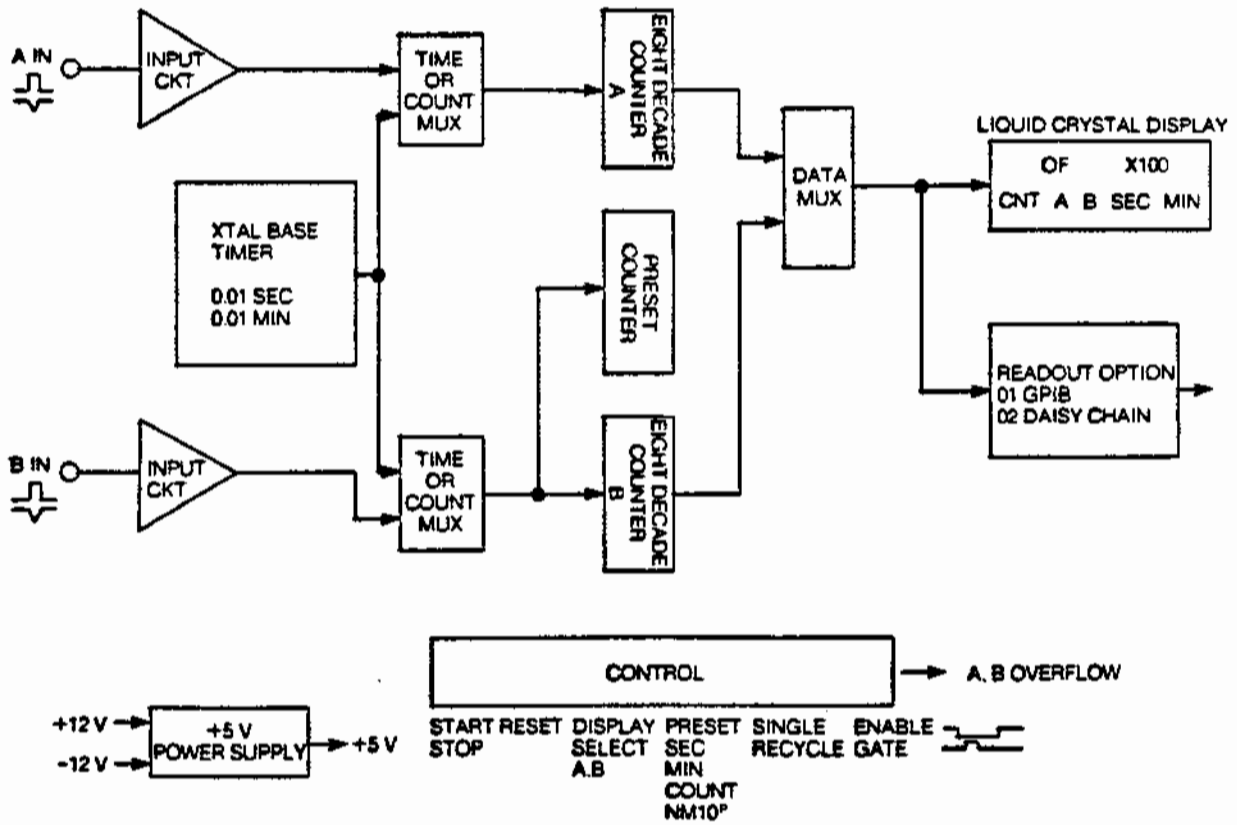


Figure 7.1  
Model 2071A Block Diagram

## 7.2 CRYSTAL BASED TIME GENERATOR

The required 0.01 second and 0.01 minute time ticks originate from a 12 MHz crystal oscillator circuit (OSC1). This frequency is divided by 12 in A33. The resulting one MHz may be gated (jumper selected) by the GATE signal as it passes through A13. This provides the unit a capability for measuring Live Time with a one microsecond resolution. The one MHz is then applied to a prescaler (A35) which provides a divide by  $10^4$  and gives a 0.01 sec output. Dividing the 0.01 sec by 60 (A34) provides the 0.01 min output. The selected time signal may be seen at TP8.

## 7.3 PRESET COUNTER

The eight-decade preset counter with three-digit control consists of a six-decade programmable prescaler plus a two decade down-counter. The three digit thumbwheel switch, labeled NM10<sup>P</sup> provides the eight decades of control. The P switch, with range zero through six, gives direct control over the prescaler (A51). A setting of zero means the input pulses are passed directly through. A setting of six results in the input prescaled (divided) by  $10^6$ . The N and M switches provide the start number for the two decade down-counter (A42, A43). In operation, the N and M decades are loaded with their preset numbers while the unit is not enabled to count. Once enabled, the N and M switches have no control; presets N and M will not be changed at any time, doing so during Enable True is not recommended. Setting both N and M to zero satisfies an eight-input NOR gate (A31) which disables the borrow from the two down counters, which normally occurs when preset is reached. Therefore, N = M = 0 turns the preset function off. It should be noted also that the contents of A51, A42, and A43 are not available for readout.

## 7.4 SIX DECADE LIQUID CRYSTAL DISPLAY

The six-decade liquid crystal display (LCD) has each digit driven by a seven-segment LCD driver IC. With this scheme all digits are driven in parallel (that is, all ON segments are turned on at the same time). The requirement to turn a segment on is that an rms voltage be applied between the backplane and particular segment that is greater than the ON threshold for the LCD. This is accomplished by applying a square wave to the backplane and another to each segment. In-phase square waves result in zero rms (OFF) and 180° out-of-phase results in an rms of 5 V (ON). The type 4056 driver consists of a four-bit latch, a seven-segment decoder and an exclusive-OR array to select the proper phase of the signal applied to each segment.

The same clock (A32) used to strobe the data from the 7031s also provides the approximately 25 Hz square-wave display clock. In addition to the six digits, any of eight annunciators can be shown to describe the data being displayed. "CNT" is displayed when counts from an external source are selected for display. When time is selected, the annunciator "SEC" (seconds) or "MIN" (minutes) will be on. Seconds or Minutes are displayed with a maximum resolution of 0.01 units, therefore a decimal point annunciator is employed, further describing the information displayed. Because the data source may be from the A channel or B channel, A and B annunciators are provided. When the magnitude of the number exceeds six digits ( $10^6-1$ ) a X100

annunciator is enabled and the displayed data is shifted so that the display is  $10^7$  to  $10^8$ , the six most significant digits. It should be noted that losing two digits means a display error ranging from 0.01% to zero. GPIB readout data includes the full eight digits. The remaining annunciator "OF" (overflow) turns on when the counter reaches  $10^8$  counts and remains on until data is reset.

The annunciators are driven by three 4054 four-signal segment drivers. These include latches and exclusive-OR arrays to develop the display-signal phasing required. Combinatorial logic consisting of gates A5, A15, A16, A17, A25, A26, A27, A28 determine which annunciators are on. Additionally A1, a slow oscillator, causes CNT, MIN, or SEC to blink during active counting.

The circuit to obtain data from each of the 7031s is essentially the same for readout or display. The selection of data from either the A channel or B channel is accomplished by multiplexer A37, whose data selection is controlled by the front panel Display Select switch and A23. A 23 is needed so that the data can be changed remotely in readout, allowing readout of both channels.

An oscillator (A32) running at about 50 Hz (divided by the other half of A23, to 25 Hz for the display clock) supplies the 7031 scan clock and an 8-stage Johnson counter (A8). The eight outputs of the Johnson counter are synchronous with the 7031 Digit Strobes and hence, the 7031 output data. The Johnson counter outputs strobe the data into the display LCD drivers. Also the first (TP11) or third (TP12) strobe generates a scan reset. This maintains synchronization and generates the X100 display data shift. Scan reset with the first strobe allows a display of  $10^4$ — $10^6$ . Scan reset with the third strobe allows a display of X100 or  $10^7$ — $10^9$ . This is accomplished by sending the first and third strobe pulses through A38, a dual multiplexer controlled by X100 signals from the A counter and B counter. In readout, the A32 oscillator is replaced by read clocks from the readout option. This is accomplished by half of A12.

## 7.5 CONTROL

The block diagram area labeled Control provides interactive control with all the blocks on the diagram. The prime control capabilities are to place the unit into the count enabled mode, determine which counter counts external events, and various jumper controlled options.

The signal ENABLE, brought to a front panel or rear panel BNC connector, is the count enable function. A low is the true state indicating counting is enabled. This is a bi-directional signal path which allows an external master unit to enable both channels for an externally determined time. The preset logic has no function in this slave mode of operation. The logic sequences in this mode are that once the ENABLE level has been pulled low by the master, a 10 microsecond reset pulse is generated (TP5) and sent to both A and B channels. This means a 10 microsecond dead time is incurred at the beginning of a measurement period. The timer logic, however, is not affected by this; thus time is measured from the beginning edge of ENABLE with only a two to three microsecond propagation delay error.

A Model 2071A may be either a master or slave with no jumper or control changes. Determination of master or slave status is dependent on whether or not the START switch has been pressed. The START switch causes one-half of A3 to be set. It, in turn, drives the ENABLE line low through A14-11. At this point any other units receiving the ENABLE signal are enabled to count as slaves. After the 10 microsecond reset period has elapsed, both counting channels and the preset channel are allowed to accumulate data.

The presence of a Daisy Chain option results in a slightly different concept of master and slave. This option provides interconnected START, STOP, and RESET signals to all units in the system. The preset control N, M, 10<sup>P</sup> must be set to N = M = 0 for a unit to operate as a slave. The ENABLE signal is not used (not connected between units). In this case the unit whose START switch was pressed (not necessarily the master unit) causes the Daisy Chain START pulse to toggle A3 to the one state via signal ST5 in each module.

Termination of counting occurs when the master reaches preset. This occurs on the simultaneous occurrence of borrow from both preset down-counters (A42 and A43), seen as a negative pulse at TP2. Pressing the STOP switch also terminates counting. The master unit then generates the STOP signal to the remainder of the system, terminating the experiment.

Determination of whether a channel counts time or external events is normally based on the preset selector, 0.01 SEC/COUNT/0.01 MIN, position. A preset of either time position results in that time interval being accumulated in channel B. Channel A will then accumulate external events through the A INput connector. Selecting a preset of counts causes external events through the B INput connector to be accumulated in channel B. The A channel will accumulate 0.01 second time intervals.

The GATE input signals normally control counting in channel A or channel B. Pulling the signal low, from an external source, will prevent any accumulation while held low. If the particular experiment requires one or the other channel only to be time gated, internal jumpers (5, P, and 6) provide control with the GATE signal. Normally in position 5, which results in the GATE A signal controlling the 1 MHz clock used to generate the time signals. This means live time can be accumulated with a resolution approaching one microsecond. To enable GATE B instead of GATE A, change this jumper to position P. To disable the Live Time gating, change this jumper to position 6.

An additional jumper-controlled operating mode is available. The mode allows an experiment to be carried out counting external events in both channel A and B and presetting the experiment with time. To accomplish this, move jumper F to U, move jumper N to T. For proper operation a preset of 0.01 SEC or 0.01 MIN is required. Note that the time information is not available for display or readout. In this special mode the display annunciators will not be correct until additional jumpers are changed. Move jumper 1 to 2, and move jumper 3 to 4 to make the display correct.

The Recycle operating circuit consists of the dual monostable A24. Its function is to restart the module approximately 10 seconds after termination of counting. When Recycle is enabled, A24 fires at the end of the count period (Enable goes false). After 10 seconds, the counters A, B, and Preset are reset to zero, counting restarted, and the experiment is carried out again. When Recycle is off (Single), A24 is held reset and the cycle does not start again. A recycle time of 100  $\mu$ seconds is selectable by moving jumper DD to position CC.

Manual data reset is accomplished by pressing the front panel RESET button. Data will be held reset while the button is pressed. To account for switch bounce, a final 10 microsecond reset is applied on release by A24 (pin 7). The application where manual reset is necessary is when jumper G is removed and jumper H installed. Now channel A is not reset with channel B, but only by the manual RESET button, allowing the A data word to accumulate continuously during succeeding count periods.

#### 7.5 POWER SUPPLY

An inverter concept is applied to supply the five volts used by the module logic. Power supplied by the bin +12 V and -12 V buses is converted to ac by the oscillator made up of T1, Q3, Q4, and C17. Oscillation is in the 60 to 70 kHz range. The output of the secondary (T1 terminals 1, 2, and 3) is full-wave rectified by D17 and D18 providing the +5 V for the logic. T2 supplies feedback to the input of T1 (terminal 5), proportional to the output loading and ripple. As the load increases (and the ripple), current is added to the normal T1 input so that the ripple is reduced, compensating for changes in loading.

Short circuit protection is provided by the circuit consisting of Q1, Q2, and their associated bias resistors and capacitors. Q2 is normally on, Q1 off. Q2 collector current passes through R57 to the bases of Q3 and Q4 where, in conjunction with the output phasing of T1 secondary (terminals 7 and 8), oscillation is maintained. When current through R61 is on the order of 200 mA, or more, sufficient voltage is dropped to turn Q1 on, causing Q2 to turn off, effectively stopping the oscillator. Neither Q3 nor Q4 can be on; causing the 5 V secondary to go to zero. At the same time the IR drop through R61 goes to zero allowing Q1 to turn off, Q2 to turn on and the supply to start up. As long as the current loading is excessive, the circuit will be protected by alternately turning off and on.

#### 7.7 DAISY CHAIN OPTION

The Daisy Chain Option allows a user to choose a type of readout or no readout at all depending on his needs. This option provides the ability to interface with existing Canberra counting modules and scanners with one limitation. Old Canberra counters were all six-decade devices so that the readout capability is also six digits. The new eight-decade counter option includes a switch to select which six digits are to read out. The six least significant digits will be selected if the user knows his experiment will not result in more than 10<sup>6</sup>-1 events counted. The six most significant digits can be selected when the experiment's results include numbers greater than 10<sup>6</sup>. This readout selection results in loss of the 10<sup>0</sup> and 10<sup>1</sup> data digits and the attendant error in the data.

The option provides interconnection for five control signals, four data-bits, and ground on two 15-pin connectors.

The control signals and their functions are:

1. **START:** a bidirectional negative-going pulse swinging from + 5 V to ground with a minimum width of 1  $\mu$ sec. The signal causes the counter it is applied to initiate a counting cycle.
2. **STOP:** a bidirectional negative-going pulse going from + 5 V to ground with a minimum width of 1.5  $\mu$ sec. The signal causes the counter it is applied to terminate a counting cycle, and the scanner it is applied to initiate a readout cycle.
3. **RESET:** a bidirectional negative-going pulse going from + 5 V to ground with a minimum width of 1  $\mu$ sec. The signal causes the counter it is applied to clear the data in its accumulators.
4. **HOLD:** a negative level at ground potential; + 5 V when false. This signal, generated by a scanner, disables the counter display-update function and enables the readout function.
5. **PRINT CLOCK:** a negative-going pulse going from + 5 V to ground with a minimum width of 3  $\mu$ sec. The signal originates at the scanner module and is used to request each BCD data character. The counting module, after receiving its required number of print clocks, passes succeeding ones on to the next module. This signal is the only one not wired in parallel to both 15-pin control connectors.

The four data bits swing between + 5 V and ground, are high true, and have 1, 2, 4, 8 weights. The signals are diode-isolated from the bus so that any module can cause a true level regardless of the others.

Readout begins with the HOLD signal going true as a result of the STOP pulse generated by any module in the system. HOLD (level) generated by the system scanner, received by the Daisy Chain interface, causes the Read Clock Enable (RCE) level to be sent to the counter logic. This results in initialization of the logic placing the most significant data digit ( $10^7$ ) on the data lines to the interface. After about 10  $\mu$ sec to allow for data propagation through the CMOS logic, the Readout flip-flop A7 is set (TP5 goes high). This removes the clear level applied to the Digit Counter (A4) and enables the fast clock (FCLK-A8) to advance the Digit Counter twice. This occurs before any Print Clocks arrive from the Scanner module. If the six least significant digits have been selected ( $10^5$  -  $10^6$  switch position), the first two fast clocks are also sent to the module as Read Clock (RCL) pulses. This advances the counter's output data from  $10^7$  to  $10^5$ . When the six most significant digits are selected ( $10^7$  to  $10^9$  switch position) the first two fast clocks are not sent to the module and the  $10^7$  data digit remains on the data lines to the option. When the scanner is ready for the first digit, a Print Clock pulse is sent. The leading edge loads the data into A3 (Data Latch). At the trailing edge, the next data digit is sent from the module to the option board. As the Scanner requires each additional digit, a Print Clock is sent requesting it, whereupon the leading edge loads the latch (A3) and the trailing edge causes the next digit data to be presented to the latch. The seventh Print Clock causes gate A9c to be satisfied resetting the Digital Counter and the Data Latch.

The Fast Clock is allowed to generate two pulses placing the  $10^3$  data digit of the second data word on the data lines to the option. The two-bit Word Counter A2 keeps track of which word is being sent. After the second word has been sent, all succeeding Print Clocks are sent out to the next module via A1-8.

The bidirectional control signals START, STOP and RESET are received and/or generated as follows:

If the START switch is pressed, the ENABLE signal is sent to the option. An edge detector (A5a and A5b) generates a pulse to Q2 which generates the START pulse and sends it out to the remaining modules in the system. A START pulse sent from an external module is sent through the option to the main logic as ST5 where it toggles A3, setting the unit into the count mode.

The same edge-detector which causes the START pulse is also applied to Q3, which sends a RESET pulse to the other modules. Also pressing the front panel RESET button causes a RESET signal to be sent out to the external modules for as long as the button is pressed.

Pressing the STOP switch terminates the counting mode and causes a positive pulse (ECOL) to be sent to the option. It is applied to Q1, causing the STOP signal to be sent to the modules in the system. A received STOP signal, inverted twice, is sent directly to the main logic as STP where it clears A3, taking the unit out of the count mode.

Four jumpers have been included in the form of three 4.7k ohm resistors to Q1, Q2, Q3, and a 2.7 ohm in the RESET circuit. This gives the user some flexibility in choosing whether a given module should generate START, STOP, and RESET in a particular application.

#### 7.8 GPIB INTERFACE OPTION (Talker)

This option provides the ability to read out the module data to the IEEE-488 interface bus. The system uses a byte-serial, bit-parallel format, with bidirectional lines for both data flow and addressing. The system employs a 16-line bus allowing interconnection of up to 15 instruments. Each instrument on the bus is connected in parallel to the 16 lines of the bus. Eight lines transmit data and eight transmit handshake timing and control. Maximum accumulative length of cable in a system cannot exceed two meters (6.5 feet) per device or 20 meters (65 feet) per system, whichever is shorter. Data is transmitted as a series of seven-bit bytes in ASCII code. The eighth data line (parity bit) is not used since this option does not have parity generation capability.

The logic levels on the bus are negative TTL; that is, True = 0 V to +0.4 V dc, False = +2.5 V to +5V dc.

Bus signal nomenclature:

DIO8	data bit	Parity	ATN	Attention
DIO7	data bit	64	SRQ	Service Request
DIO6	data bit	32	IFC	Interface Clear
DIO5	data bit	16	NDAC	Not Data Accepted
DIO4	data bit	8	NRFD	Not Ready for Data
DIO3	data bit	4	DAV	Data Valid
DIO2	data bit	2	EOI	End Or Identify
DIO1	data bit	1	REN	Remote Enable

### 7.10 TYPICAL BUS INTERCHANGE

It is not the intent of this section to be a primer on how the GPIB controller must be programmed. Each of these have unique characteristics and must be studied in detail. There are also several tutorial publications available from Hewlett Packard, Teletronix and Fluke as well as the IEEE. The following descriptions illustrate how the 2071A will respond in the modes that it will be most commonly used.

#### Serial Poll

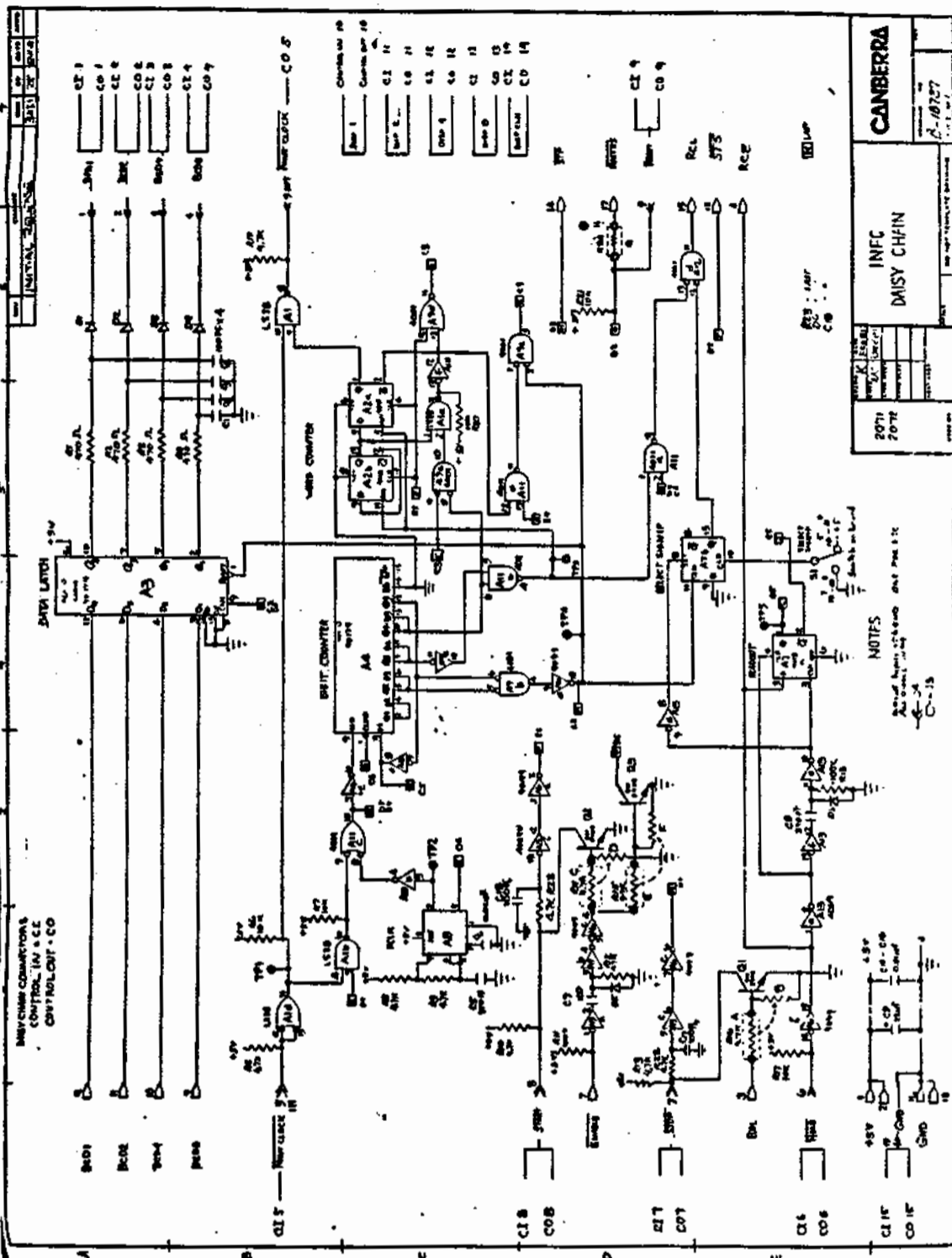
This allows the controller to determine which device requires service. The 2071A will output a Service Request

(SRQ) when it stops counting. The controller may then perform a Serial Poll (SPE) to determine who is requesting service. During the polling sequence, the controller will assign each of the devices to be polled Talk address, and then the device will put out a Status-byte. If the 2071A is requesting service it will output a 42<sub>h</sub>, and remove its Service Request. If it was not the requesting device, then it outputs a status equal to 0. The controller completes the serial poll mode by doing a Serial Poll Disable (SPD). If the 2071A is the only possible source of the Service Request, the controller can choose to respond by Reading the data from the module; this will also clear its Service Request.

<u>Source</u>	<u>7-bit Hex Code</u>	<u>ATN Status</u>	<u>Description</u>
<b>Device Clear</b>			
Controller	14	ATN Asserted	Will cause 2071A to terminate counting if jumper B installed in GPIB interface.
<b>Read Data</b>			
Controller	3F	ATN Asserted	Unlisten all devices
Controller	35	ATN Asserted	Assign Listener at decimal address 27 <sup>3</sup>
Controller	44	ATN Asserted	Assign Talker at decimal address 4 <sup>4</sup>
2071A	30	ATN False	10 <sup>7</sup> digit from counter A equals 0
2071A	30	ATN False	10 <sup>6</sup> digit from counter A equals 0
2071A	38	ATN False	10 <sup>5</sup> digit from counter A equals 8
2071A	31	ATN False	10 <sup>4</sup> digit from counter A equals 1
2071A	36	ATN False	10 <sup>3</sup> digit from counter A equals 6
2071A	32	ATN False	10 <sup>2</sup> digit from counter A equals 2
2071A	39	ATN False	10 <sup>1</sup> digit from counter A equals 9
2071A	37	ATN False	10 <sup>0</sup> digit from counter A equals 7
2071A	0D <sup>1</sup>	ATN False	Carriage return
2071A	39	ATN False	10 <sup>7</sup> digit from counter B equals 9
2071A	38	ATN False	10 <sup>6</sup> digit from counter B equals 8
2071A	37	ATN False	10 <sup>5</sup> digit from counter B equals 7
2071A	36	ATN False	10 <sup>4</sup> digit from counter B equals 6
2071A	35	ATN False	10 <sup>3</sup> digit from counter B equals 5
2071A	34	ATN False	10 <sup>2</sup> digit from counter B equals 4
2071A	33	ATN False	10 <sup>1</sup> digit from counter B equals 3
2071A	32	ATN False	10 <sup>0</sup> digit from counter B equals 2
2071A	0D <sup>1</sup>	ATN False	Carriage return
2071A	0A <sup>2</sup>	ATN False	EOI Asserted, Line Feed

#### Note:

1. The carriage return indicating end-of-word may be switch selected to output a form feed (code 0C).
2. The line feed and EOI indicate to the controller that the 2071A presently talking is now finished sending data.
3. 27<sub>10</sub> is the address of the device which is to receive the 2071A's data.
4. 4<sub>10</sub> is the 2071A's address in this example with its channel A and B counters equal to 816297 and 98765432, respectively.



MECHANICAL COMPUTER'S CONTROL (IN & CE CONTROL UNIT - CO)

DATA LATCH

BRIT. COUNTER

UNIT COUNTER

RELAY

NOTES

As per drawing and Part 112

A-15

CANBERRA

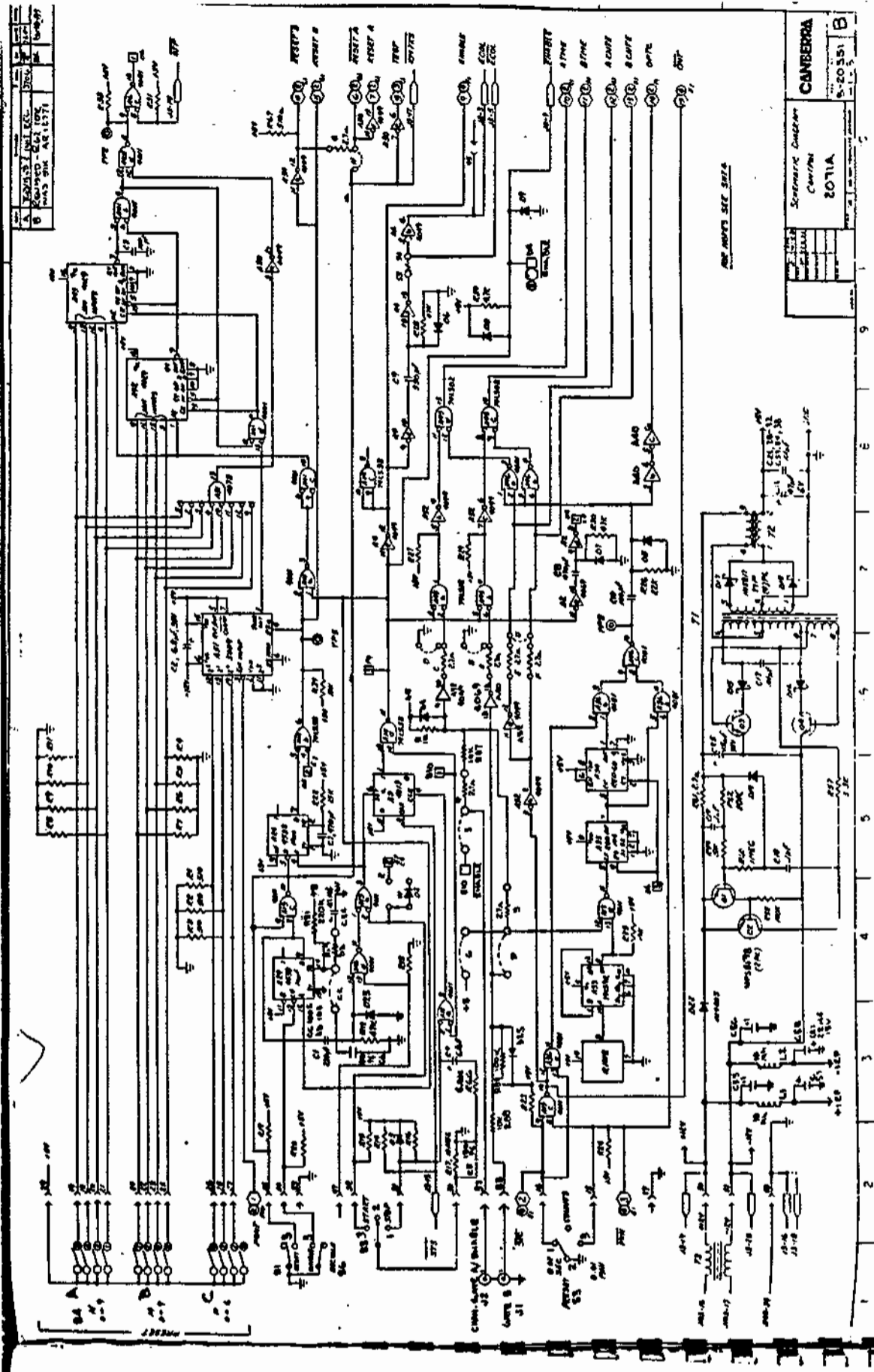
DISY CHIN

1957

1958







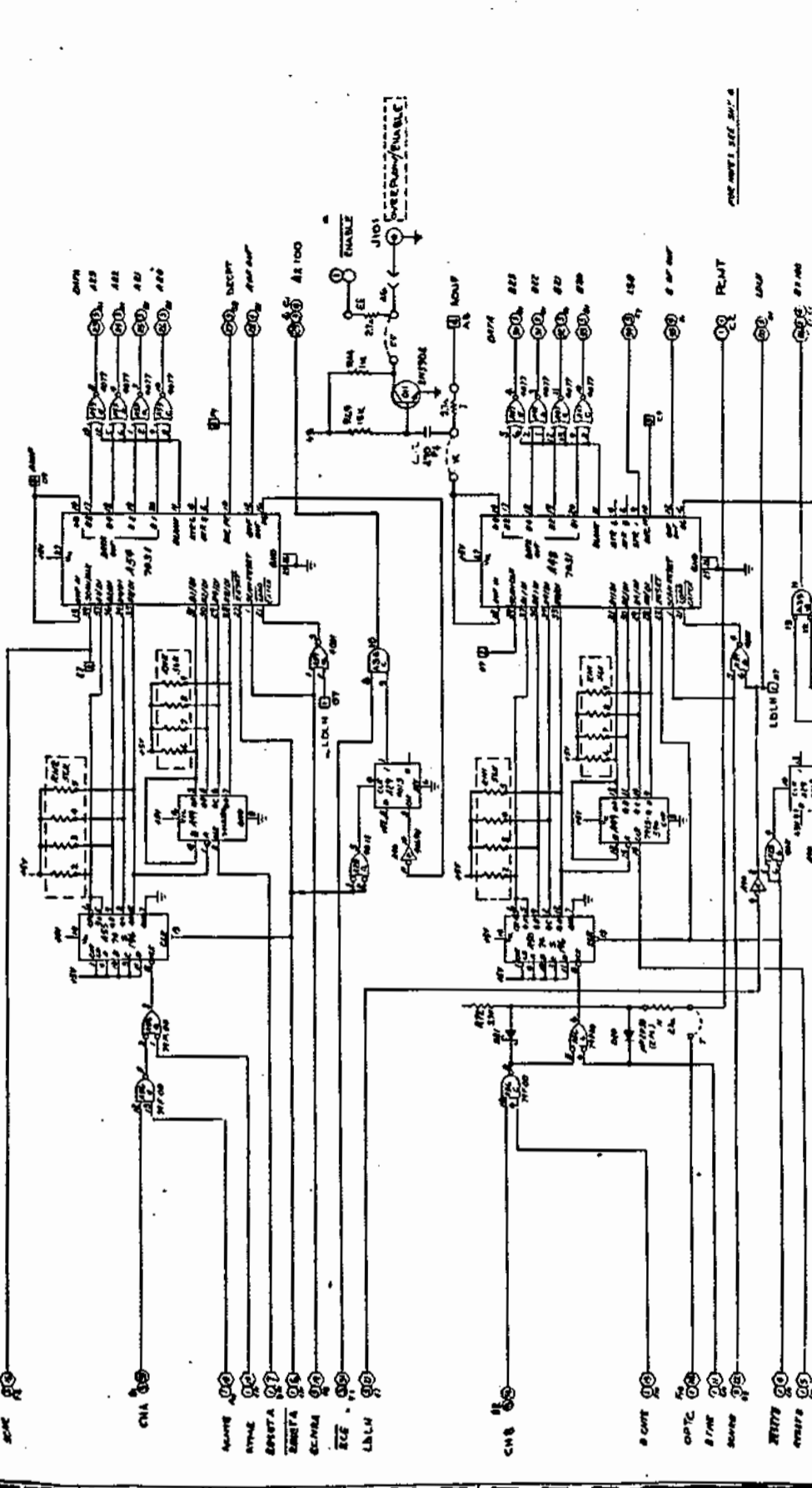
**CANBERRA**  
 SCHEMATIC DIAGRAM  
 CONTROL  
 2071A

5-20551  
 B

SEE DRAWING SEC 5074

1 2 3 4 5 6 7 8 9

REV	NO	DATE	BY
A	1	10/1/51	J. L. B.
B	1	10/1/51	J. L. B.



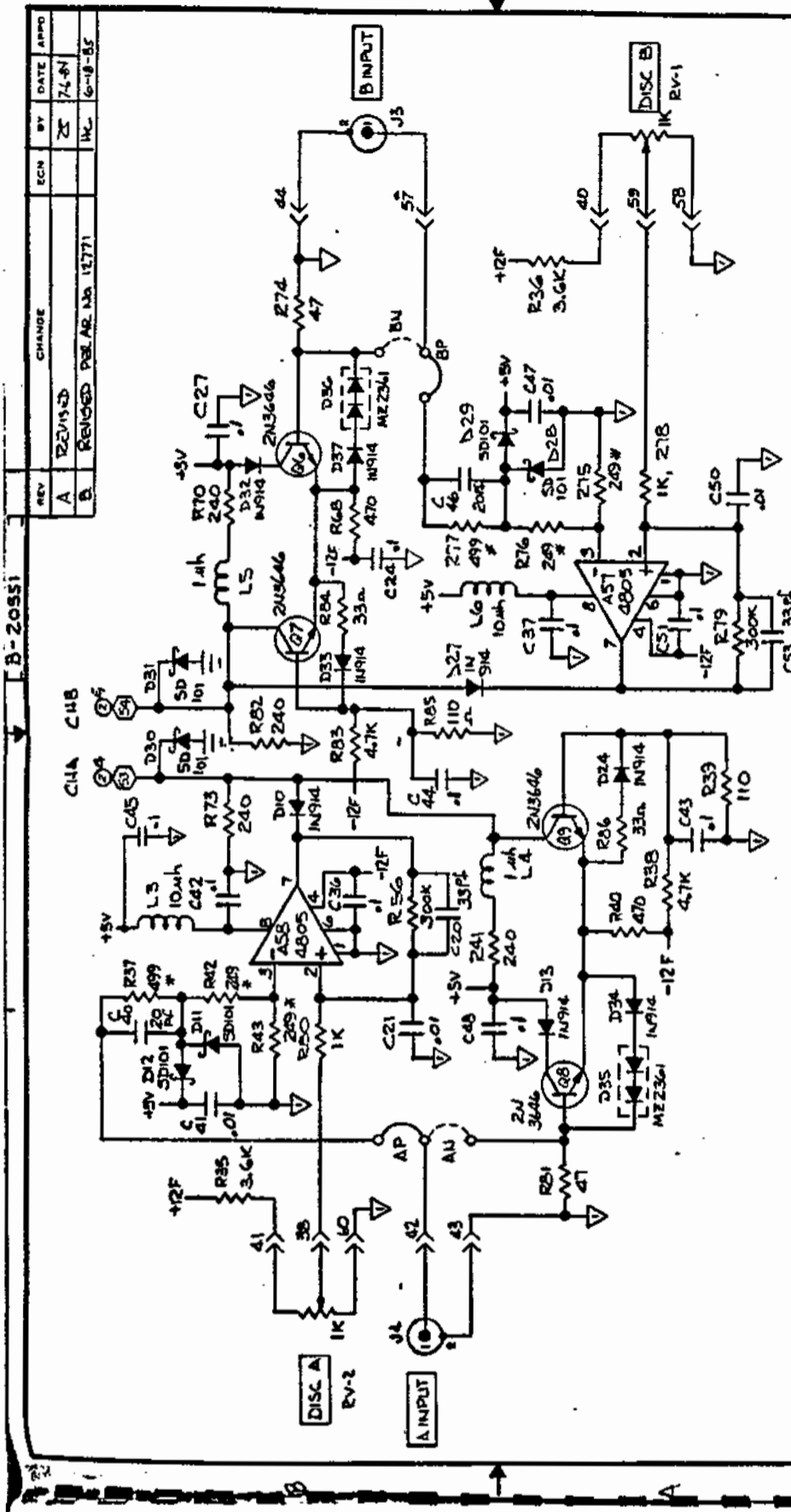
REV	NO	DATE	BY
A	1	10/1/51	J. L. B.
B	1	10/1/51	J. L. B.

CAMBERA  
 SCHEMA DE CONTROL  
 CHANNELS A/B  
 B-20551

FOR WPT-1 SEE SH-4







REV	CHANGE	ECN	BY	DATE	APPRO
A	REVISED		ZC	7-4-81	
B	REVISED PER AR NO. 12771		WC	6-18-85	

**CANBERRA**  
MERIDEN, CONNECTICUT

DRAWING NO. B-20551  
REV. 1

SCALE: 1/8" = 1"

DO NOT TEMPLATE DRAWING

INTERMEDIATE	REVISIONS	DATE	BY	REASON
	1	3-22-84		
	2			
	3			
	4			
	5			

UNLESS OTHERWISE SPECIFIED  
RESISTORS: 5% TOLERANCE  
CAPACITORS: 5% TOLERANCE  
WIREWOUND RESISTORS: 1% TOLERANCE  
RESISTORS: 1% TOLERANCE  
CAPACITORS: 5% TOLERANCE

2071  
USED ON