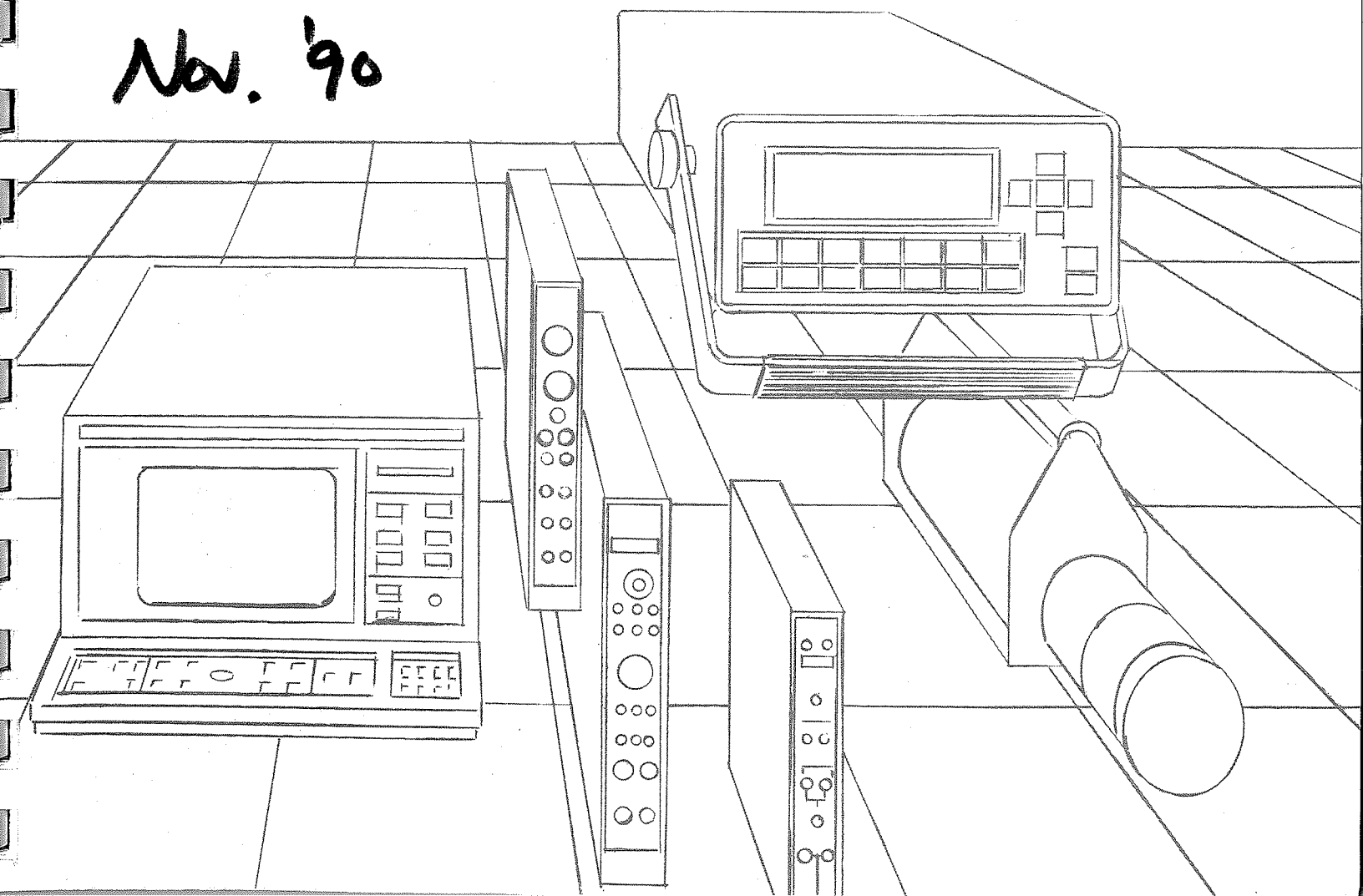
CANBERRA

LOGIC SHAPER AND DELAY
Model 2055

Instruction Manual

Physics 191/297 laboratory

Nov. '90



LOGIC SHAPER & DELAY
Model 2055

CONTENTS

CONTENTS
(continued)

Page

LOGIC SHAPER & DELAY
MODEL 2055

Section 1
INTRODUCTION

The Model 2055 Logic Shaper and Delay offers versatility and performance. Its five simultaneous outputs offer solutions to many timing and logic interface problems. In addition input/output incompatability between instruments of different manufacture can be eliminated by the 2055.

Standard logic input pulses of either polarity generate the five simultaneous outputs for the experimenter's use. Separate positive and negative output logic signals are available with continuously adjustable delay, width and amplitude. Accompanying outputs include a Fast Negative NIM logic output following the selected delay time and a Period Output with its width equal to the delay time. Thus, logic signals meeting the input requirements of the Model 2055 may be reshaped and delayed up to 110 microseconds to provide maximum logic interface capability.

In timing applications, the multi-function 2055 compensates for inter-channel timing differences in fast/slow coincidence experiments. Since the PERIOD OUT is positive and negative, both coincidence and anticoincidence measurements can be performed.

The range of delay (0.1 to 110μs) allows the 2055 to be used in a wide variety of timing experiments from fast NIM logic applications to slow gas proportional detector anticoincidence measurements.

Typical interfacing applications are illustrated below:

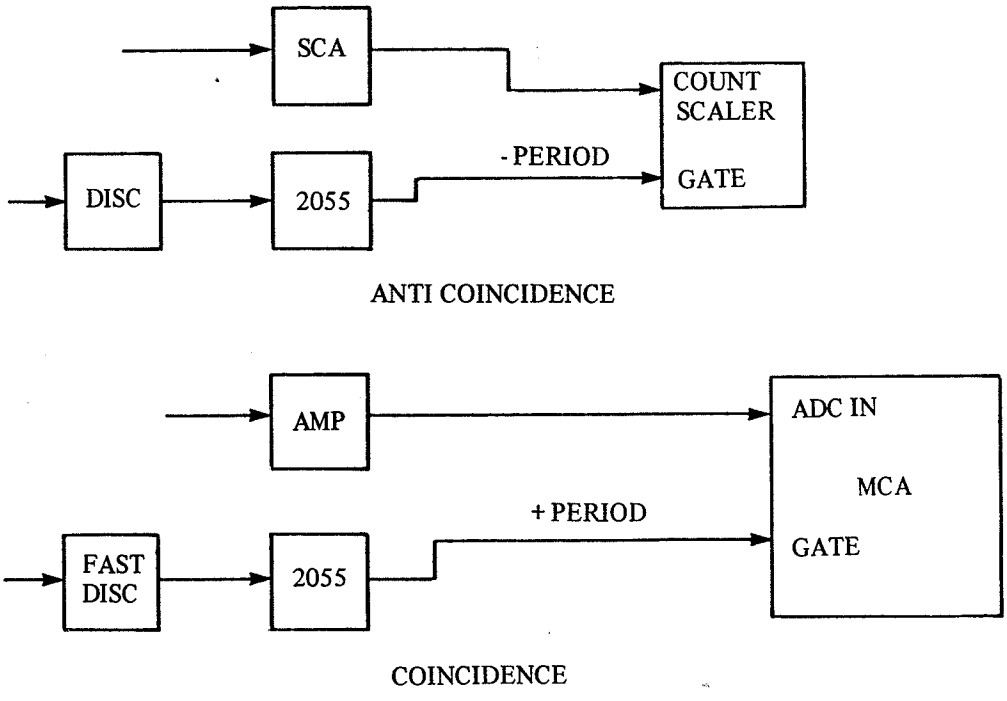


Figure 1-1. Typical Applications

Section 2
SPECIFICATIONS

2.1 INPUTS

INPUT

Accepts positive 0.7 to 12V or negative 0.4 to 12V NIM logic pulses
Rise time: any
Width: 20 nanoseconds minimum at +1V:
20 nanoseconds minimum at −1V
Z_{in}: ≈ 1K ohm, DC coupled, front/rear panel BNC connectors

2.2 OUTPUTS

POSITIVE

Logic pulse; variable amplitude range +2 to +10V
Width: Variable, 0.5 to 5μsec
Delay: Variable, 0.1 to 110μsec (plus propagation delay of approximately 75 nanoseconds)
Rise and fall time: ⩽ 25 nanoseconds
Z_{out}: ⩽ 25 ohms; short circuit protected, DC coupled, front panel BNC connector

NEGATIVE

Logic pulse characteristics identical to Positive output except for negative polarity

FAST

Standard fast negative NIM logic pulse: −800mV into 50 ohm load
Rise time: ⩽ 5 nanoseconds
Width: ≈ 20 nanoseconds
Z_{out}: 50 ohms; short circuit protected, DC coupled, front panel BNC connector

+ PERIOD

Logic pulse; amplitude ⩾ +4, ⩽ 5 Volts
Width: equal to selected Delay
Rise and fall time: ⩽ 25 nanoseconds
Z_{out}: ⩽ 25 ohms; short circuit protected, DC coupled, front panel BNC connector

− PERIOD

Logic pulse characteristics identical to + PERIOD output except inverted pulse excursion is to 0 to + 0.5 Volts from + 4 to 5 Volts.

Signal provided on front and rear panel BNC connectors.

2.3 CONTROLS

DELAY μsec

Front panel ten-turn precision locking potentiometer, continuously variable from 100 nanoseconds to 110μseconds (plus propagation delay ≈ 75 nanoseconds) in three overlapping ranges

MULTIPLIER	Front panel toggle switch to select DELAY potentiometer range of 0.1 to 1.1μsec, 1.0 to 11μsec, or 10 to 110μsec; X0.1, X1, and X10 positions
WIDTH	Front panel single-turn potentiometer to simultaneously adjust the Positive and Negative logic output widths; 0.5 to 5μsec range
AMPLITUDE	Front panel single-turn potentiometer to simultaneously adjust the Positive and Negative logic output amplitudes; 2 to 10V range
INPUT POS/NEG	Front panel toggle switch selects either Positive or Negative position to match logic input pulse polarity

2.4 PERFORMANCE

DELAY NONLINEARITY	Less than ± 0.5% of selected DELAY range
DELAY DRIFT	Less than ± 0.1%/°C of DELAY range selected
DELAY JITTER	Less than 0.02% of selected DELAY range
PULSE PAIR RESOLUTION	
DELAY MULTIPLIER X 10	DELAY Plus 10μs
DELAY MULTIPLIER X 1	DELAY Plus 1μs } When POS or NEG outputs used add WIDTH plus 1.5μs
DELAY MULTIPLIER X 0.1	DELAY Plus 0.5μs } When POS or NEG outputs used add WIDTH plus 1.5μs

2.5 CONNECTORS

INPUT, POS, NEG, FAST, +PERIOD, −PERIOD	Front panel, BNC, UG-1094/U
INPUT, NEG PERIOD	Rear panel, BNC, UG-1094/U

2.6 POWER

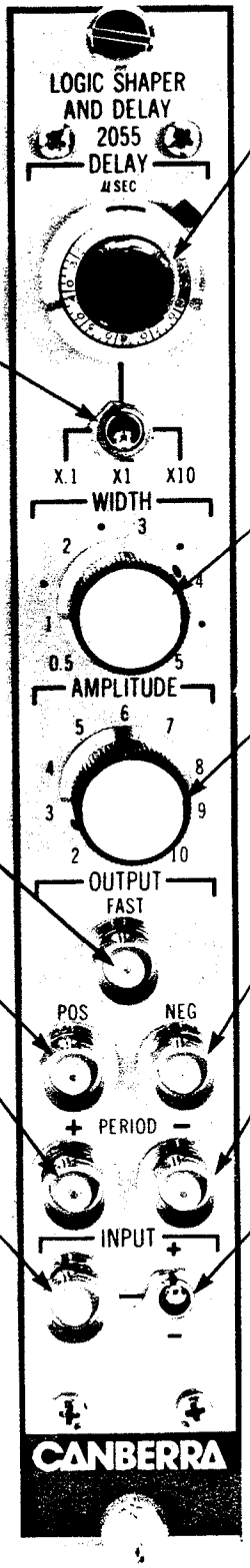
+24V	0mA
−24V	0mA
+12V	100mA
−12V	70mA

2.7 PHYSICAL

SIZE	Standard single-width NIM module (1.35 x 8.714 inches) per TID-20893 (Rev.)
WEIGHT	1.6 lbs. (0.7 kgs.)

Section 3
CONTROLS AND CONNECTORS

FRONT PANEL



R3
DELAY CONTROL
1.0 to 11μsec.

S1
DELAY MULTIPLIER
X0.1, X1, or X10 provides a total range of 0.1 to 110μsec

R4
OUTPUT PULSE WIDTH CONTROL
0.5 to 5μsec.

R5
OUTPUT PULSE AMPLITUDE
2 to 10 volts.

J1
FAST OUTPUT SIGNAL
−800mV into 50 ohms;
tr ≤5 nanosec;
tw ≈20 nanosec.

J2
NEGATIVE OUTPUT SIGNAL

J3
POSITIVE OUTPUT SIGNAL

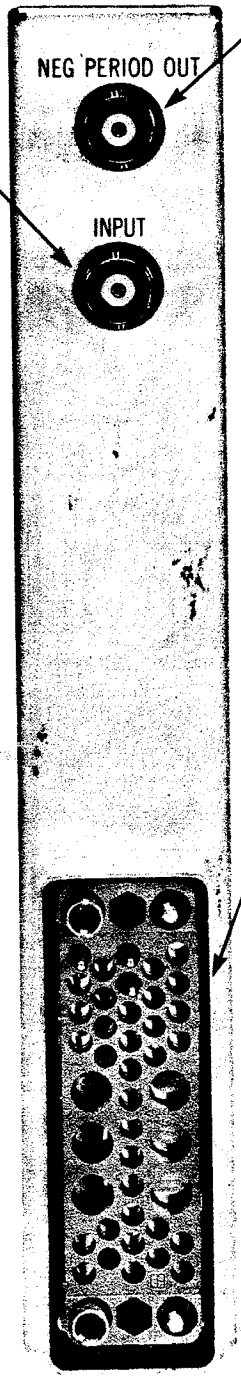
J4
−PERIOD
Logic Pulse - Zero: +4 to +5V.
One: 0 to +0.5V.
Width equal to delay

J5
+ PERIOD
Logic Pulse - Zero: 0 to +0.5V.
One: +4 to +5V
Width equal to delay.

S2
INPUT SIGNAL POLARITY SELECTOR

J6
INPUT SIGNAL
+0.7 to +12V, Width >20nsec
−0.4 to −12V, Width >20nsec
Z_{in} ≈1K ohms, DC coupled.

REAR PANEL



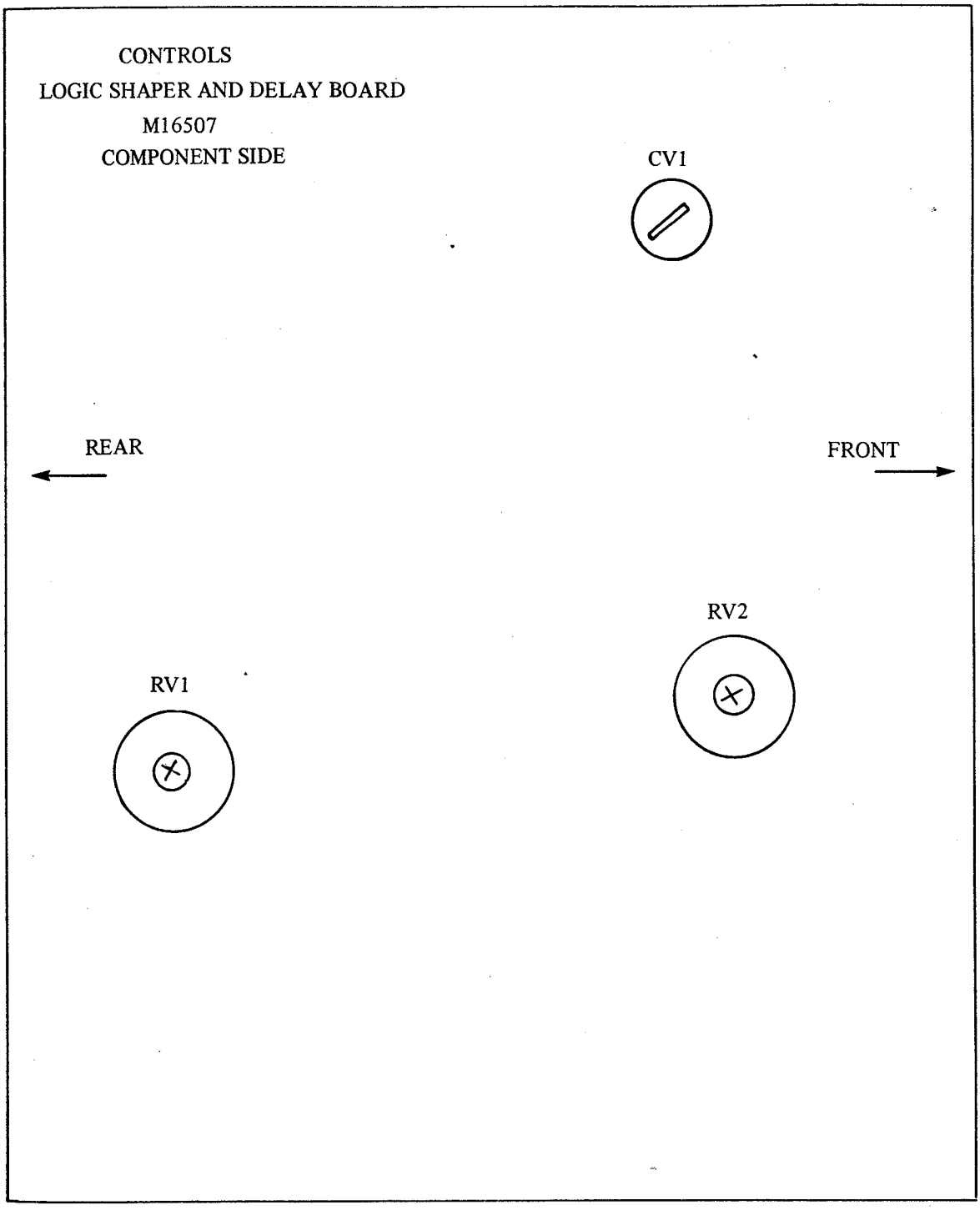
J101
NEG PERIOD OUT
Parallel Connection to J4, –Period.

J102
INPUT
Parallel Connection to J6, Input

J103
POWER
Connections used:

PIN	VOLTAGE
16	+12 Volts
17	–12 Volts
34	Ground

INTERNAL CALIBRATION CONTROLS



Section 4
OPERATING INSTRUCTIONS

4.1 GENERAL

1. The purpose of this section is to familiarize the user with the controls of the Model 2055 Logic Shaper and Delay and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

2. 50 ohm as well as 93 ohm coaxial cables and terminations may be utilized with the Model 2055.

4.2 INITIAL OPERATION

1. Insert the Model 2055 Delay Amplifier in on AEC compatible bin unit/power supply such as Canberra Model 2000. Set the Power switch to ON.

2. Set the 2055 Polarity Selector to Pos. Adjust a pulse generator for a +5.0 volt, 1 microsecond wide signal and connect it to the 2055 Input. Input rate to be < 5kHz.

3. Using an oscilloscope (use 93 ohm coax), monitor the Pos Output connector. Set the WIDTH control mid range and vary the AMPLITUDE control from CCW to CW and observe the pulse amplitude change from less than 2.0V to greater than 10.0V. The unterminated max. of 10.0V becomes 8.0V with 93 ohm termination and 7.5V at 50 ohm termination.

4. Set the AMPLITUDE control to mid scale and vary the WIDTH control. Terminate the cable in 93 ohms. When the WIDTH control is full CCW, the output pulse width should be less than 500 nanoseconds. Move WIDTH to full CW and observe the output signal width is 5 microseconds or greater.

5. Repeat Steps 3 and 4 observing the NEG Output signal.

6. Monitor the +PERIOD Output connector (terminate the cable with 93 ohms). Decrease the DELAY Control to full CCW. Set the Multiplier to X0.1. The output signal should be $\geqslant 4.0$ volts in amplitude and the width should be 100 nanoseconds. Turn DELAY to full CW and observe the output width should be 1.1 microseconds. Turn the DELAY control to 5.0 and observe the pulse width to be 0.5 microseconds. Switch the Multiplier to X1.0 and observe that the output width changes to 5.0 microseconds. Switch the Multiplier to X10 and observe that the output width changes to 50 microseconds.

7. Repeat Step 6 monitoring the - Period Output connector.

8. Monitor the Fast Output connector with the oscilloscope (terminate in 50 ohms). Trigger scope on the leading edge of +Period Output. Observe that Fast Output pulse occurs at end of Delay time setting. The pulse is approximately 20 nanoseconds wide and has a negative amplitude of 800mV.

4.3 INTERCONNECTIONS

Interconnecting between the various units in an experiment requires coaxial cables. These cables should be terminated resistively in their characteristic impedances. Failure to follow this requisite may result in ringing (several cycles of oscillation of varying amplitude at signal transition times) and/or spurious pulses appearing on the output. Both can initiate false triggering and subsequent erroneous experiment results.

INPUT and NEG PERIOD OUT on the rear panel are parallel connections to the front panel INPUT and –PERIOD output connectors, respectively. They are there to aid interconnecting to other units. Also, fewer cables to the front panel contributes to neatness of the installation.

5.6 FAST NEGATIVE CIRCUIT

This circuit provides a standard negative Fast NIM logic signal at the end of the delay period selected. The trailing edge of the delay monostable pulse is differentiated by CV1 (internal adjustment for setting the Fast negative output width) and R31. The negative portion of this pulse is fed to the drivers Q22 and Q23 and presented to the Fast Output BNC.

5.7 WIDTH MONOSTABLE

This monostable provides a means of adjusting the output width of the Positive and Negative Outputs. It consists of A2b, A2c, Q13, Q14 and is fired by the trailing edge of the delay monostable pulse. Q13, a current source, provides a constant current to the timing capacitor C9. By adjusting the Width control R4, the current to the timing capacitor is varied to change the time Q14 is ON and therefore the width of the monostable from 0.4 to 5 microseconds. RV2 is an internal adjustment to calibrate the Width control R4.

5.8 AMPLITUDE ADJUSTMENT CIRCUIT

This circuit controls the amplitude of the pulse, by a front panel Amplitude control, that is fed to the Negative and Positive Outputs. The output of the width monostable is fed through Q17. In the collector of Q17 is a voltage source Q18 which controls the amplitude of the pulse at the collector of Q17. This voltage is determined by R5, the Amplitude control. The pulse at the collector of Q17 is then fed to the Negative and Positive outputs through their buffers.

5.9 POSITIVE OUTPUT BUFFER

The Positive Output buffer provides a low impedance fast rise and fall time pulse with variable width and amplitude to the Positive Output BNC. This buffer is made up of a pair of complementary emitter followers Q15 and Q16.

5.10 NEGATIVE OUTPUT BUFFER

The Negative Output buffer provides a low impedance fast rise and fall time pulse with variable width and amplitude to the Negative Output BNC. This buffer is made up of an inverter Q19 and a pair of complementary emitter followers Q20 and Q21.

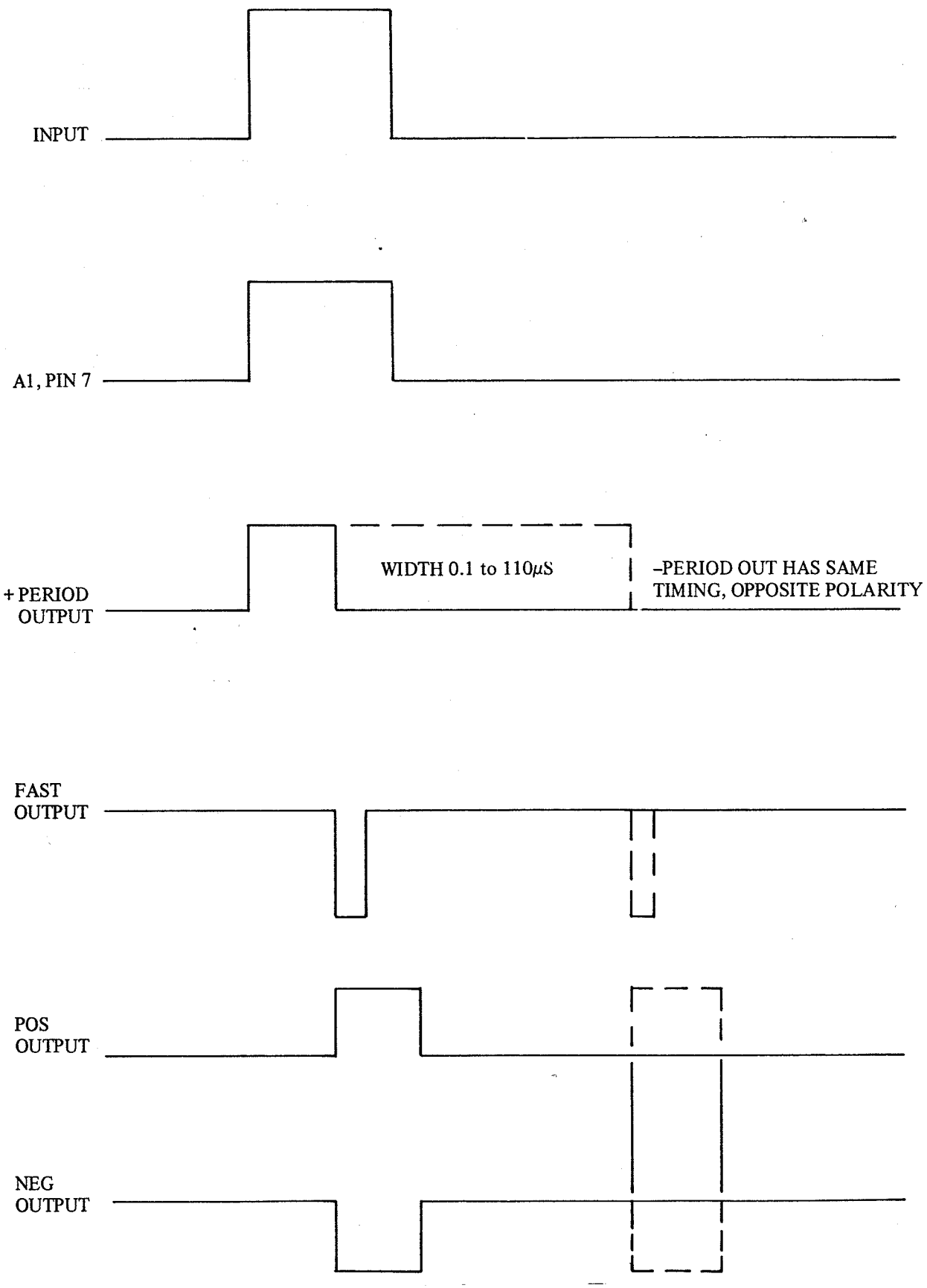


Figure 5-1. Model 2055 Timing Diagram

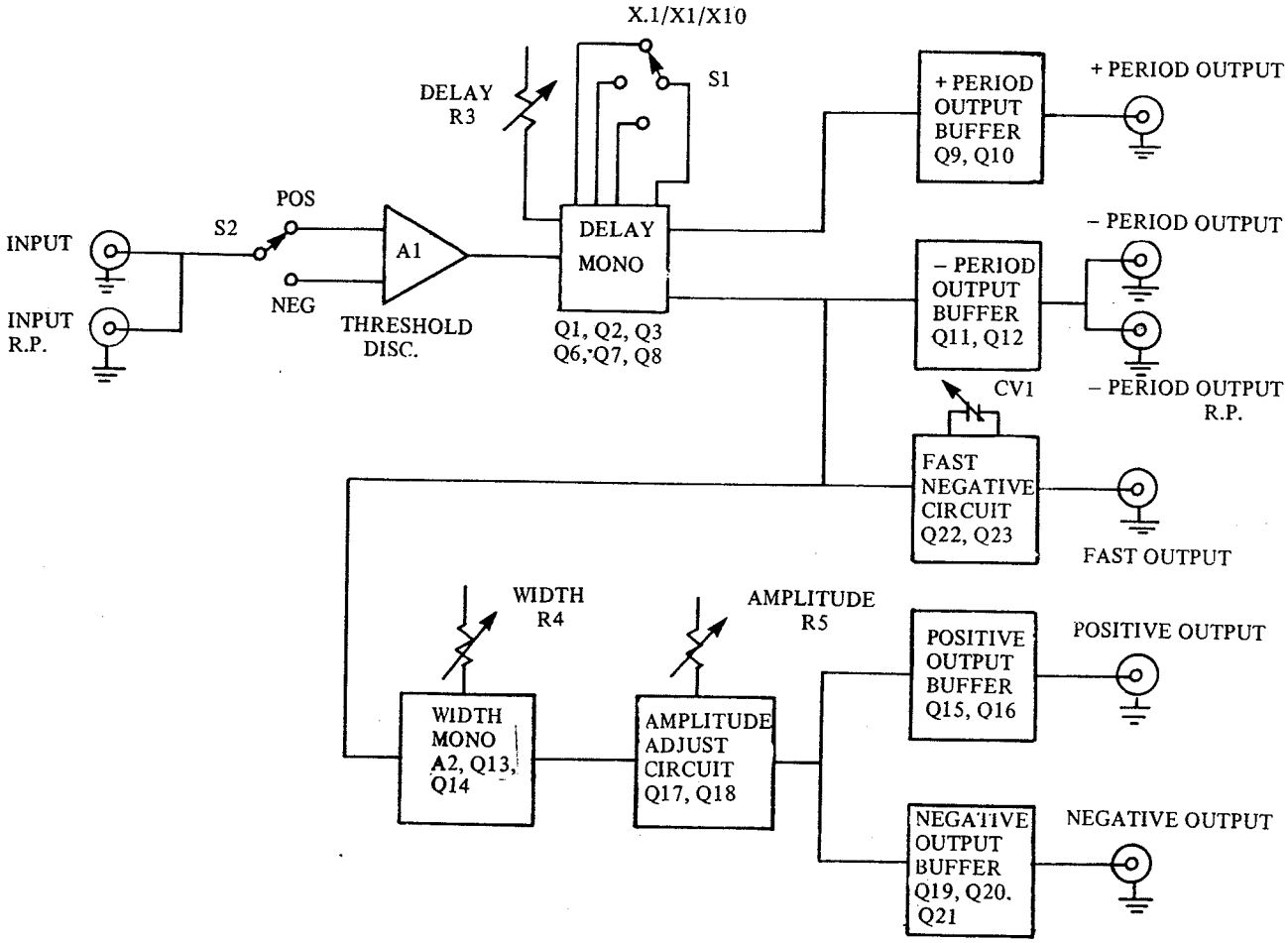


Figure 5-2. Model 2055 Block Diagram

LOGIC SHAPER AND DELAY
Model 2055

Instruction Manual

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

LOGIC SHAPER & DELAY
Model 2055

CONTENTS

CONTENTS
(continued)

LOGIC SHAPER & DELAY
MODEL 2055

Section 1
INTRODUCTION

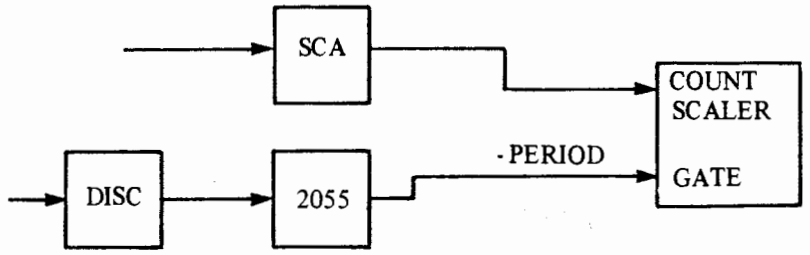
The Model 2055 Logic Shaper and Delay offers versatility and performance. Its five simultaneous outputs offer solutions to many timing and logic interface problems. In addition input/output incompatability between instruments of different manufacture can be eliminated by the 2055.

Standard logic input pulses of either polarity generate the five simultaneous outputs for the experimenter's use. Separate positive and negative output logic signals are available with continuously adjustable delay, width and amplitude. Accompanying outputs include a Fast Negative NIM logic output following the selected delay time and a Period Output with its width equal to the delay time. Thus, logic signals meeting the input requirements of the Model 2055 may be reshaped and delayed up to 110 microseconds to provide maximum logic interface capability.

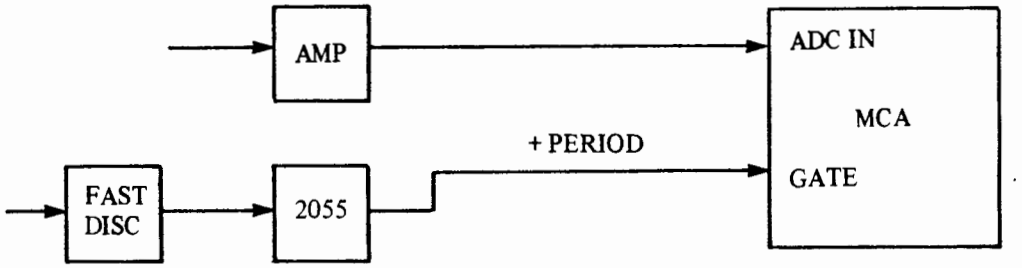
In timing applications, the multi-function 2055 compensates for inter-channel timing differences in fast/slow coincidence experiments. Since the PERIOD OUT is positive and negative, both coincidence and anticoincidence measurements can be performed.

The range of delay (0.1 to 110μs) allows the 2055 to be used in a wide variety of timing experiments from fast NIM logic applications to slow gas proportional detector anticoincidence measurements.

Typical interfacing applications are illustrated below:



ANTI COINCIDENCE



COINCIDENCE

Figure 1-1. Typical Applications

Section 2
SPECIFICATIONS

2.1 INPUTS

INPUT	Accepts positive 0.7 to 12V or negative 0.4 to 12V NIM logic pulses Rise time: any Width: 20 nanoseconds minimum at +1V: 20 nanoseconds minimum at −1V Z_{in}: ≈ 1K ohm, DC coupled, front/rear panel BNC connectors

2.2 OUTPUTS

POSITIVE	Logic pulse; variable amplitude range +2 to +10V Width: Variable, 0.5 to 5μsec Delay: Variable, 0.1 to 110μsec (plus propagation delay of approximately 75 nanoseconds) Rise and fall time: ⩽ 25 nanoseconds Z_{out}: ⩽ 25 ohms; short circuit protected, DC coupled, front panel BNC connector
NEGATIVE	Logic pulse characteristics identical to Positive output except for negative polarity
FAST	Standard fast negative NIM logic pulse: −800mV into 50 ohm load Rise time: ⩽ 5 nanoseconds Width: ≈ 20 nanoseconds Z_{out}: 50 ohms; short circuit protected, DC coupled, front panel BNC connector
+ PERIOD	Logic pulse; amplitude ⩾ +4, ⩽ 5 Volts Width: equal to selected Delay Rise and fall time: ⩽ 25 nanoseconds Z_{out}: ⩽ 25 ohms; short circuit protected, DC coupled, front panel BNC connector
− PERIOD	Logic pulse characteristics identical to + PERIOD output except inverted pulse excursion is to 0 to + 0.5 Volts from + 4 to 5 Volts. Signal provided on front and rear panel BNC connectors.

2.3 CONTROLS

DELAY μsec	Front panel ten-turn precision locking potentiometer, continuously variable from 100 nanoseconds to 110μseconds (plus propagation delay ≈ 75 nanoseconds) in three overlapping ranges

MULTIPLIER	Front panel toggle switch to select DELAY potentiometer range of 0.1 to 1.1μsec, 1.0 to 11μsec, or 10 to 110μsec; X0.1, X1, and X10 positions
WIDTH	Front panel single-turn potentiometer to simultaneously adjust the Positive and Negative logic output widths; 0.5 to 5μsec range
AMPLITUDE	Front panel single-turn potentiometer to simultaneously adjust the Positive and Negative logic output amplitudes; 2 to 10V range
INPUT POS/NEG	Front panel toggle switch selects either Positive or Negative position to match logic input pulse polarity

2.4 PERFORMANCE

DELAY NONLINEARITY	Less than ± 0.5% of selected DELAY range
DELAY DRIFT	Less than ± 0.1%/°C of DELAY range selected
DELAY JITTER	Less than 0.02% of selected DELAY range
PULSE PAIR RESOLUTION	
DELAY MULTIPLIER X 10	DELAY Plus 10μs
DELAY MULTIPLIER X 1	DELAY Plus 1μs (When POS or NEG outputs used add WIDTH plus 1.5μs)
DELAY MULTIPLIER X 0.1	DELAY Plus 0.5μs (When POS or NEG outputs used add WIDTH plus 1.5μs)

2.5 CONNECTORS

INPUT, POS, NEG, FAST, + PERIOD, −PERIOD	Front panel, BNC, UG-1094/U
INPUT, NEG PERIOD	Rear panel, BNC, UG-1094/U

2.6 POWER

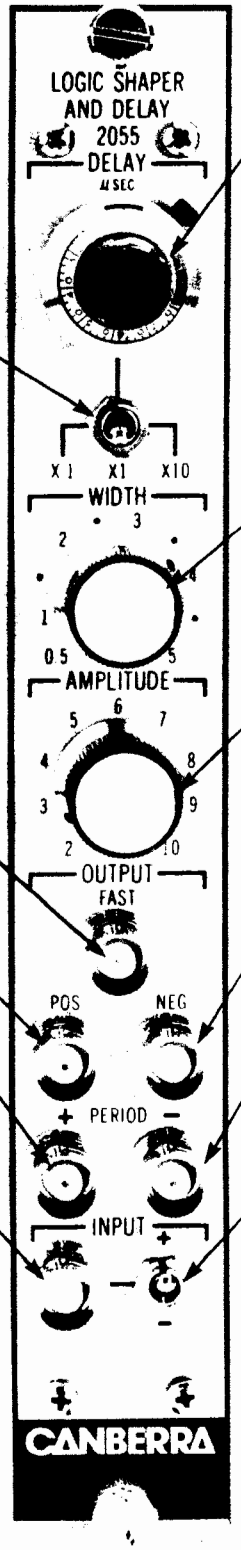
+24V	0mA
−24V	0mA
+12V	100mA
−12V	70mA

2.7 PHYSICAL

SIZE	Standard single-width NIM module (1.35 x 8.714 inches) per TID-20893 (Rev.)
WEIGHT	1.6 lbs. (0.7 kgs.)

Section 3
CONTROLS AND CONNECTORS

FRONT PANEL



R3
DELAY CONTROL
1.0 to 11μsec.

S1
DELAY MULTIPLIER
X0.1, X1, or X10 provides a total range of 0.1 to 110μsec

R4
OUTPUT PULSE WIDTH CONTROL
0.5 to 5μsec.

R5
OUTPUT PULSE AMPLITUDE
2 to 10 volts.

J1
FAST OUTPUT SIGNAL
−800mV into 50 ohms;
$t_r \leq 5$ nanosec;
$t_w \approx 20$ nanosec.

J2
NEGATIVE OUTPUT SIGNAL

J3
POSITIVE OUTPUT SIGNAL

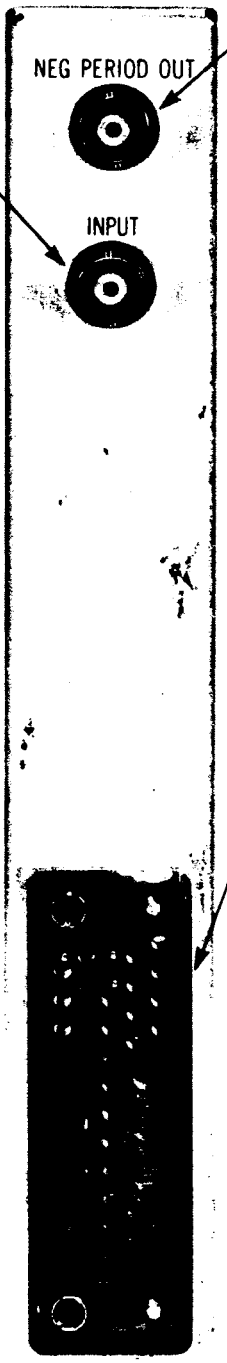
J4
−PERIOD
Logic Pulse - Zero: +4 to +5V.
One: 0 to +0.5V.
Width equal to delay

J5
+ PERIOD
Logic Pulse - Zero: 0 to +0.5V.
One: +4 to +5V
Width equal to delay.

S2
INPUT SIGNAL POLARITY SELECTOR

J6
INPUT SIGNAL
+0.7 to +12V, Width >20nsec
−0.4 to −12V, Width >20nsec
$Z_{in} \approx 1$K ohms, DC coupled.

REAR PANEL



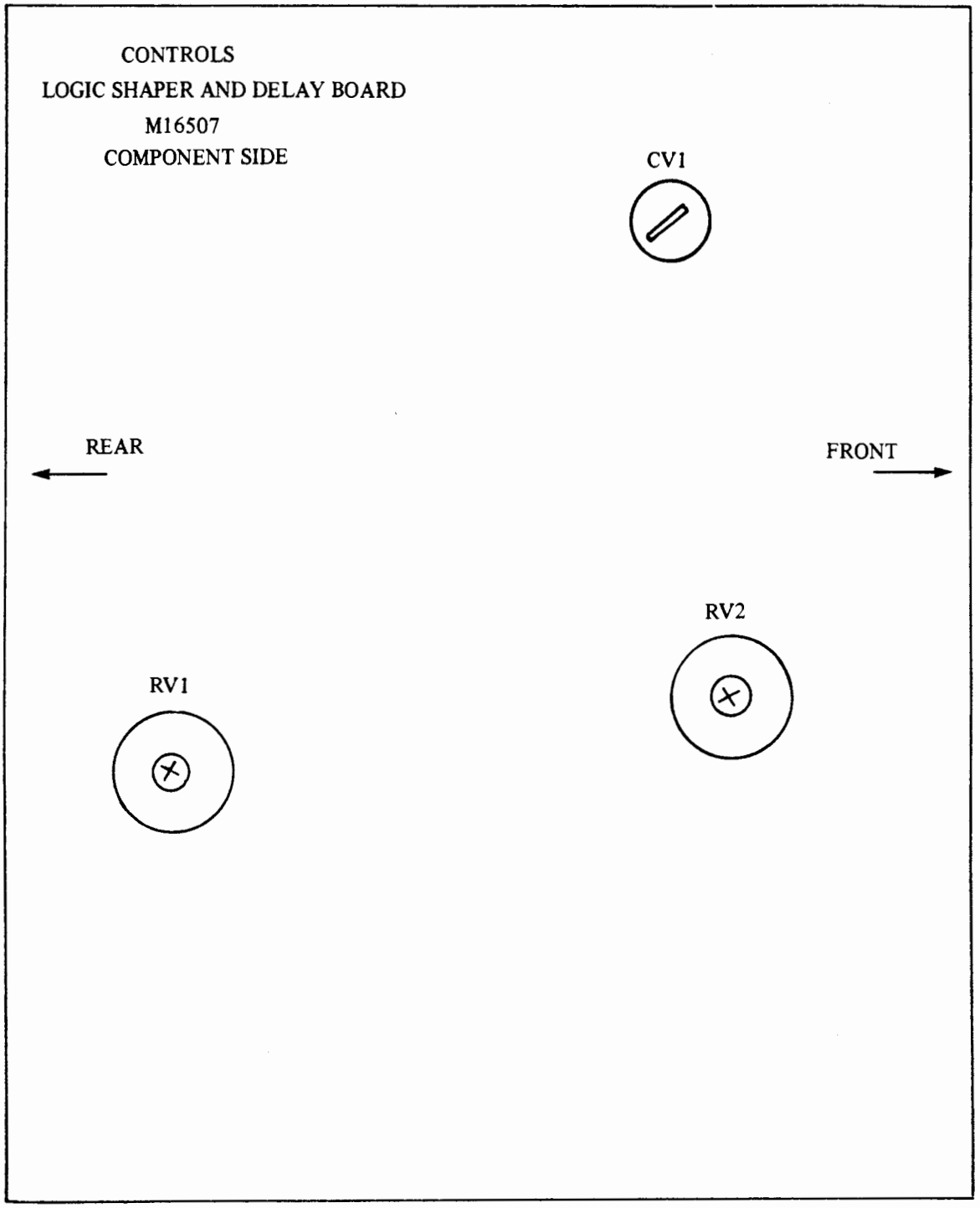
J101
NEG PERIOD OUT
Parallel Connection to J4, -Period.

J102
INPUT
Parallel Connection to J6, Input

J103
POWER
Connections used:

PIN	VOLTAGE
16	+12 Volts
17	-12 Volts
34	Grou...

INTERNAL CALIBRATION CONTROLS



Section 4
OPERATING INSTRUCTIONS

4.1 GENERAL

1. The purpose of this section is to familiarize the user with the controls of the Model 2055 Logic Shaper and Delay and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

2. 50 ohm as well as 93 ohm coaxial cables and terminations may be utilized with the Model 2055.

4.2 INITIAL OPERATION

1. Insert the Model 2055 Delay Amplifier in on AEC compatible bin unit/power supply such as Canberra Model 2000. Set the Power switch to ON.

2. Set the 2055 Polarity Selector to Pos. Adjust a pulse generator for a +5.0 volt, 1 microsecond wide signal and connect it to the 2055 Input. Input rate to be < 5kHz.

3. Using an oscilloscope (use 93 ohm coax), monitor the Pos Output connector. Set the WIDTH control mid range and vary the AMPLITUDE control from CCW to CW and observe the pulse amplitude change from less than 2.0V to greater than 10.0V. The unterminated max. of 10.0V becomes 8.0V with 93 ohm termination and 7.5V at 50 ohm termination.

4. Set the AMPLITUDE control to mid scale and vary the WIDTH control. Terminate the cable in 93 ohms. When the WIDTH control is full CCW, the output pulse width should be less than 500 nanoseconds. Move WIDTH to full CW and observe the output signal width is 5 microseconds or greater.

5. Repeat Steps 3 and 4 observing the NEG Output signal.

6. Monitor the +PERIOD Output connector (terminate the cable with 93 ohms). Decrease the DELAY Control to full CCW. Set the Multiplier to X0.1. The output signal should be $\geqslant 4.0$ volts in amplitude and the width should be 100 nanoseconds. Turn DELAY to full CW and observe the output width should be 1.1 microseconds. Turn the DELAY control to 5.0 and observe the pulse width to be 0.5 microseconds. Switch the Multiplier to X1.0 and observe that the output width changes to 5.0 microseconds. Switch the Multiplier to X10 and observe that the output width changes to 50 microseconds.

7. Repeat Step 6 monitoring the - Period Output connector.

8. Monitor the Fast Output connector with the oscilloscope (terminate in 50 ohms). Trigger scope on the leading edge of +Period Output. Observe that Fast Output pulse occurs at end of Delay time setting. The pulse is approximately 20 nanoseconds wide and has a negative amplitude of 800mV.

4.3 INTERCONNECTIONS

Interconnecting between the various units in an experiment requires coaxial cables. These cables should be terminated resistively in their characteristic impedances. Failure to follow this requisite may result in ringing (several cycles of oscillation of varying amplitude at signal transition times) and/or spurious pulses appearing on the output. Both can initiate false triggering and subsequent erroneous experiment results.

INPUT and NEG PERIOD OUT on the rear panel are parallel connections to the front panel INPUT and –PERIOD output connectors, respectively. They are there to aid interconnecting to other units. Also, fewer cables to the front panel contributes to neatness of the installation.

Section 5
THEORY OF OPERATION

5.1 GENERAL

The Model 2055 Logic Shaper and Delay module generates several outputs whenever the input, positive or negative, crosses the threshold level. The + or –Period Output begins when the input is sensed and extends for the period selected via the front panel Delay Control. The trailing edge of this pulse initiates all the other Output pulses. These Outputs are a Positive and Negative logic signal with selectable Width and Amplitude and a standard negative Fast NIM logic signal.

The Model 2055 consists of: The Threshold Discriminator, Delay Monostable, +/–Period Output Buffers, Fast Negative Circuit, Width Monostable, Amplitude Adjust circuit, and the Negative and Positive Output Buffers. A timing sequence and block diagram are provided at the end of this description. Also refer to schematic diagram.

5.2 THRESHOLD DISCRIMINATOR

The threshold detector circuit is used to shape the input pulses which are above a certain level. The circuit uses a voltage comparator (A1) to detect the input level and to shape the pulses. This comparator is capable of taking relatively slow rise time or fast rise time pulses and shaping them into pulses with the same rise time. It is also used to inhibit the passage of pulses below –0.4 volts or +0.7 volts depending upon the input polarity selected. The Pos/Neg switch (S-2) is provided to allow the input of A1 to accept either positive or negative pulses. Diodes D1 and D2 protect the input of A1 from too great an input pulse amplitude.

5.3 DELAY MONOSTABLE

This monostable provides a variable width pulse which is adjusted by the front panel Delay controls. The leading edge of the threshold-circuit-pulse fires this monostable consisting of Q1, 2, 3, 6, 7, and 8. The actual monostable timing is sensed by Q1 and Q8. Q2 forces the monostable to reset quickly. Q7 provides quicker switching at the start of the Delay period. Q3 is an emitter follower providing approximately 5 volts to Q1C and Q2B. Q6 is the active element in the current source which linearly discharges the timing capacitors; C10, 11 in X 10 (10 to 110 microsec range); C12, 13 in X 1 (1 to 11 microsec range); C13 in X 0.1 (0.1 to 1.1 microsec range). RV1 is the internal calibration control for the current source. R3 is the front panel Delay control and its setting varies the current source over its 10 to 1 current range.

5.4 +PERIOD OUTPUT BUFFER

The output buffer provides a low impedance fast rise and fall time pulse with variable width to the +Period Output BNC. This buffer is made up of a pair of complementary emitter followers Q9 and Q10.

5.5 –PERIOD OUTPUT BUFFER

The output buffer provides a low impedance fast rise and fall time pulse with variable width to the –Period Output BNC's on the front and rear panels. This buffer is made up of a pair of complementary emitter followers Q11 and Q12.

5.6 FAST NEGATIVE CIRCUIT

This circuit provides a standard negative Fast NIM logic signal at the end of the delay period selected. The trailing edge of the delay monostable pulse is differentiated by CV1 (internal adjustment for setting the Fast negative output width) and R31. The negative portion of this pulse is fed to the drivers Q22 and Q23 and presented to the Fast Output BNC.

5.7 WIDTH MONOSTABLE

This monostable provides a means of adjusting the output width of the Positive and Negative Outputs. It consists of A2b, A2c, Q13, Q14 and is fired by the trailing edge of the delay monostable pulse. Q13, a current source, provides a constant current to the timing capacitor C9. By adjusting the Width control R4, the current to the timing capacitor is varied to change the time Q14 is ON and therefore the width of the monostable from 0.4 to 5 microseconds. RV2 is an internal adjustment to calibrate the Width control R4.

5.8 AMPLITUDE ADJUSTMENT CIRCUIT

This circuit controls the amplitude of the pulse, by a front panel Amplitude control, that is fed to the Negative and Positive Outputs. The output of the width monostable is fed through Q17. In the collector of Q17 is a voltage source Q18 which controls the amplitude of the pulse at the collector of Q17. This voltage is determined by R5, the Amplitude control. The pulse at the collector of Q17 is then fed to the Negative and Positive outputs through their buffers.

5.9 POSITIVE OUTPUT BUFFER

The Positive Output buffer provides a low impedance fast rise and fall time pulse with variable width and amplitude to the Positive Output BNC. This buffer is made up of a pair of complementary emitter followers Q15 and Q16.

5.10 NEGATIVE OUTPUT BUFFER

The Negative Output buffer provides a low impedance fast rise and fall time pulse with variable width and amplitude to the Negative Output BNC. This buffer is made up of an inverter Q19 and a pair of complementary emitter followers Q20 and Q21.

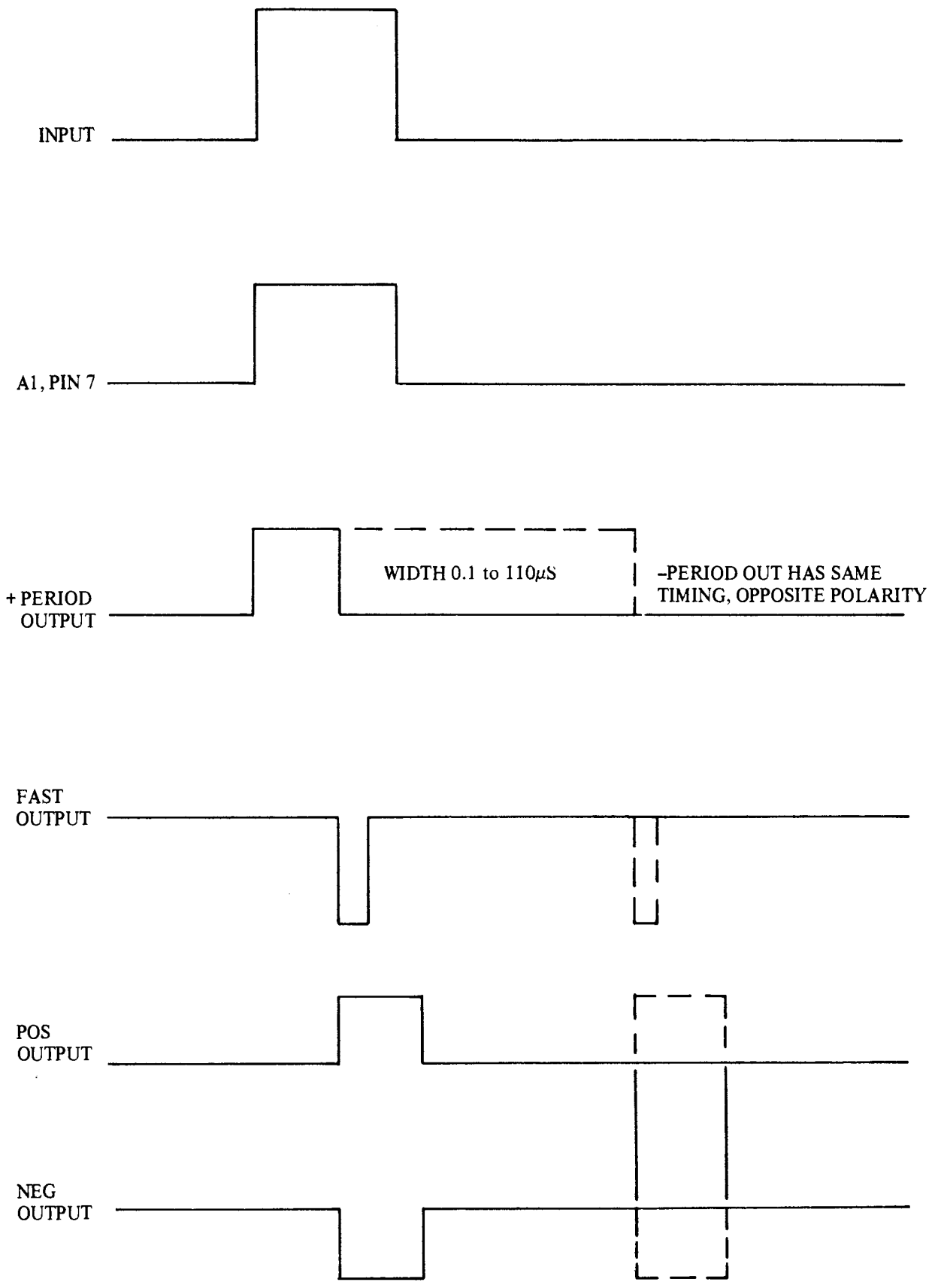


Figure 5-1. Model 2055 Timing Diagram

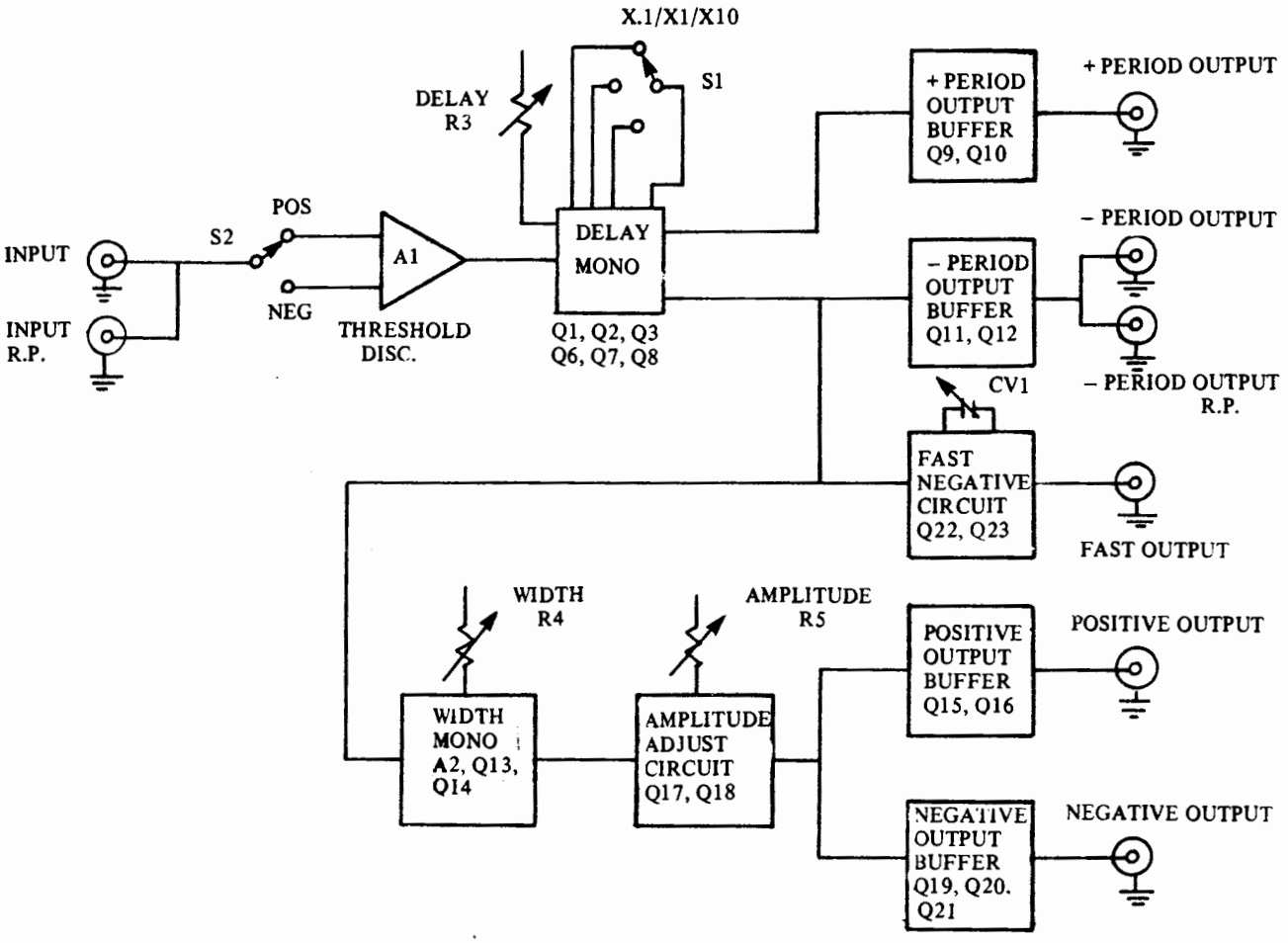


Figure 5-2. Model 2055 Block Diagram

Section 6
TROUBLESHOOTING

6.1 GENERAL

The purpose of this section is to provide the user with some guidelines on how to troubleshoot this instrument. It is not meant to be a comprehensive analysis of the circuit, but rather general outline of some quick tests that will help a qualified technician locate the problem.

6.2 EQUIPMENT REQUIRED

1. Pulse Generator (DATAPULSE Model 101, 110B, or equivalent)
2. Oscilloscope (TEKTRONIX 581, 454, 453, or equivalent)
3. Digital Voltmeter (± 0.1% of full scale accuracy)
4. Current Meters

6.3 INITIAL CHECK

1. Measure the dc voltage output of the NIM Bin. The Model 2055 requires ± 12 volts for operation.
2. Inspect the 2055 for opens and/or shorts across the power input connectors. Examine all connectors to front and rear panel. Look for shorts or damaged components on the PC board.

6.4 ELECTRICAL CHECK

1. Apply power to the unit and measure the supply currents. They should be:

   +12V – 100mA ± 20%
   −12V – 70mA ± 20%

   Measure by unsoldering the wires to WP27 (−12V) and WP38 (+12V) one at a time and connecting a DC current meter in series with the wire and its wire point (WP). A significant increase in current indicates a shorted component. Less current is probably an open connection. Carefully check the decoupling networks (see schematic).

2. Measure, with the digital voltmeter, A2 pin 14; it should be:

   +5V ± 0.25V

   This is the dc supply for all the integrated logic. The circuit consists of R8, D3, and C2.

3. Measure, with the digital voltmeter, Pin 4 of A1; it should be:

   −6.2 ± 0.6V

   This voltage is provided to the comparator by R13, D6, L4, and C7.

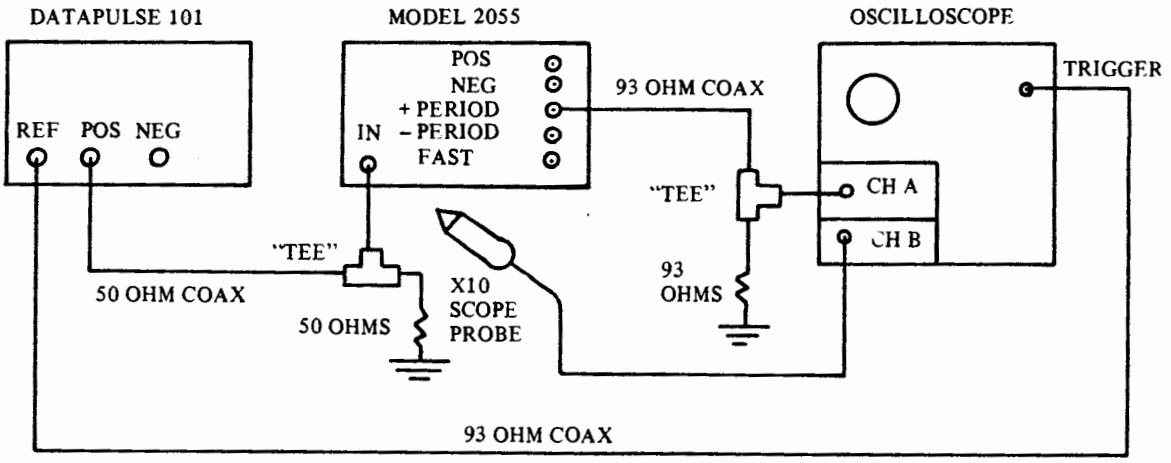
6.5 PERFORMANCE CHECK

6.5.1 SETUP

1. Datapulse Model 101 - Set the front panel controls as follows:

REPETITION RATE	-	5kHz
PULSE DELAY	-	Minimum
PULSE WIDTH	-	1.0μsec
AMPLITUDE (POS)	-	10V (fully CW)
AMPLITUDE (NEG)	-	10V (fully CW)
GATE MODE	-	NON-GATED
PULSE MODE	-	SGL (single)

2. Connect pulse generator to 2055 as shown below:



3. Waveforms - Output signal waveform widths are measured at 50% height and rise/fall times from 10% to 90% height unless otherwise noted.

6.5.2 THRESHOLD DISCRIMINATOR CHECK

1. Apply + 10V pulse to 2055 INPUT.
2. Set the 2055 POS/NEG switch to POS position.
3. Observe 2055 + PERIOD Output with the scope (terminated 93 ohms); a pulse greater than +4V should be present.
4. Decrease the pulser INPUT until the 2055 PERIOD Output just disappears; minimum positive INPUT should be +0.7V, ± 0.1V tolerance.
5. Set the 2055 POS/NEG switch to NEG position.
6. Apply –10V pulse to 2055 INPUT.
7. Observe Step 3 again, except monitor –PERIOD Output.

8. Decrease the pulser INPUT until the 2055 –PERIOD Output just disappears; minimum negative INPUT should be –0.4V, ± 0.1V tolerance.

6.5.3 DELAY MONO CALIBRATION (limited by oscilloscope time base accuracy)

1. + and –PERIOD Output times differ only by propagation delays. Therefore, calibration by observation of the + PERIOD Out is sufficient. Verification of several times at the –PERIOD Output should be carried out for assurance of the –PERIOD Output Buffer circuit operation.

2. The 2055 DELAY duo-dial knob is offset to read 1.00 at full CCW position.

3. Apply +10V pulser INPUT to 2055.

4. Set 2055 POS/NEG switch to POS position.

5. Observe 2055 + PERIOD Output with the scope (terminated 93 ohms).

6. Adjust 2055 DELAY for 110 microseconds (DELAY pot should read 11.00 and DELAY MULTIPLIER switch in X10 position).

7. Set scope for 20μsec TIME/CM.

8. Adjust RV1 for 2055 + PERIOD Output width of 110μsec, exactly. This is the only calibration adjustment.

9. Set scope for 10μsec TIME/CM.

10. Decrease 2055 DELAY pot to read 5.00; 2055 + PERIOD Output width should be 50μsec, ± 1μsec tolerance.

11. Decrease 2055 DELAY to minimum (1.00); the + PERIOD Output width should be 10 microseconds, ± 1μsec tolerance.

12. Set scope for 1μsec TIME/CM.

13. Set 2055 X0.1/X1/X10 switch to X1 position with DELAY pot at minimum (1.00).

14. + PERIOD Output width should be 1μsec, ± 0.12μsec tolerance.

15. Set DELAY pot to 5.00. + PERIOD output width should be 5μsec, ± 0.2μsec tolerance.

16. Set DELAY pot to 10.00. + PERIOD Output width should be 10μsec, ± 0.25μsec.

17. Set scope for 0.1μsec TIME/CM. Measure periods at 25% of peak height in steps 19, 20, and 21.

18. Set 2055 X0.1/X1/X10 switch to X0.1.

19. Set DELAY pot to 10.00. + PERIOD Output width should be 1μs, ± 0.07μs tolerance.

20. Set DELAY pot to 5.00. + PERIOD Output width should be 0.5μs, ± 0.03μs tolerance.

21. Set DELAY pot to 1.00. + PERIOD Output width should be 0.1μs, ± 0.03μs tolerance.

6.5.4 PERIOD OUTPUT CHECK

1. Apply +10V pulser INPUT to 2055.
2. Observe 2055 + PERIOD Output with the scope (terminated 93 ohms).
3. Decrease 2055 DELAY to minimum (100nsec).
4. Check 2055 + PERIOD Output amplitude; should be $\geqslant$ 4.0V.
5. Check 2055 + PERIOD Output rise and fall time; should be $\leqslant$ 25nsec.
6. Repeat 2 through 5 observing –PERIOD Out.

6.5.5 FAST OUTPUT CHECK

1. Apply +10V pulser INPUT to 2055.
2. Connect 2055 FAST Output to the scope with 50 ohm coax cable and terminated with 50 ohms at scope end of cable.
3. Set 2055 DELAY for 150nsec.
4. Observe the 2055 negative FAST Output and adjust CV1 for a FAST Output width of 20nsec at 50% of pulse peak height.
5. Check 2055 FAST Output amplitude; should be –0.78V to –1.0V.
6. Check 2055 FAST Output rise and fall time; should be $\leqslant$ 5nsec with Tektronix 454 scope or equivalent. Using Tektronix 581, 453, or equivalent, should be $\leqslant$ 10nsec.
7. Verify that the leading edge of the FAST Output is not delayed more than 100nsec from the trailing edge of the + PERIOD Output.

6.5.6 POSITIVE OUTPUT CHECK

1. Apply +10V pulser INPUT to 2055.
2. Set 2055 DELAY for minimum (100nsec).
3. Observe 2055 POS Output with the scope (use 93 ohm coax cable and terminate with 93 ohms at scope end of cable).
4. Adjust 2055 AMPLITUDE and WIDTH controls to maximum (fully CW).
5. Adjust RV2 for 2055 POS Output width of 5.0μsec exactly.
6. Decrease 2055 WIDTH control to 3.0; 2055 POS Output width should be 3.0μsec, ± 0.5μsec tolerance.
7. Decrease 2055 WIDTH control to minimum (fully CCW); POS Output width should be $\leqslant$ 0.5μsec.

8. Check 2055 POS Output rise and fall time with WIDTH at minimum and AMPLITUDE at maximum; should be $\leqslant$ 25nsec.

9. Check 2055 POS Output amplitude with AMPLITUDE Control at maximum; should be $\geqslant$ 8.0V (terminated 93 ohms), $\geqslant$ 10.0V (unterminated).

10. Decrease 2055 AMPLITUDE control to 6.0; 2055 POS Output amplitude should be 6.0V, ± 0.6V tolerance (unterminated).

11. Decrease 2055 AMPLITUDE control to minimum (fully CCW); POS Output amplitude should be $\leqslant$ 2.0V (unterminated).

12. Verify that the leading edge of the POS Output is not delayed more than 100nsec from the trailing edge of the + PERIOD Output.

6.5.7 NEGATIVE OUTPUT CHECK

1. Repeat 6.5.6 and verify that the NEG Output will meet all the requirements of Step 1 through 12, except voltages will be negative.

2. Do not readjust RV2 in 6.5.6 Step 5.