TIME ANALYZER
Model 2043

Operator's Manual

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M126R1 4/82 Printed in U.S.A.

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FIGURE LISTING

Section 1. Introduction

The Canberra Model 2043 Time Analyzer generates a rectangular analog output pulse whose peak amplitude over a 0 to +10 volt range is linearly proportional to the time interval between a START and a subsequent STOP input. Built-in features such as the Time Single Channel Analyzer, COINCidence/ANTICOINCidence gating, RESET, and STOP INHIBIT enhance the utility and flexibility of this module for the spectrum of nuclear analysis needs.

The basic time-to-amplitude conversion (TAC) is used to analyze correlations between random nuclear events that occur within a selected interval of time, for time of flight, positron lifetime, pulse shape analysis in particle studies, and for pulse pair timing in position sensitive detector systems. The Model 2043 offers 15 time ranges from 20 nanoseconds to 1000 microseconds to span these needs. The positive unipolar TAC output is essentially flattopped for accurate measurement by a multichannel analyzer ADC.

Internal gating prevents a TAC output pulse for (1) overrange START to STOP time differences; (2) STOP inputs received prior to an accepted START; and (3) START or STOP signals received during the converter busy time. The front panel OVERRANGE LED is illuminated for the first condition to simplify setup of the instrument.

The COINCidence/ANTICOINCidence gating feature permits prompt (early) gating of a START/STOP pulse pair and is best used to minimize conversion time on unwanted pulses. The GATE input must be received at least 10 nsec prior to and overlap the START input.

The RESET/INHIBIT input permits late anticoincidence gating. It is used to terminate a conversion cycle and prevent subsequent conversions while driven. This mode prevents a TAC output for slow energy analysis restrictions, for example.

For user convenience, the START, STOP, GATE, and RESET/INHIBIT inputs accept positive or negative NIM pulses without the need for polarity selection switches. The circuit provides an input impedance of 1k ohms or 50 ohms (internally selectable) for positive voltage signals, and 50 ohms nominal for negative NIM current pulses.

The rear panel STOP INHIBIT adjustment allows rejection of STOP input signals in a range of 1% to 100% of each time range. This is useful in suppressing noise inputs in some applications such as linear accelerators, and prevent false outputs. A MONITOR output is provided for the user to observe the lockout time following a START signal as a logic pulse width.

The single channel analyzer (SCA) portion of the Model 2043 operates on the TAC output pulse amplitude, and places equivalent timing restrictions on the time spectrum being accumulated. The "time window" of interest is adjustable from 0 to 100% of the selected time range by the settings of the front panel ten-turn locking dial potentiometers. An SCA logic output is produced for every TAC pulse whose peak amplitude is greater than the TIME dial setting, but less than the sum of TIME + Δ TIME settings. An internal jumper plug permits the user to gate the TAC output with the SCA directly, or to let the TAC output be generated normally.

The TAC and SCA output pulses may be delivered immediately upon completion of the START to STOP conversion by using the MINimum DELAY switch on the front panel, or may be delayed over a range of 0.5 to 10.5 μsec using a 22-turn screwdriver adjustment potentiometer. Both the TAC and SCA outputs are simultaneously adjustable in width (internal jumper plug for 0.5, 1.0, or 2.5 μsec) and the two outputs are synchronous, so timing jitter on the SCA output is essentially non-existent.

VALID START and VALID STOP auxiliary logic outputs are also provided. The VALID START output duration is the time interval between an accepted START input and the end of TAC reset time, and thus represents the full conversion busy time. The VALID STOP output duration is the time interval between an accepted STOP input, and the end of TAC reset time. Converter reset occurs after generation of a TAC output, upon receipt of a RESET/INHIBIT input, or upon detection of an overrange condition (no STOP input received within the selected time range). Reset time is a fixed 1 μsec on the X1, X10, and X100 MULTIPLIER ranges and 10 μsec maximum on the X1K and X10K ranges.

The VALID START, VALID STOP, SCA and MONITOR outputs are each available by internal selection as positive voltage pulses or negative fast NIM current pulses. The voltage outputs are also adjustable in peak amplitude for compatibility with interfacing instruments. Each positive output is source matched with a 50 ohm series resistive termination to prevent ringing due to reflections on unterminated cables, and the resulting multiple counting frequently experienced. The instrument is shipped with socketed resistors for each output which limit them to +5 nominal (open circuit) for direct interface to common TTL circuitry. The user may remove the resistors as desired to obtain a +8 V nominal open circuit voltage for instruments requiring the NIM pulse level, or +4 V nominal into the 50 ohm load termination which some other instruments provide. This flexibility allows the user to adapt the output signal to his needs without risking the problems encountered with improperly driven cables and critical timing pulses.

The TAC output signal is provided on the rear panel as a source matched 93 ohm output, and on the front panel as a 10 ohm output for use with short lenghts of cable (less than 1 meter) interfacing to an MCA. Both are direct coupled and essentially pedestal-free.

The START, STOP, and GATE inputs are accommodated on both front and rear panels. To prevent unterminated stub pulse reflections on these NIM fast low level inputs, the user selects the front or rear inputs via internal jumper plugs. The balanced 50 ohm termination is thus preserved on the desired line for maximum noise immunity and timing stability.

Section 2. Specifications

2.1 INPUTS

START—Accepts either a positive logic signal or dc level with amplitude ≥2 V, or a negative logic signal or dc level with amplitude ≥-250 mV; width ≥2 nsec at above limits; Z_{in} ≈1k ohm for positive signals (internally selectable by jumper plug to 50 ohms), and 50 ohms for negative signals; dc coupled; leading edge initiates time conversion cycle; front and rear panel BNC connectors.

STOP—Input specifications identical to START input; leading edge terminates time conversion cycle; see INTERNAL GATING LOGIC for restrictions; front and rear panel BNC connectors.

GATE—Accepts either a positive logic signal or dc level with amplitude ≥3 V, or a negative logic signal or dc level with amplitude ≥-500 mV; width ≥50 nsec; Z_{in} ≈1k ohm for positive signals (internally selectable to 50 ohms), and 50 ohms for negative signals, dc coupled; provides external means of gating the TAC output in either COINCidence or ANTIcoincidence. GATE input must begin 10 nsec prior to and overlap START input signal; front and rear panel BNC connectors.

RESET/INHIB—Input specifications identical to GATE input; serves as a late anticoincidence input and terminates conversion cycle; front panel BNC connector.

2.2 OUTPUTS

TAC—Provides positive flattopped rectangular unipolar pulse; constant shape independent of TIME RANGE or amplitude; amplitude proportional to accepted START/STOP input pulse time difference; adjustable delay (0.5 to 10 μsec) and width (0.5, 1.0, or 2.5 μsec); rise time ≈250 nsec; dc coupled; front panel Z_{out} <10 ohms and rear panel Z_{out} = 93 ohms BNC connectors. Output range 0 to 10 V for 0 to 100% of selected time scale.

VALID START—(converter busy time)—Provides internally selectable positive voltage pulse of 5 or 8 V, with rise and fall times of ≤25 nsec, or by another internal selection a negative current pulse of -16 mA with rise time of ≤5 nsec; Z_{out} = 50 ohms, dc coupled; duration equal to time interval between accepted START input and end of cycle reset time; front panel BNC connector.

VALID STOP—Output pulse specifications identical to VALID START; duration equal to time interval between accepted STOP input signal and end of cycle reset time; front panel BNC connector.

SCA—Output pulse specifications identical to VALID START; leading edge in time coincidence with, and duration equal to, TAC output; front panel BNC connector.

STOP INHIBIT MONITOR—Output pulse specifications identical to VALID START; provides observation of rear panel STOP INHIBIT RANGE adjustment, rear panel BNC connector.

2.3 PERFORMANCE

TIME RESOLUTION—<0.01% of full scale plus 5 psec FWHM for all ranges.

TAC INTEGRAL NONLINEARITY—< ±0.1% from 5 nsec to full scale on X1 MULTIPLIER range; < ±0.1% from 1% to 100% of full range for all higher ranges.

TAC DIFFERENTIAL NONLINEARITY—< ±2% from 5 nsec to full scale on X1 MULTIPLIER range; < ±2% from 1% to 100% of full scale for all higher ranges.

SCA TIME/Δ TIME INTEGRAL NONLINEARITY—< ±0.5% of full scale.

TAC OUTPUT TEMPERATURE STABILITY—better than ±0.01%/° C (±100 ppm/° C) of full scale.

SCA TIME/Δ TIME TEMPERATURE STABILITY—better than ±0.01%/° C (±100 ppm/° C) of full scale.

OUTPUT DELAY/OUTPUT WIDTH TEMPERATURE STABILITY—better than 0.01%/° C(±100 ppm/° C) of full scale.

TEMPERATURE OPERATING RANGE—0 to 50° C.

TAC OUTPUT DROOP—<0.015%/μsec of output delay on all ranges.

TAC RESET TIME—Fixed 1 μsec recovery time on X1, X10, and X100 MULTIPLIER ranges, and 10 μsec on X1K and X10K MULTIPLIER ranges; occurs after each normal output and each overrange.

GATE PEDESTAL—Essentially zero pedestal, factory calibrated.

SCA OUTPUT TIME WALK—None, with respect to TAC output.

MINIMUM START TO STOP CONVERSION TIME—≈2 nsec.

COUNT RATE CAPABILITY—All inputs and outputs are dc coupled for optimum count rate independence, maximum internal count rate is limited by the converter busy time (time interval between accepted START input and end of reset time).

INTERNAL GATING LOGIC—Prevents TAC output for (1) overrange STOP signals; (2) STOP signals prior to an accepted START, (3) START/STOP inputs during converter busy time (eliminates pulse pileup).

2.4 CONNECTORS

All signal connectors are BNC type.

Section 4.
Operating Instructions

4.1 GENERAL

The purpose of this section is to familiarize the user with the operation of the Model 2043 Time Analyzer and to check that the unit is functioning correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

4.2 INITIAL CHECKOUT

Before attempting to use the Model 2043 Time Analyzer, the user should remove the left side-cover of the instrument and set the internal jumper plugs to provide the desired input and output characteristics. Reference Section 3.4 for the locations of these jumpers. It is recommended that these selections be performed with the power OFF.

Inputs:

The START, STOP, and GATE inputs are each accommodated by selecting individually the use of the front or rear panel BNC connectors provided. The front and rear BNC's are not wired together because the unused (unterminated) line presents a stub reflection to the fast logic signal wavefront, and the resulting ringing will deteriorate instrument performance. Therefore, the user must set the jumper plugs for START, STOP, and GATE inputs to either REAR or FRNT (front) as desired.

The input circuits for START, STOP, GATE, and RESET/INHIBIT each accept positive voltage or negative current NIM pulses without the need for polarity selection switches. The input impedance for the negative current pulse is a nominal 50 ohms. The input impedance for the positive voltage pulse may be set for an effective 50 ohms, or 1k ohms, to accommodate the characteristics of different sourcing equipment. The user should select the 50 ohm impedance if the input pulse is to come from an instrument having an output impedance of less than 10 ohms. This will minimize reflection-induced ringing which could cause a degradation of performance in the Model 2043 due to its very sensitive input circuits. For use with instruments which provide a 50 ohm nominal output impedance, the 1k ohm position of the jumper plug is recommended.

Outputs:

The VALID START, VALID STOP, SCA AND MONITOR outputs each may be selected individually to provide the specified positive voltage or negative current NIM pulse to represent their specific functions. The positive voltage pulse may further be selected to source either a 5 V or 8 V (nominal) open-circuit voltage level to accommodate the threshold and interface needs of other instruments. The positive voltage pulse output provides a 50 ohm nominal source impedance to prevent ringing and pulse reflections, which can cause spurious effects or multiple pulse counting. The negative current-pulse output is shunt terminated in 50 ohms (nominal) for the same reason.

The user may select the positive voltage pulse by setting the appropriate jumper near the identified output to +, and the negative current output by setting to -. The positive voltage pulses are normally set to 5 V, and can be individually increased to 8 V by removing a socketed 1.5k ohm resistor near the output function jumper.

SCA IN/SCA OUT:

The Time SCA function may be used to simply generate the logic SCA output pulse; it may also be used to gate the TAC output. The user should set this jumper plug as desired: SCA IN to have the SCA gate the TAC output, SCA OUT to have the SCA function by itself only.

Width:

The TAC output pulse may be set for a nominal width (at the 50% level) of 0.5, 1.0, or 2.5 microseconds to accommodate the pulse requirements of the ADC being used. In each case, the risetime of the output pulse is controlled to 0.25 microseconds to prevent slew-rate induced errors in the peak detector of the ADC. The user should set the WIDTH jumper plug into the sockets corresponding to the desired pulse width. Note that the SCA output pulse (either positive or negative) will have the same width as the TAC output.

Once the internal jumper plugs have been set to provide the input/output characteristics desired, the user should make external cable connections to the instrument to set up a familiarization test. Again, these connections should normally be done with power OFF.

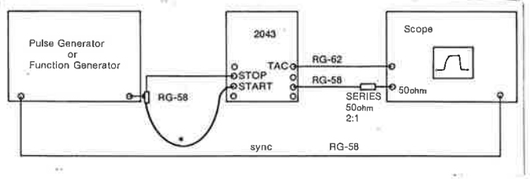


Figure 4-1a
Checkout Setup

*Note: Because of the internal analog and logic propagation delays of the Model 2043, a cable about 3m (10 feet) in length should be used between the tee connector and the START input to obtain a useful TAC output using this setup.

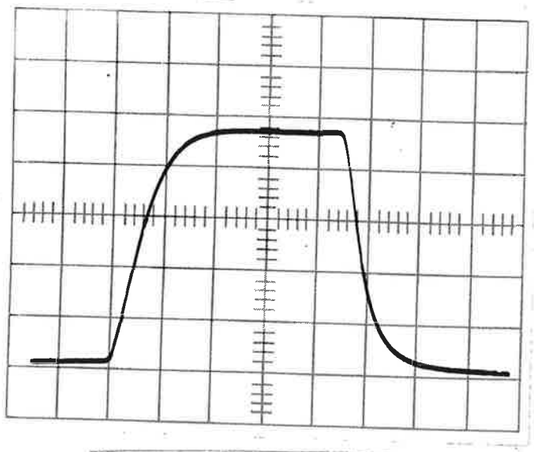


Figure 4-1b
Typical TAC Output Signal

The most straightforward method to verify proper operation and/or calibration of the Model 2043 Time Analyzer is to apply a known fixed-frequency pulse to both the START and STOP inputs and to observe the amplitude of the TAC output. As illustrated in Figure 4-1, a pulse waveform (either positive or negative) is first applied to the STOP input and then linked by a "tee" to the START input. The input signal should be adjusted to deliver ≥2 V if using positive signals, and ≥ -250 mV for negative signals. Note that with START and STOP linked together, the net input impedance will be reduced to as low as 25 ohms in this demonstration, and will attenuate a pulse generator's normal output. The small skew delay of the cable, and internal gating of the Model 2043, will force the instrument to recognize a START-STOP pair with a time difference equal to the period (inverse of frequency or pulse rate) of the input.

For a reference condition, a 1 MHz pulse with a width of up to 0.5 microseconds, or a suitable square wave from a laboratory function generator, may be used initially. It is suggested that the Model 2043 be configured as follows:

Internal Jumpers:
- START, STOP, and GATE each to FRNT
- all impedance jumpers set to 50 ohms
- SCA initially OUT
- WIDTH initially 1 μsec
- all +/- jumpers initially to +

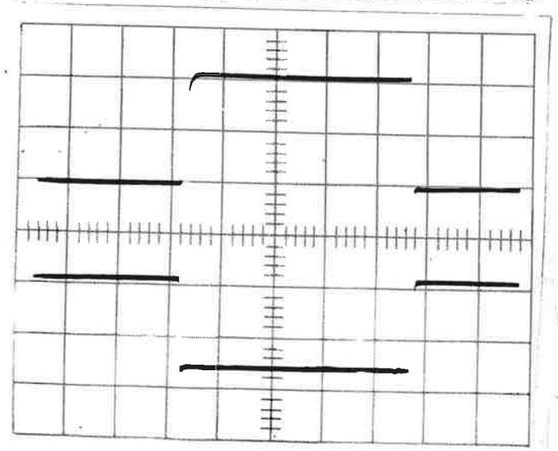
Front Panel:
- TIME RANGE to 20
- MULTIPLIER to X100
- COINC/ANTICOINC to ANTICOINC
- DELAY to MIN

Rear Panel:
- STOP INHIBIT to OFF

Given the above setup, the user should observe a TAC output pulse of 5 V peak amplitude on an oscilloscope. A change in the frequency (rate) of the applied input will then result in a proportional change in the amplitude of the TAC output. By reducing the rate to approximately 0.45 MHz (2.2 microsecond period), the user may verify that the TAC output disappears and the front panel OVERRANGE indicator will come on.

With the DELAY switch in MINimum, the TAC and SCA output pulses will be seen to occur 150 nsec (nominal) after the STOP input pulse. With the DELAY switch in VARiable, these two output pulses can be seen to vary between 0.5 and 10.5 μsec (nominal) after the STOP input pulse, depending on the adjustment of the direct reading ten-turn DELAY potentiometer.

At this point the user may examine the VALID START, VALID STOP, and SCA output pulses (see discussion of SCA below) in either + or - modes. Figure 4-1 illustrates the proper method of connection to use when observing these outputs on an oscilloscope. Figure 4-2 illustrates typical SCA output pulses using the prescribed termination; Figure 4-3 illustrates the aberrations caused by ungrounded oscilloscope probes (top) and oscilloscope input capacitance on direct viewing (bottom).

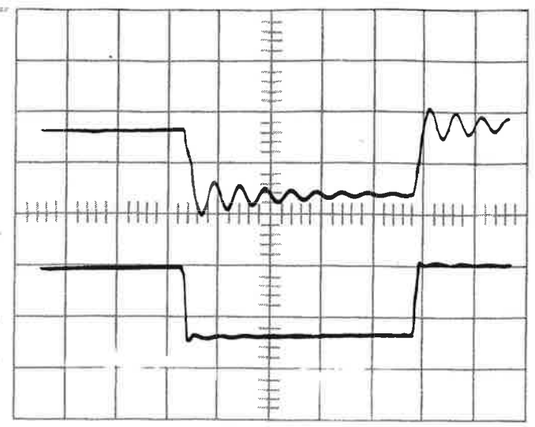


Upper: + 2 V/cm.

Lower: -0.2 V/cm.

Horizontal: at 100 nsec/cm.

Figure 4-2
Typical SCA Output Pulses



Upper: Ungrounded Scope Probe

Lower: At scope without proper termination

Vertical.: at 0.5 V/cm.
Horizontal.: at 100 nsec/cm.

Figure 4-3
SCA Output Pulses

4.3 USE OF SCA FUNCTIONS

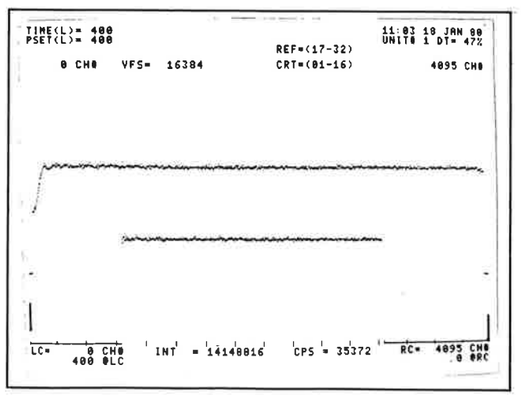
The Time Single Channel Analyzer function is most commonly used to restrict the spectrum of pulse pairs received by the instrument to a narrow range of most interest in a given experiment. These may represent coincidences from several detectors representing particle disintegrations, annihilations, lifetimes, etc. The Time SCA function evaluates the result of a given time-to-amplitude conversion and generates a logic output for input time differences within the bounds set by the front panel controls.

The TIME control on the front panel sets the lower limit for the SCA region or window, as scaled from 0 to 100% of any selected time range. The Δ TIME control sets the width of the SCA window over the same 0 to 100% range, so that the upper limit of time is read as the sum of TIME + Δ TIME dials.

The logic output decision of the SCA function may be used to gate the TAC output so that only those pulses within the set SCA limits will be delivered to an external ADC for analysis. This is done by moving the internal SCA OUT jumper to SCA IN.

Using the setup of Section 4.2, if the user will move the jumper to SCA IN, and set the front panel TIME dial control to 2.0 and the Δ TIME dial control to 6.0, an oscilloscope observation of the TAC output will be seen only for pulses between 2.0 and 8.0 volts as the input test frequency is varied up and down.

Figure 4-4 depicts the differential nonlinearity of the Model 2043 as observed on a Canberra Series 80 MCA using random noise pulses to generate a time spectrum on the 100 nanosecond range, and with the SCA set as above. The sharp skirts of the spectrum attest to the precision of the SCA as built into the Model 2043.



UPPER TRACE:
without SCA

LOWER TRACE:
SCA IN, with
TIME = 2.0
Δ TIME = 6.0

Figure 4-4
100 nsec Differential Nonlinearity

4.4 USE OF THE STOP INHIBIT FUNCTION

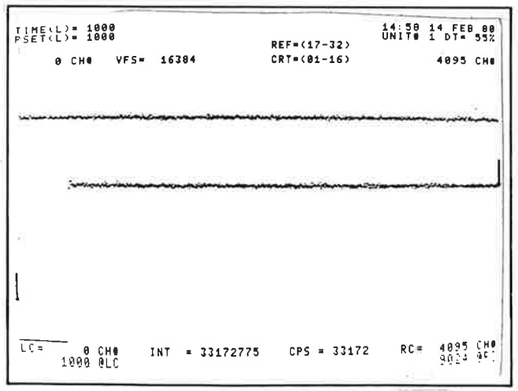
It is possible in some experiments to have STOP pulses that are caused by, or contaminated by, noise or by pulse reflections. If these unacceptable STOP pulses were not rejected in some way, they would initiate unintended time analysis cycles, contribute to the Time Analyzer's dead time, and thus affect the high throughput qualities of the Model 2043.

The self-contained Time SCA would reject these STOP pulses by creating a time window which would restrict the TAC output to acceptable pulse pairs. However, this would still incur increased dead time and possibly block time analysis on a desired START/STOP pair.

The STOP INHIBIT function has been designed to overcome this limitation by setting a "time threshold" which begins with an accepted START pulse and is adjusted by the operator to end just before an acceptable STOP pulse. The Time Analyzer will not recognize STOP pulses which are below this threshold.

By careful adjustment of the STOP INHIBIT control, unacceptable (early) STOP input pulses can be suppressed, Time Analyzer dead time reduced and the generation of false TAC outputs avoided. As an aid in setting the Inhibit threshold, there is a MONITOR output BNC which provides a logic pulse whose width is equal to the blocking time interval following an accepted START input pulse.

Figure 4-5 illustrates the effect of a STOP INHIBIT set at approximately 10% of the 1 microsecond range of the Model 2043, as seen of a flat time spectrum using random pulser inputs.



UPPER TRACE:
Typical 1 μsec time spectrum.

LOWER TRACE:
Same as above with STOP INHIBIT set to approximately 10% of full scale.

Figure 4-5
Effect of STOP INHIBIT on a Time Spectrum

4.5 USE OF THE COINCIDENCE FUNCTION

The most common use of the Coincidence function is for early (prompt) gating of START/STOP pulse pairs as an aid in reduction of the Time Analyzer's dead time. Since the internal logic of the Analyzer is set to reject any STOP pulses that arrive before an accepted START pulse, a means of accepting or rejecting a START pulse will allow the operator to control pulse pair conversion.

By selecting one of the two modes of gating and applying a specified signal to the selected front panel or rear panel GATE connector, the operator can enable or disable the acceptance of a START pulse, and thus the conversion of any pulse pairs, depending on the established criteria of a given experiment.

In the COINCidence mode, an applied GATE signal will enable the operator to select a START pulse for beginning a conversion cycle by causing the GATE signal to coincide with the selected START pulse. Noncoincident pulse pairs will not be processed by the Analyzer.

In the ANTICOINCidence mode, the GATE signal will inhibit the acceptance of a START pulse and prevent the occurrence of an undesired conversion cycle. All other pulse pairs will be converted.

In either mode, an applied GATE signal will affect acceptance of a START pulse if the GATE signal is received at least 10 nsec prior to the START pulse and overlaps it by approximately 50 nsec.

Note that if the Coincidence function is not to be used, the mode switch must be left in the ANTICOINCidence position and the GATE input must be left open.

Section 5.
Circuit Description

5.1 GENERAL

The Canberra Model 2043 provides time analysis be using the time interval between accepted START and STOP input signals to gate a precision current into a selected integrating capacitor. The voltage accumulated on this capacitor from the impressed charge (current x time) is gated to the output as a rectangular analog voltage pulse whose peak amplitude is directly and linearly proportional to the input time interval. This OUTPUT is most commonly fed to the ADC (analog to digital converter) input of a multichannel pulse height analyzer for data accumulation and display of the time spectrum being studied.

The paragraphs which follow detail the operation of the various sections of the Model 2043 circuitry, and explain design features which assure consistent excellence in performance.

5.2 INPUT CIRCUITS

The START, STOP, GATE and RESET/INHIBIT inputs of the Model 2043 are designed to provide the user new degrees of latitude and flexibility in instrument interface. The circuit configuration is essentially identical for each of these inputs and is described here for the START input.

A START signal may be introduced from either the front or rear BNC connectors. To prevent unnecessary ringing and amplitude/timing distortions from stub reflections when using a very fast low level inputs signals, only one cable is used at a time. The user selects this input by setting a jumper plug on the printed circuit board adjacent to the receiving circuit to either FRONT or REAR.

The receiving circuit consists of a pair of high speed transistors configured to accept either a positive NIM voltage pulse ($\geq$ 2 V), or a negative NIM current pulse ($\geq$ -5 mA). Q6 is prebiased as a common-base stage to accept the negative current pulse. Its emitter resistor sets the circuit input impedance at a nominal 50 ohm level for such negative currents, but immediatety reverse biases to high impedance for positive signals. The collector current of Q6 is used to sink the clock input of the START flip-flop A4b and thereby initiate a time conversion cycle. Prebias for Q6 and several other devices is provided by Q12.

Positive voltage pulses are accepted by Q7, which operates as a saturating inverter to sink the clock input of A4b as above. The positive input impedance is nominally 1k ohm, with D2 steered by a second jumper plug to the +5 V supply to clamp positive-input overvoltages. To provide a nominal 50 ohm impedance (when desired) for positive voltage pulses, D2 is steered by its jumper plug to ground such that the emitter resistor of Q6 will again yield the desired termination.

The GATE input cascades a second stage of the above steering logic, and remotely enables the common base Q4 for the ANTICOINCidence mode of gating, or the inverter Q5 for the COINCidence mode. In this manner a positive voltage or negative current input signal is first normalized in polarity at the collectors of Q1/Q2, and then steered to the desired polarity for enabling (COINC) or inhibiting (ANTICOINC) recognition of a START pulse by controlling the J input of flip-flop A4b. This early gating requires application of a GATE input at least 10 nsec prior to and slightly overlapping the START pulse that is to be gated. In ungated operation, the mode switch is left in ANTICOINCidence; Q1 through Q5 will be off, and the J input of A4b is thereby enabled.

5.3 CONTROL LOGIC

Given an enabling logic high on both the J input and CLR to A4b, a START pulse sinks the clock input and sets the flip-flop (Q high, $\overline{Q}$ low). The Q output now enables the STOP channel flip-flop A5a by driving its J input high, (thereby inhibiting any STOP signal received prior to a recognized START) and switches off the clamp Q15 prior to ramp initiation. The Q output of A4b clocks A4a to set the latter's output. This cascaded structure provides a propagation delay to assure proper clamp switchoff, and matches the delay incurred in the STOP flip-flop A5a. STOP input pulses are skewed to match the START flip-flop A4b by using A5a in a self clearing pseudo-monostable mode. The clock inputs of A4b and A5b are each prebiased to $\approx$2.5 V to enhance response to narrow input pulses.

With the START and STOP latching pulse edges now skew adjusted at the $\overline{Q}$ outputs of A4a and A5a respectively, the time interval between the applied pulses can toggle a differential current-switch to gate a precision current into a capacitor. Q18 and Q19 level translate the TTL signals to the bases of Q16 and Q17, which form that differential current-switch.

The $\overline{Q}$ output of STOP flip-flop A5a initiates a variable DELAY one-shot in A7a. This one-shot allows full settling of the charge integrator after current gating, and provides a convenient dead time for external gating functions related to acceptance of the output pulse in a multichannel analyzer. At the end of this delay period, a second one-shot in A7b is initiated to strobe the settled analog voltage to the output. An internal jumper plug may be set for a strobe pulse width of 0.5, 1.0, or 2.5 μsec, as desired, for compatibility with the ADC being used. The gating between A7a and A7b is set to recognize the end of A7a's delay pulse, but to prevent the rising edge of a CLEAR pulse during an overrange correction from causing a false strobe-pulse. Specifically, the turn-on delay of Q22 permits only a narrow ($<$30 nsec) window at the end of A7a's pulse in which the A and B inputs of A7b are respectively low and high such as to permit triggering the one-shot. Under all other conditions A7b cannot fire.

A6b responds to the falling edge of A7b's strobe pulse to trigger the reset pulse. The width of this pulse is nominally 1 μsec on the X1K and X10K positions by switching on Q23 to add C35 in parallel to C34. The Q output of A6b drives Q24, which provides the higher sinking current required to clear A4a, A4b, and A5a. The width of the reset pulse is keyed to the capacitor being discharged by clamp Q15 to assure full settling of all elements prior to the next conversion. Q15 is normally on between conversions, driven by the reset (low) Q state of A4b. Capacitor C33 provides a small skew delay on Q24 to prevent the clamp action from inducing any transient on the end of the flat-topped OUTPUT pulse.

An overrange condition is detected by A3, which monitors the dc voltage level on the selected integrating capacitor. A3's Q output on pin 7 fires a one-shot to illuminate the front panel LED, and also generates an immediate reset pulse to speed-up circuit recovery for the next conversion. This pulse directly drives Q24 to clear flip-flops A4a, A4b, and A5a, and also drives Q11 on to immediately clear any timing cycles underway in A7a or A7b. As the integrating capacitor voltage decays during discharge, A3 pin 7 returns low, and Q11 returns high, thereby forcing a full-width reset pulse in A6a by triggering its B input. The integrating capacitor is now assured of a full discharge before the next conversion is begun.

5.4 INTEGRATOR

As discussed above, Q18 and Q19 form a level translator between the Q outputs of START and STOP flip-flops and the differential current switch Q16/Q17. R49 prebiases Q19 on (Q18 off) between conversions, such that the integrating current is normally steered thru Q17 to ground. A low on the START Q at A4a pin 7 switches on Q18 and thereby Q16 (Q19 and Q17 off) to steer the desired current to the selected integrating capacitor. A low on the STOP Q at A5a pin 7 reverts the states of Q16 through Q19 to the earlier condition and halts the integration.

Two small embellishments of note in the integrator enhance linearity and stability on the shortest time conversion ranges. D8 and D11 limit the cutoff bias on the clamp transistor Q15 in a bootstrap manner from the buffered integrator voltage, and minimize voltage sensitive capacitance changes in the base-emitter of Q15. Secondly, CV1 couples a charge from flip-flop A4b which compensates the switching charge in Q15 and prevents a low-end offset error which would limit linearity and sensitivity to very short time intervals. The result of these efforts is a useable sensitivity to below 2 nsec, and a differential linearity flat to below 5 nsec.

5.5 OUTPUT AMPLIFIER

The integrator voltage, buffered as above, is gated to the output by the action of the quad set of shunt analog switches in Q28 through Q31. All switches are current-driven through Q33 by the strobe pulse from A7b as discussed above. The first pair of switches (Q28 and Q29) are operated as normal mode shunts for lowest "on" resistance. The second pair (Q30 and Q31) are operated in the inverting mode for lowest offset voltage. This complement drives the input of A1 differentially to minimize switching transients and cancel the switch offsets by common mode rejection. Q32 provides the current boost to drive external low impedance loads through coaxial cable.

The compensation around A1 has been set to permit a fast, controlled pulse rise-time without any preshoot or overshoot which would interfere with proper pulse capture by an ADC. This network includes C40 and C41 to equalize and smooth the switching charge transients in Q30/Q31, and C42 and C45 to shape the pulse rise time and balance the inputs to A1.

The series output resistors R101 and R102 are used to prevent cable capacitance from causing oscillation in the output amplifier due to uncontrolled phase lags. R101 permits short lengths ($<$ 1 meter) of coax to be used to connect from the front panel to an ADC input. R102 provides a source matched 93 ohm output on the rear panel for use with longer lengths of coax. The series resistor will diminish the net voltage presented to the ADC somewhat, but may be the most advisable interface in some setup conditions.

5.6 LOGIC OUTPUTS

The VALID START signal is derived from the start flip-flop A4a $\overline{Q}$ line to represent the interval between the acceptance of a START input and the beginning of reset. The reset pulse width from A6b is then OR'ed with the above width in A11d to drive a discrete totem-pole output stage for positive NIM voltage outputs via Q42, Q43, and Q44, and to drive a fast complementing current switch via Q45 and Q46 to generate the fast negative NIM current pulse.

The VALID STOP signal is derived similarly using the stop flip-flop A5a $\overline{Q}$ line as OR'ed with the same reset pulse width in A11a, to drive a similar output network using Q47 through Q51.

The SCA output pulse is derived by using the selected width of the TAC output as generated in A7b to strobe a set of comparators A12 and A13 which are set up to monitor the analog ramp voltage from the time conversion. The front panel TIME control presents a lower-level limit through A10 to the reference input of A13. The selected voltage from the TIME control is summed with that from the Δ TIME control in A9 to present an upper-level limit to the reference input of A12. The width pulse from A7b strobes A13 first to determine if the analog ramp voltage from the time conversion is above the upper limit. If it is not, A13's output drives Q36 to strobe A12 to determine if the ramp is likewise above the lower level limit. If it is, A12 generates a drive pulse to provide a positive and negative output pulse as above for the VALID START, using Q52 through Q56.

When it is desired to have the SCA logic pulse gate the analog TAC output, A13's drive pulse is coupled via the SCA IN jumper to drive Q33 and the analog switches Q28 through Q31. Thus, the same selected-width pulse is routed thru the SCA comparators to gate the TAC output.

The STOP INHIBIT function is accomplished in comparator A2, which fires when the ramp voltage exceeds a reference level set by the rear panel RANGE control. The MONITOR pulse is initiated by an accepted START input (A4a Q drives Q35 on and sets the positive and negative outputs), and terminated by A2 as it switches on Q34 and cuts off Q35. A2's Q output is simultaneously fed to the J input of the stop flip-flop A5b to enable the next applied STOP input.