SPECTROSCOPY AMPLIFIER
Model 2020

0187

Operator's Manual

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Section 1. Introduction

Functionally, the Model 2020 provides in a double width NIM module, an exceptional spectroscopy amplifier, a gated, active baseline-restorer, a pulse pileup rejector and a live time corrector. The amplifier's excellent dc stability, ultra low noise, broad gain-range and wide choice of shaping time-constants makes it ideally suited for applications involving Germanium, Silicon, Scintillation, Gas Proportional and Surface Barrier detectors.

Canberra's near-Gaussian filter shaping has been refined in the Model 2020 for improved pulse symmetry, minimum sensitivity of output amplitude to variations in detector rise time, and maximum signal-to-noise ratio. For a given shaping-time constant, the improved pulse symmetry minimizes the pulse dwell-time by tucking in the trailing skirt of the unipolar pulse shape. This allows a faster return to the baseline. The result is superior energy resolution, count rate and throughput performance. Unipolar shaping is achieved with one differentiator and two active filter integrators. The differentiator is placed early in the amplifier to insure good overload recovery. The integrators are placed late to minimize noise contribution from the gain stages. The amplifier offers 12 front panel switch selectable pulse SHAPING time constants of 0.25, 0.5, 1, 1.5, 2, 3, 4, 5, 6, 8, 10, and 12 μsec, and allows optimum resolution/count rate performance. A front panel adjustable pole/zero can be user trimmed to match the preamp fall-time constant and minimize undershoot following the first differentiator for improved overload and count-rate performance.

Simultaneous UNIPOLAR and BIPOLAR outputs are available at both front and rear panel BNC connectors. The unipolar output includes a baseline restorer which samples the output signal and maintains the baseline at reference ground. The baseline restorer allows the unipolar output to appear dc coupled by imposing the unipolar output signal on a corrected dc level, 0 ± 5 mV dc. Thus, to realize best spectroscopy performance, the UNIPOLAR output should always be used when interfacing to dc coupled ADCs. The BIPOLAR output is normally used for crossover timing applications. To obtain the proper UNIPOLAR/BIPOLAR crossover timing relationship, used with coincidence timing systems, a 2 μsec or optional 4 μsec UNIPOLAR output delay is provided, jumper selectable.

The gated dc restorer offers automatic features on both the restorer threshold and restorer rate, assuring the best possible low and high count-rate performance. Amplifier performance is very much dependent on the restorer rate and threshold settings. The Model 2020 includes circuitry which automatically and continuously samples the amplifier output noise and count rate, and automatically sets the respective restorer threshold and rate with precision for optimum performance. The restorer is also flexible. The discriminating researcher can override the automatic restorer features. Setting the RESTORER RATE and THRESHOLD switches to their manual positions, HIgh and VARiable respectively, allows manual operation of the restorer. A front panel LED is provided as a user aid for setting the restorer threshold manually.

The flexibility of the restorer is further enhanced by providing SYMmetrical or ASYMmetrical restorer selection. The symmetrical restorer mode is used for detector systems which exhibit baseline discontinuities resulting from excessive noise and/or high-voltage effects, preamp reset pulses and preamp secondary time-constants. The asymmetrical restorer mode virtually eliminates charge accumulation and correlated noise on the restorer holding capacitor. This restorer mode is especially suited for use with high resolution detector systems that exhibit minimal baseline discontinuities and whose signals have a clean monotonic return to the baseline. The result is superior resolution/count rate performance when compared to more conventional methods.

The internal live time corrector and pileup rejector provides the capability of quantitative gamma spectrum analysis nearly independent of system count rate. By connecting the ADC's Linear Gate (LG) signal to the Model 2020 and connecting the Model 2020's REJECT and Dead Time (DT) signals to the ADC and live timer, the Model 2020 and associated ADC together perform pileup rejection and live time correction. During the amplifier and ADC processing time, the Model 2020 inspects for pileup and permits the ADC to convert only those detector signals resulting from a single energy event. To compensate for pulses rejected, amplifier and ADC dead times, a system dead time is generated by the live time correction function. The system dead time is the composite dead time of the ADC and Model 2020, extending the collection time by the appropriate amount. A front panel LED is provided as a user aid for setting the PUR DISCriminator.

1.1 APPLICATIONS

This section is not intended to serve as a complete list of applications. It is intended to identify some of the important features, and to indicate areas where they might be applied.

The Model 2020 Spectroscopy Amplifier's selection of shaping-time constants allows it to be used in surface barrier, proportional counter, NaI and Ge detector applications. The choice of shapings also allows the best possible performance by tailoring the system for the conflicting requirement of optimum signal-to-noise ratio and high count-rate performance. The excellent stability and low noise contribution enhances the use of this amplifier in most applications.

1.1.1 High Count Rate Systems

Normal passive restorers fail at high rates simply because of increasing undershoot observed as the count rate goes up. The gated restorer in the Model 2020 accumulates very little signal charge on its holding capacitor, thus minimizing the undershoot following a series of piled up pulses. This allows excellent resolution at high count-rates. Loss of resolution at high count rates is virtually non-existent if the pileup rejector is used.

1.1.2 Pileup Rejection/Live Time Correction System

Nuclear spectroscopy with high count rates can be made more accurate by testing for pulse pileup and rejecting contaminated pulses. Pulse pileup produces distortions in the higher ranges of the spectrum because successive shaped amplifier pulses tend to merge, and cause aberrations in the precise amplitude of any single pulse as measured by the ADC. Since many spectra have higher count rates at the lower energies, the pileup of these pulses strongly affects the less intense higher energy counts and can result in significant errors. A pileup reject circuit provides substantial improvement to the spectrum.

If pulses are rejected from further analysis by the circuitry, the system is "dead" for some portion of time. It is customary to correct for dead or busy time in the ADC; this dead time should also be activated when a pileup reject circuit is operated with the ADC. The Model 2020 provides the capability for activating the dead time signal when pileup occurs.

Typical applications are shown in Figure 1.1 and 1.2 for two systems, with Ge and NaI(Tl) detectors.

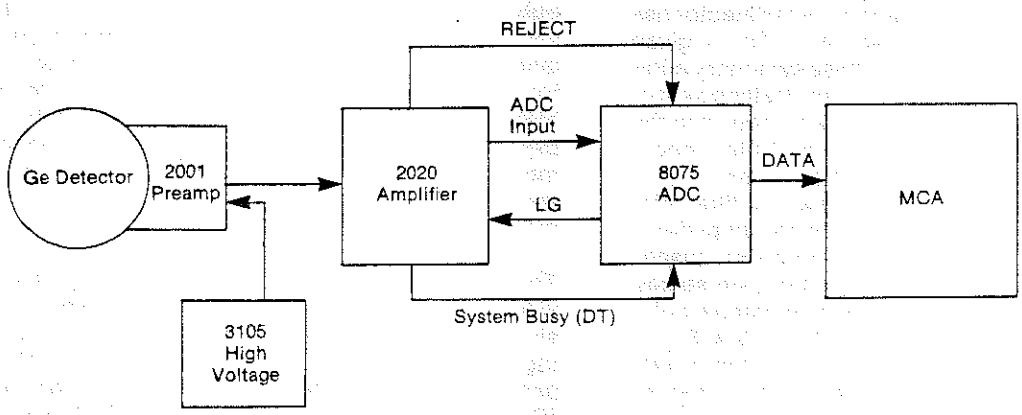


Figure 1.1
Ge Detector and External ADC System

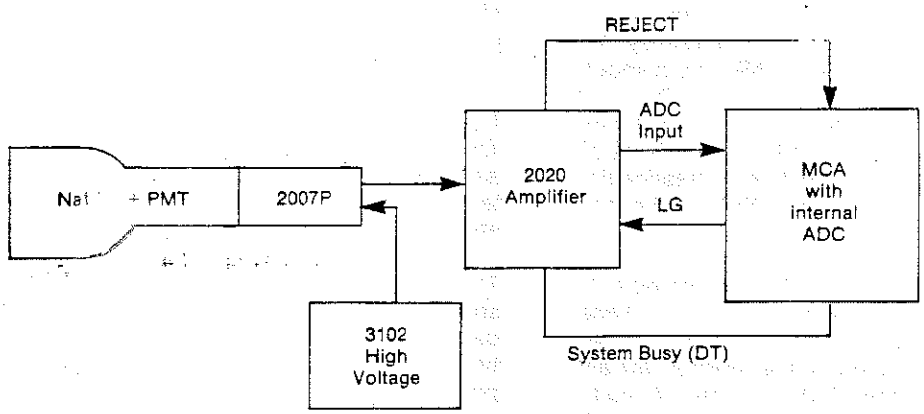


Figure 1.2
NaI(Tl) Detector and MCA System

Section 2.
Controls and Connectors

A complete understanding of the purpose of the various controls and connectors is essential for proper operation of the Model 2020, and it is recommended that this section be read before proceeding with module operation.

2.1 FRONT PANEL CONTROLS

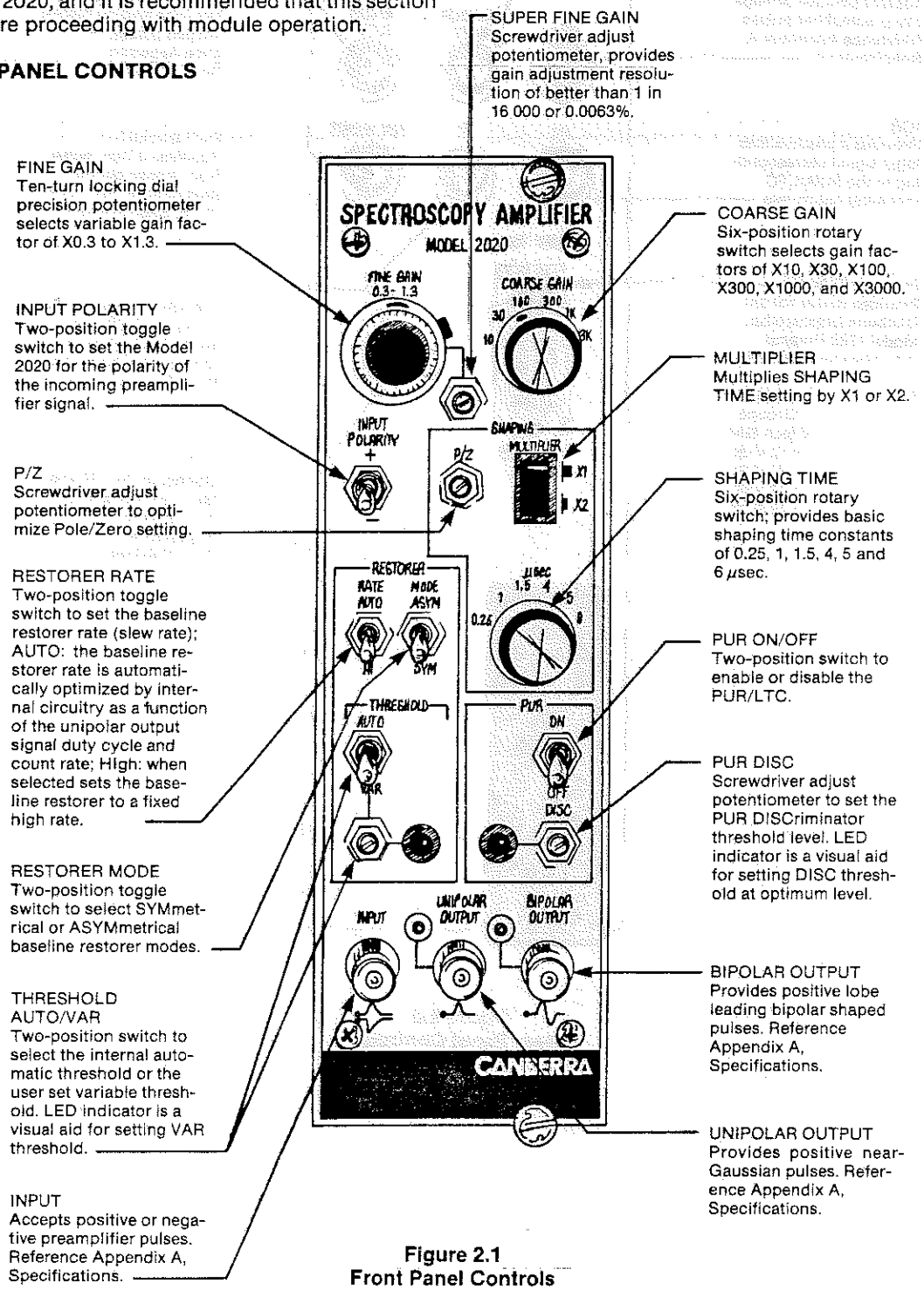


Figure 2.1
Front Panel Controls

2.2 REAR PANEL CONTROLS

UNIPOLAR OUTPUT
Parallel connected to front panel UNIPOLAR OUTPUT; provides positive near-Gaussian pulses. Reference Appendix A, Specifications.

INPUT
Parallel connected to front panel INPUT; accepts positive or negative preamplifier pulses. Reference Appendix A, Specifications.

BIPOLAR OUTPUT
Parallel connected to front panel BIPOLAR OUTPUT; provides positive lobe leading bipolar shaped pulses. Reference Appendix A, Specifications.

ICR
Provides a positive true logic signal corresponding to the PUR/LTC incoming count rate.

PUR INHIBIT
Receives a logic pulse from pulsed optical preamplifier. See Appendix A, Specifications.

PREAMP POWER
Provides power for any Canberra preamplifier. Model 1708 Preamp requires a special cable.

PIN	FUNCTION
1	Ground
2	Clean Gnd
4	+12 V dc
6	– 24 V dc
7	+24 V dc
9	– 12 V dc

DT
Provides a negative logic signal to ADC's Live Timer for live time correction. See Appendix A, Specifications.

PUR
Connector for LG and reject signals and common ground. Reference Appendix A, Specifications.

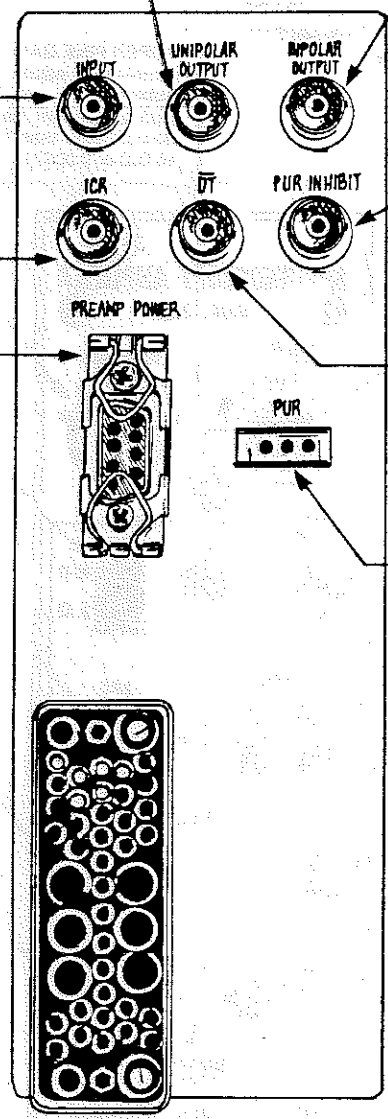


Figure 2.2
Rear Panel Controls

2.3 INTERNAL CONTROLS

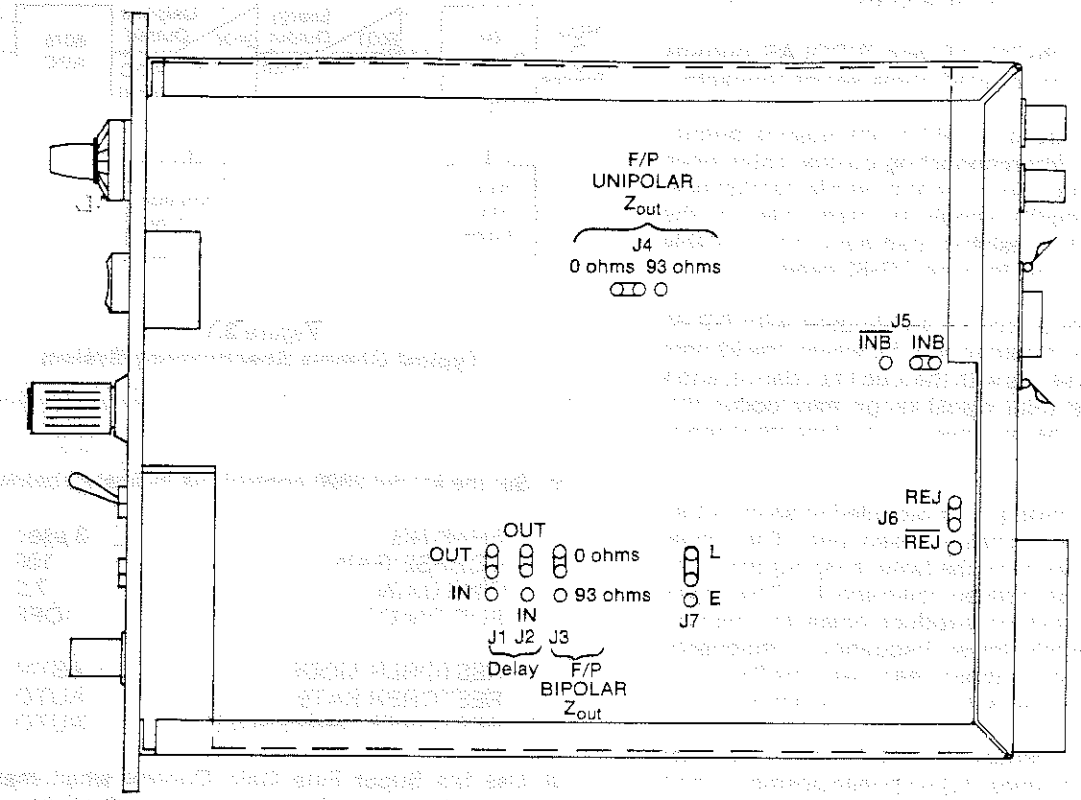


Figure 2.3
Internal Controls, Right Side Cover Removed

Section 3. Amplifier Operation

The purpose of this section is to familiarize the user with the operation of the Model 2020 Amplifier and to check that the unit is functioning correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand.

3.1 INSTALLATION

The Canberra Model 2000 Bin and Power Supply, or other bin and power supply systems conforming to the mechanical and electrical standards set by AEC Report TID-20883 (rev.) will accommodate the Model 2020. The right side cover of the two-width NIM module acts as a guide for insertion of the instrument. The module is secured in place by turning the two front-panel captive screws clockwise until finger tight. It is recommended that the NIM bin power switch be OFF whenever the module is installed or removed.

The Model 2020 can be safely operated where the ambient air temperature is between 0°C and +50°C (+120°F maximum). Perforations in the top and bottom sides permit cooling air to circulate through the module. When rack mounted along with other heat generating equipment, adequate clearance should be provided to allow for sufficient air flow through both the perforated top and bottom covers of the NIM bin.

3.2 SPECTROSCOPY SYSTEM SETUP

Figure 3.1 shows a typical gamma spectroscopy system. Prior to installation, the internal controls should be set to their desired positions. See Figure 2.3 for the locations of the controls.

a. Jumper plugs J1 and J2 change the UNIPOLAR output delay from the factory set OUT (Prompt mode) to the IN (Delayed 2 μsec mode, or 4 μsec with option 2020-4). Jumper plugs J3 and J4 select the front panel BIPOLAR and UNIPOLAR output impedance.

The output impedances can be changed from the factory setting of ≤1 ohm to approximately 93 ohms.

The rear panel UNIPOLAR and BIPOLAR outputs have a fixed impedance of 93 ohms, series connected.

When using the front panel low impedance output, short lengths of interconnecting coaxial cable need not be terminated. To prevent possible oscillations, longer cable lengths should be terminated at the receiving end in a resistive load equal to the cable impedance (93 ohms for type RG-62 cable).

The 93 ohm output may be safely used with RG-62 cable up to a few hundred feet. However, the 93 ohm impedance is in series with the load impedance, and a decrease in the total signal range may occur. For example, a 50% loss will result if the load impedance is 93 ohms.

Another jumper plug (J7) is provided to select a Linear or Exponential restorer response. The Linear response is optimum for the faster shaping-time constants and their associated noise spectra. The slower shaping-time constants produce noise spectra having proportionately lower frequency components, requiring a different restorer response. The Exponential response is better suited to these shapings.

The Model 2020 is shipped with the restorer response jumper plug in the linear (L) response position, which will give the best restorer response for shaping time constants of 0.25 through 4 μs. These are the time constants generally used with Coaxial Ge, proportional counter, surface barrier, and scintillation photomultiplier detectors.

The exponential (E) response will give the best restorer response for the 5 through 12 μs shaping-time constants. This time constant is most often used with Planar Ge and Si(Li) detectors. The exponential response may also be used with the other shaping time constants without loss of resolution performance, provided that the input count-rate remains below 20 kcps.

Additionally, there is a jumper plug to invert the logic sense of the pileup rejector's incoming inhibit (INB) signal (J5) and another for the output reject (REJ) signal (J6). Both are factory set for positive true logic. Either or both may be set for negative true logic by the operator.

b. Insert the Model 2020 into a standard NIM bin. Preamp power is provided by means of a connector located on the rear panel of the Model 2020 amplifier. Allow the total system to warm up and stabilize.

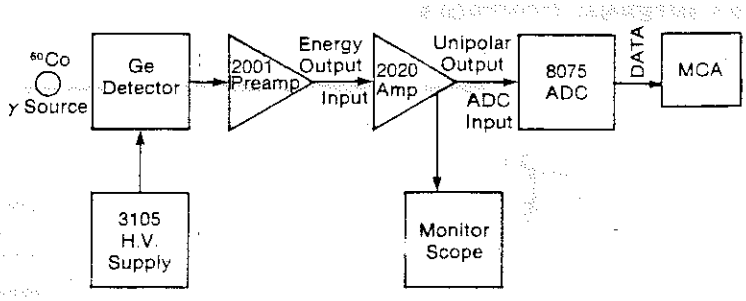


Figure 3.1
Typical Gamma Spectroscopy System

c. Set the Model 2020 controls as indicated below:

SHAPING	3 μsec
COARSE GAIN	100
FINE GAIN	7.2
PUR ON/OFF	OFF
RESTORER MODE	ASYM
RESTORER RATE	AUTO
RESTORER THRESHOLD	AUTO

d. Use the Super Fine Gain Control when matching gains of several detectors or when establishing a specific gain (energy per channel). This control provides 100 times more resolution than the FINE GAIN Control.

e. Set the INPUT POLARITY switch to match the output polarity of the preamp (positive (+) for a Canberra Model 2001 Preamp). This will give approximately a 9 V output when using a preamp gain of 100 mV/MeV and a ^{60}Co radioactive source.

f. Install a "Tee" connector on the Model 2020 UNIPOLAR output. Connect one end to the ADC INPUT on the Analyzer. The ADC must be direct coupled for linear input signals to fully exploit the rate capabilities of the Model 2020. All Canberra ADCs are dc coupled.

g. Connect the other end of the "Tee" connector to an oscilloscope to monitor the UNIPOLAR output.

3.3 SPECTROSCOPY PERFORMANCE ADJUSTMENTS

a. POLE ZERO using a Ge Detector and a ^{60}Co source. The best way to adjust the pole/zero is with the RESTORER MODE set to ASYM, RESTORER RATE set to AUTO, and RESTORER THRESHOLD set to AUTO.

The pole/zero trim is extremely critical for good high count-rate resolution performance. Adjust the radiation source count-rate between 2 kcps and 25 kcps. While observing the UNIPOLAR output on the scope, adjust the pole/zero so that the trailing edge of the unipolar pulse returns to the baseline with no over- or undershoots.

Figure 3.2a shows the correct setting of the P/Z control, with Figures 3.2b and 3.2c showing under- and over-compensation for the preamplifier decay time-constant. Notice some small amplitude signals with long decay times in Figure 3.2a. These are due to charge trapping in the detector and cannot be corrected by the P/Z control.

NOTE

At high count rates, the P/Z adjustment is extremely critical for maintaining good resolution and low peak shift. For a precise and optimum setting of the P/Z, a scope vertical sensitivity of 50 mV/div should be used.

Higher scope sensitivities can also be used, but result in a less precise P/Z adjustment. However, most scopes will overload for a 10 V input signal when the vertical sensitivity is set for 50 mV/cm. Overloading the scope input will distort the signals' recovery to the baseline. Thus the P/Z will be incorrectly adjusted resulting in a loss of resolution at high count rates.

To prevent overloading the scope, a clamping circuit, such as Canberra Model LB1502, Schottky Clamp Box, should be used.

b. Pole/Zero Adjustment Using a Square Wave and Preamp Test Input

1. Driving the preamp test input with a square wave will allow a more precise adjustment of the amplifier Pole/Zero.

2. The amplifier's COARSE GAIN, SHAPING, and INPUT POLARITY controls should be set for the intended application.

3. Adjust the square wave generator for a frequency of approximately 1 kHz.

4. Connect the square wave generator's output to the Preamp's TEST INPUT.

5. Remove all radioactive sources from the vicinity of the detector.

6. Set the scope's Channel 1 vertical sensitivity to 5 V/div, and adjust the main time base to 0.2 ms/div. Monitor the Model 2020's UNIPOLAR output and adjust the square wave generator's amplitude control (attenuator) for output signals for ± 8 V.

   NOTE: Both positive and negative unipolar pulses will be observed at the output.

7. Reduce the scope vertical sensitivity to 50 mV/div.

NOTE

When adjusting the P/Z using the square wave technique, the calibration square wave generated by the oscilloscope can be used. Most scopes generate a 1 kHz square wave used to calibrate the vertical gain and probe compensation. Connect the scope CALIBRATION Output through an attenuator to the preamp test input and repeat Section 3.3.b, steps 1 through 6.

Figure 3.3a shows the correct setting of the P/Z control. Figures 3.3b and 3.3c show under and over compensation for the preamplifier decay time constant. As illustrated in Figure 3.3a, the UNIPOLAR output signal should have a clean return to the baseline with no bumps, overshoots or undershoots.

c. Restorer Mode

The baseline restorer in the Model 2020 is flexible in that both the SYMmetrical and ASYMmetrical modes are offered. In the SYMmetrical mode, the restoration currents are identical for above and below the baseline. For the ASYMmetrical mode the restorer current above the baseline (referenced to a positive output), is much less than that below the baseline.

The ASYMmetrical restorer mode offers superior high count rate performance for high resolution Ge spectroscopy. The SYMmetrical mode is used on Ge systems with low quality preamps, scintillation and proportional counting, and Si systems.

The SYMmetrical mode should always be used for detector systems which exhibit baseline discontinuities resulting from excessive noise and/or high voltage effects, preamp reset pulses and preamp secondary time constants. Secondary preamp fall time constants result in unipolar output undershoots making it difficult to pole/zero the amplifier.

d. Restorer Threshold

Normally, the restorer threshold will be set to AUTO. The Model 2020's restorer circuitry will automatically set the threshold to optimum point, just above the system's noise level. The AUTO setting realizes best performance for most conditions.

The user also has the option of setting the threshold manually by changing the THRESHOLD switch to VARiable. The gain and shaping should be selected with pole/zero properly set prior to VARiable threshold adjustment. To set the threshold properly, the adjustment must be done with the system connected as for normal use but with no radioactive source on or in the vicinity of the detector.

The THRESHOLD DISCriminator has a positive range of 0 V to + 200 mV. The negative threshold is fixed at -500 mV, referred to the UNIPOLAR output. To adjust the DISCriminator, first set it to the 0 V position (fully counterclockwise). The threshold indicator LED should be fully illuminated.

Now increase the threshold by turning the control clockwise until the LED indicator begins to blink. The restorer threshold is now set properly for normal operation. On detector systems which exhibit excessive microphonics, the restorer threshold may have to be raised by an additional amount. For this case, monitor the unipolar output baseline. Set the VAR threshold as low as possible without introducing baseline instability.

e. Restorer Rate

With the restorer rate switch set to AUTO, the restorer is automatically set for optimum performance throughout the usable input count rate range for the shaping selected.

If desired, the restorer rate may be set to HIgh. This increases the restoration current approximately 4 times.

The HIgh restorer rate can be used where a higher than normal restoration rate is required. Improved amplifier performance may be realized at extreme high input counting rates or where more control is required to maintain the baseline, such as with some NaI(Tl) scintillation detector systems. The HIgh restoration rate is normally not used since there will be a loss of resolution due to increased correlated noise inherent in dc restoration.

f. Restorer Response

Faster shaping time constants (0.5 through 4 μs) give rise to output noise spectra having different frequency components than the slower shaping time constant (5 through 12 μs). The Model 2020 provides a restorer response for each of the two conditions: a linear (L) response for the faster time constants and an exponential (E) response for the slower time constants. Jumper plug J7 (see Figure 2.3) selects the required response. Shipped in the linear (L) position. See Section 3.2.a for further information.

g. ADC Controls

To get optimum resolution, the ADC's Lower Level Discriminator (LLD) should be set just above the noise so that the effects of trailing edge pileup are minimized.

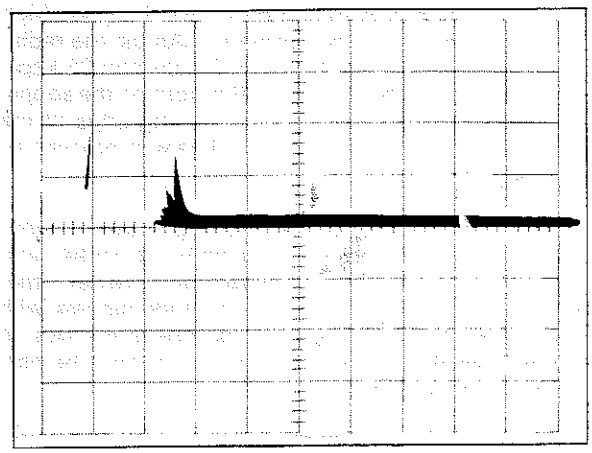


Figure 3.2a
Correct Pole/Zero Compensation

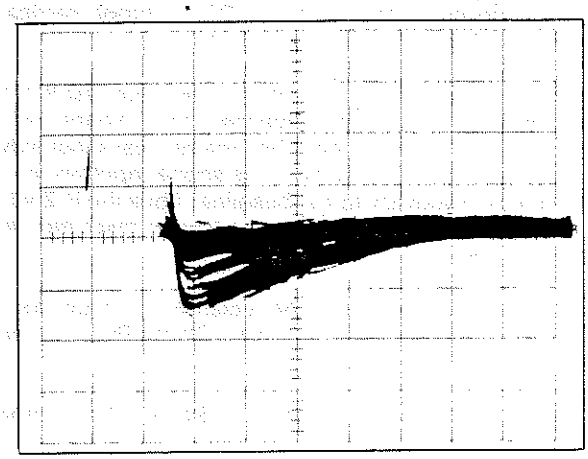


Figure 3.2b
Undercompensated Pole/Zero

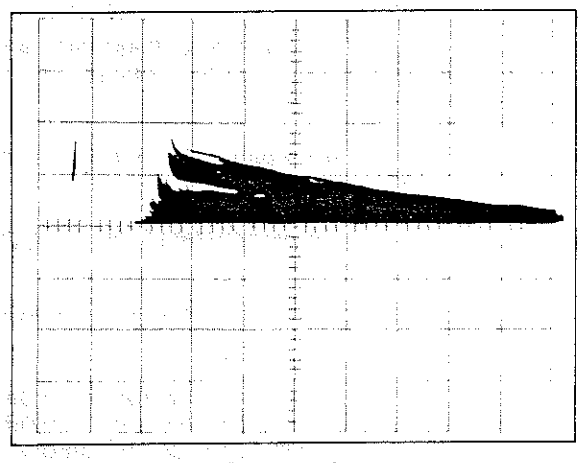


Figure 3.2c
Overcompensated Pole/Zero

Oscilloscope
Vert.: 50 mV/div
Horiz.: 10 μs/div
Source ^{60}Co
1.33 MeV peak: 7 V amplitude
Count Rate: ≈ 2 kcps
Shaping: 3 μs

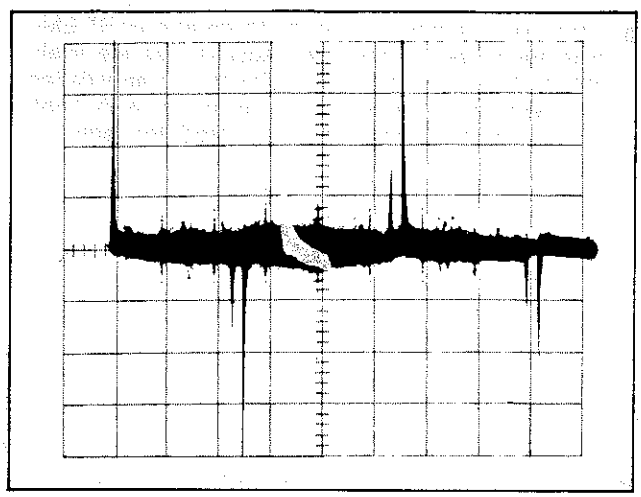


Figure 3.3a
Correct Pole/Zero Compensation

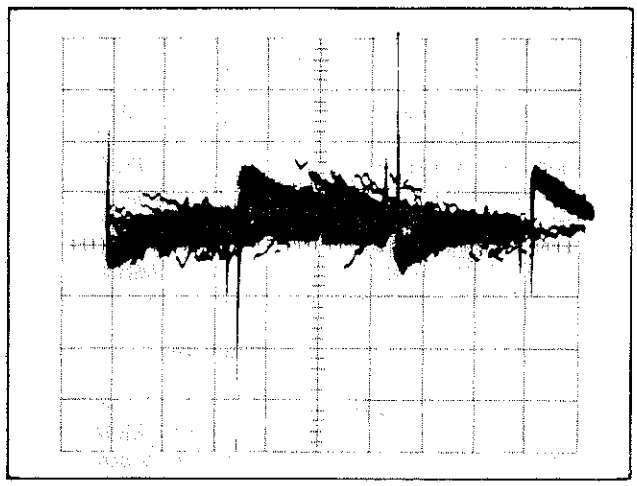


Figure 3.3b
Undercompensated Pole/Zero

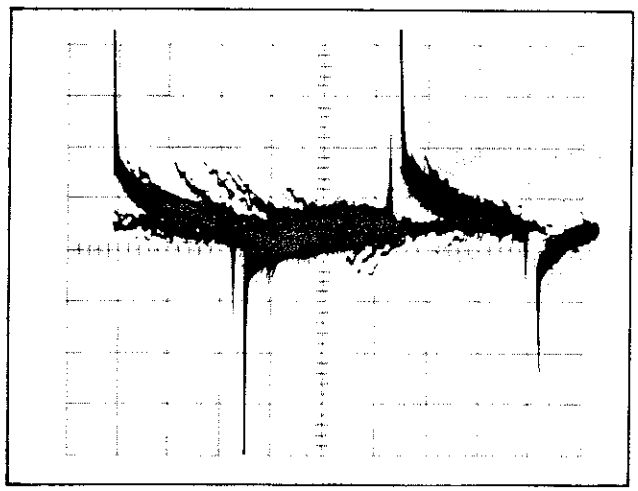


Figure 3.3c
Overcompensated Pole/Zero

Oscilloscope
Vert.: 50 mV/div
Horiz.: 50 μs/div

3.4 RESOLUTION VERSUS COUNT RATE AND SHAPING

The 4 μsec shaping-time constant is optimum for Ge detector systems over a wide range of incoming count rates. For high resolution, longer shaping-time constants offer a better signal-to-noise (S/N) ratio, resulting in better resolution. However, as the count rate increases, the effects of pileup will degrade the resolution much sooner. The optimum shaping-time constant depends on the detector characteristics (such as its size, configuration and collection characteristics), preamplifier and incoming count rate. Below is a list of optimum shaping-time constant ranges for other common detectors.

Scintillation Photomultiplier	0.5
Silicon Charged Particle	0.5 through 2
Cooled Silicon	8 through 12
Gas Proportional Counter	0.5 through 2
Lithium Drifted Germanium [Ge(Li)]	2 through 4
Planar Germanium	4 through 12

3.5 RESOLUTION DESTROYING INTERFERENCE

a. Vibration transmitted to the detector and cryostat. This can be through the floor or mounting, as well as direct audio coupling through the air. Vibration isolators in the mounting and sound absorbing covers around the detector can reduce this problem.

b. The close proximity of a radio station can be picked up by the "dipstick" of the cryostat. Good contact between the dipstick and the cryostat can often help solve this problem. Beware of grounding the cryostat and dipstick as this may increase power line frequency (50 or 60 Hz) ground loops.

c. Ground loops and power line frequency interference can be caused by long cable connections between the detector, preamplifier and shaping amplifier. There is no general solution for this problem. As a first step, the preamp should use the power supplied by the main shaping amplifier. Second, the system should have a single point house ground. For example, on a general system connect the NIM bin to house ground via the ac line cord. Isolate all other equipment requiring ac voltage from the house ground. Connect all the chassis in the system to the grounded NIM bin using heavy braided wire.

d. High voltage power supplies. Generally, an ac line powered HVPS should float from power line ground with the only ground being made at the preamplifier through the high voltage connecting cable.

e. Analyzer EMI (electro-magnetic interference). If the detector is located within 3 to 5 m (10 to 15 feet) of a multichannel analyzer containing a ferrite CORE memory, it can receive EMI. This is due to high memory-core-currents during the memory cycle of the analyzer. The only practical cure for this problem is to operate the analyzer in the "Live" Mode of accumulation. In this way, the memory cycle operates only while no signal is being analyzed.

f. Amplifier parasitic oscillations. If the cable connecting the front panel outputs of the amplifier to the ADC exceeds 3 to 5 m (10 to 15 feet) in length, oscillations can occur. The cure is to use RG-62 cable (93 ohm impedance) and terminate the ADC end of the cable with a 93.1 ohm metal film resistor. Alternatively, the 93 ohm output impedance of the amplifier can be used with no terminator.

g. If trouble is isolated to ground loops and/or RF EMI, detector system loop-buster accessories are available to help minimize these effects. An application note entitled "System Considerations with High Resolution Detectors" is available from the factory.

Section 4. PUR/LTC Operation

The Model 2020 and associated ADC work together as an integral system to perform pileup rejection and live time correction. The associated ADC can be an MCA's internal ADC, or any current Canberra NIM ADC. Older Canberra MCAs and ADCs can be adapted for use with the 2020's PUR/LTC circuits; consult the factory.

During the amplifier and ADC processing time, the Model 2020 Amplifier inspects for pileup, utilizing the ADC's Linear Gate (LG) signal when making the distinction between leading edge and trailing edge pileup. The Model 2020 initiates an ADC reject sequence when pileup is detected during the ADC's Linear Gate time (LG) permitting the ADC to convert only those detector signals resulting from single energy event.

To compensate for dead times associated with rejected pulses and amplifier processing times, the Model 2020 generates a dead time (DT) signal which extends the collection time by the appropriate amount.

The following instructions apply to obtain maximum performance when utilizing the Model 2020 and 8075 ADC and apply to these two instruments. For a complete germanium detector system, refer to the system's instructions.

4.1 PUR/LTC SYSTEM SETUP

a. Connect the Model 2020 and 8075 ADC as shown in Figure 4.1.

b. Set the Model 2020 controls as follows:

COARSE GAIN	300
FINE GAIN	4.4
INPUT POLARITY	POS
SHAPING	4 μsec
PUR ON/OFF	ON
RESTORER RATE	AUTO
RESTORER MODE	ASYM
RESTORER THRESHOLD	AUTO

c. Set the Model 8075 controls as follows:

CONVERSION GAIN	8K
RANGE	Set as required by MCA
OFFSET	Equal to the MCA's memory size

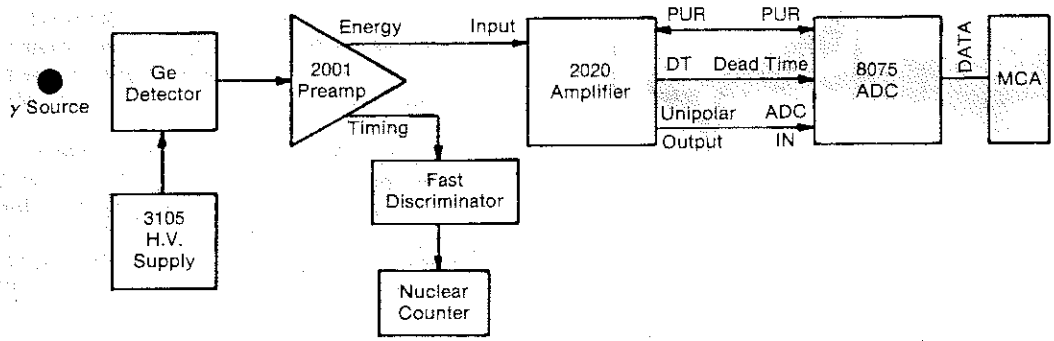


Figure 4.1
Gamma Spectroscopy System With Pileup Rejection and Live Time Correction

4.2 PERFORMANCE ADJUSTMENTS

a. Monitor the UNIPOLAR OUTPUT of the Model 2020 on Channel 1 of the scope; adjust the P/Z, see Section 3.3.a or 3.3.b. The 122 keV ^{57}Co peak will be approximately 1.65 V.

b. IMPORTANT! Remove all excitation sources from the vicinity of the detector.

c. Set the MCA to COLLECT.

d. Set the Model 8075 SCA LLD threshold just above the system noise level.

e. The following step is to optimize the discriminator sensitivity; to insure that the discriminator threshold is at its lowest setting above the noise level:

On the Model 2020, adjust the PUR DISC control fully counterclockwise. The DISC LED indicator will continuously glow and the ADC's % Dead Time indicator will show 100%. Adjust the PUR DISC control clockwise until the DISC LED indicator begins to blink. The DISC Threshold is now properly set.

f. If the VAR restorer threshold is to be used, adjust as indicated in section 3.3.d.

g. The % Dead Time Meter should now be at zero with only occasional deflections when a transient or spurious event is received.

h. IMPORTANT: If the Amplifier GAIN or SHAPING or the Detector or Preamplifier are changed, the Model 2020 PUR DISC control must be rechecked or adjusted. The MCA/ADC LLD must be set just above the system noise level.

4.3 PILEUP REJECTION WITH A LIVE SOURCE

a. Bring a source such as ^{57}Co near the detector. Adjust the ^{57}Co source for an input count rate of approximately 50 kcps.

b. Set the MCA's memory to first half.

c. Set the MCA to Collect. Adjust the Model 2020 gain to allow collection of the primary and sum peaks. If a gain adjustment was necessary, readjust the PUR DISC as described in step 4.2.e.

d. Set the MCA's preset to 60 Live seconds.

e. Disable Collect. Clear Data, then enable Collect. Accumulate a spectrum.

f. Set the MCA's memory to second half.

g. Accumulate a spectrum with the Model 2020 PUR ON/OFF switch OFF. Enable the MCA's OVERLAP function and compare the first half of the memory (PUR ON) to that of the second half (PUR OFF), see Figure 4.2. Note the reduction in amplitude of both the sum peaks and background. Also note the improved resolution of the sum peaks. The background reduction and improved resolution are directly indicative of the Pileup Rejector's capabilities, since only sum peak pulses which are indeed 100% in coincidence should be processed.

4.4 LIVE TIME CORRECTION WITH A LIVE SOURCE

a. Set up the equipment as indicated in step 4.1.

b. Confirm performance adjustments indicated in step 4.2.

c. Set the MCA's preset to 500 Live seconds.

d. Position a radioactive source, such as ^{65}Zn, near the Ge detector and adjust for an incoming count rate of 1 kcps. Once in place, the ^{65}Zn source should not be moved or altered in any way for the remainder of the experiment.

e. Collect a spectrum for 500 Live seconds. Record the ^{65}Zn peak's net AREA.

f. To the 1 kcps of ^{65}Zn, add approximately 5 kcps of ^{137}Cs to make the total incoming rate 6 kcps.

g. Collect a new spectrum for 500 Live seconds, and record the ^{65}Zn peak's net AREA.

h. Repeat steps f and g in 5 kcps increments up to 30 kcps.

i. Compare the ^{65}Zn peak net area in steps f through h to that in step e and compute the percentage change.

j. Set the PUR ON/OFF switch to OFF. Repeat steps c through i.

Since the detector-source (^{65}Zn) geometry was maintained and the preset Live Collection time was held constant, the ^{65}Zn net area can be used as a standard when comparing the effect of background (^{137}Cs) count rate.

NOTE: Each time the background count (^{137}Cs) is changed, allow the detector to stabilize a few minutes before collecting the spectrum.

With the PUR OFF, large changes will be observed in the ^{65}Zn net peak area as a function of count rate. With the pileup rejector set ON, changes in the ^{65}Zn peak net area will be significantly reduced, the Live Time corrector extends the collection time compensating for amplifier processing time and ^{65}Zn events rejected due to pileup.

Performance may vary and is dependent on factors such as ADC type, ADC calibration, spectrum energy distribution and detector characteristics such as geometry, size, and ballistic deficit.

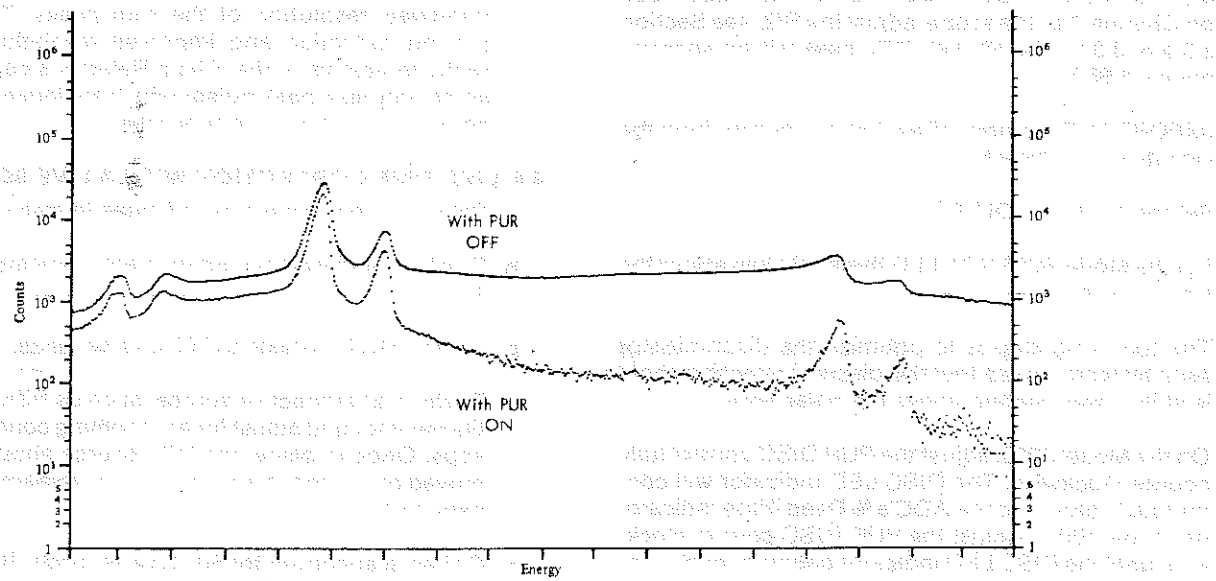


Figure 4.2
^{57}Co at 60 kcps at 4 μs Shaping

Section 5.
Theory of Operation

The following is a description of the circuitry used in the Model 2020 AMP/PUR/LTC. Components are referred to reference designations such as Q2, C5 and R10. Throughout the following circuit description, refer to the circuit block diagram, schematics, and timing sequence.

5.1 BLOCK DIAGRAM DESCRIPTION (Drawing B-21728)

The preamp signal enters the front panel INPUT BNC (J3) or rear panel INPUT (J103), passes through the input buffer, Q19 and Q20, and is differentiated by C5 through C11, R6 and/or R7 as selected by S2b and S4a and pole/zero compensated by R77, R78, R80, or R82, and RV7. The time constants are selected by SHAPING switch S4 and the MULTIPLIER switch, S2. The differentiated signal is amplified by Amp 1, Amp 2 and Amp 3, or by Amp 1 and Amp 3 only, depending on the COARSE GAIN switch (S1) selection. The amplified signal is then integrated by the complex-pole integrators. Between the two integrators the signal is either buffered or inverted by the polarity amplifier, depending on the switch position of S3.

The output of the second integrator drives both the unipolar and bipolar output amplifiers. The unipolar output signal is connected to front and rear panel BNC connectors J2 and J102. The bipolar output signal is connected to front and rear panel BNC connectors J1 and J101. The unipolar output signal also drives the restorer and auto threshold circuitry. The restorer comparator gates the restorer transconductance amplifier and provides a clear signal for the THRESHOLD PUR circuitry. The output of gain amplifier Amp 3 is connected to the PUR/LTC circuitry where the analog signal is shaped and used for pileup rejection and live time correction.

5.2 AMPLIFIER CIRCUIT DESCRIPTION (Drawing B-17873)

5.2.1 Gain Amplifiers

For optimum signal to noise ratio, most of the gain is accomplished before integration. To avoid excessive attenuation between gain stages and maintain low output noise, only amplifiers Amp 1 and Amp 3 are used at low gains. As a result, the input amplifier Amp 1 is always the dominant noise source. Amp 2 is added to the circuit at high gains. This enables each of the three gain stages to operate at relatively low closed-loop gains providing stable operation with time and temperature.

Amplifiers Amp 1 (Q1 through Q6), Amp 2 (Q7 through Q12) and Amp 3 (Q13 through Q18) are all basically the same configuration; therefore, only Amp 1 will be fully described.

5.2.2 Amp 1

The differential input pair Q1 drives the common base transistors Q2 and Q3. Transistors Q2 and Q3 are operated at low current levels, providing a high output impedance to drive output transistors Q5 and Q6, through the common source FET Q4.

C15 provides feedback for closed loop stability and allows the amplifier to follow a 100 nanosecond rise time input signal with very low distortion. Transistors Q5 and Q6 are biased on by D51 and R22 respectively, with the junction of R26 and R28 providing a low impedance output.

The differentiation network and pole/zero cancellation circuitry are both located at the inverting input of Amp 1. SHAPING switch S4 and MULTIPLIER switch S2 select the passive differentiator capacitors C5 through C11, passive differentiator resistors R6 and R7, and pole/zero compensating resistors R77, R78, R80, and R82 for the selected time constant. The pole/zero control (RV7) sets the degree of pole/zero compensation. The dc balance control (RV1) is factory set so that changes of the FINE GAIN control (RV6) will not shift the output dc level of AMP 1 and to minimize the dc offset that appears at the output of Amp 2. D49 is a fast-switching overload protection diode enhancing good overload recovery.

5.2.3 Amp 2 and Amp 3

Amplifier Amp 2 is non-inverting with a gain of 30, determined by R30, R31, R50, and R51. It is switched into the amplification chain by COARSE GAIN switch S1 only for gains above 300. Diode D3 prevents charge accumulation on C27 during overload conditions, enhancing good overload recovery.

Amp 3 is an inverting amplifier with its gain controlled by the ratio of the parallel combination of R56 and R58 and input resistors R52, R53, and R54, selected by the COARSE GAIN switch. Diodes D8 and D9 provide overload protection, enhancing good overload recovery. Capacitor C37 allows the gain stage to be ac coupled with a time constant of C37 and R58. This very long time constant contributes to the effectiveness of the dc restorer.

5.2.4 Integrators

The first integrator comprises A6, R83 through R94, C46, C47, C50, and C51. The second integrator includes A8, R107 through R118, C68, C69, C73, and C74. These are low-pass active filters that provide complex pole pairs which have the locus of the poles equidistant from the abscissa on the S-plane. The real part of the complex poles are equal to the pole of the input differentiator. The active filter networks are selected by SHAPING switch S4 and S2.

Amplifiers A6 and A8 are wide band, high slew rate, integrated circuit operational amplifiers. They are connected in a non-inverting configuration with a dc gain of 1.

5.2.5 Polarity Amplifier

The polarity amplifier is situated between the two integrators and include A7, Q23, Q24, and associated resistors. Amplifier A7 is a wide band, high slew-rate, integrated circuit operational-amplifier. When the INPUT POLARITY switch is set to negative (-), the gates of FETs Q23 and Q24 are driven to approximately -17 V, turning them off. Since pin 3 of A7 is not tied to ground and it is allowed to follow the integrated input signal, the amplifier acts as a voltage follower with unity gain. When the INPUT POLARITY switch is set positive (+), both FETs Q23 and Q24 turn on, shorting pin 3 of A7 to ground. With A7 pin 3 grounded, the amplifier has an inverting gain of 1.

5.2.6 Unipolar Output Amplifier

A4 and a power output driver, Q28 through Q30, constitute the output amplifier. Integrated circuit A4 is a wide-band, high slew-rate operational amplifier. The overall amplifier (op-amp and driver) provides an inverting gain of 3.3 with single-pole integration to minimize noise introduced by amplifier A4. The integration time-constant is derived from R125 and/or R126, depending on the MULTIPLIER switch position, and capacitors C86 through C91 as selected by the SHAPING switch. The output driver transistors are biased Class "AB". Diodes D21, D24, resistor R266, and current source Q28 form the biasing network for the output transistors.

5.2.7 Bipolar Output Amplifier

The bipolar output amplifier is composed of A3, Q25, Q26, and Q27. The negative unipolar signal from the second integrator is differentiated to produce the bipolar signal. The time constants for the differentiator are determined by the selection of R184, R185, and C75 through C80. The bipolar signal is then amplified and inverted by A3, which is a high slew-rate integrated circuit operational-amplifier. The output driver circuit, Q25, Q26, and Q27, is of the same design as the unipolar output driver circuit.

5.2.8 Restorer Gate Threshold Circuits

One of two circuits, AUTO or VAR, may be selected by switch S8 to set the reference threshold for the restorer gate circuitry. The AUTO circuit consists of A9, Q34 through Q36, S5b and S1c. A9, Q34 and Q35 form a closed-loop circuit whose operation resembles an op-amp. The AUTO THRESHOLD circuit monitors the unipolar output noise level. Diode D26 causes this circuit to have a unidirectional response, so that it responds only to negative excursions of the unipolar output noise. With S5b in the SYMmetrical Mode, a positive reference equal to the average value of the unipolar output noise is generated at TP17. In the ASYMmetrical MODE, the threshold is set at approximately twice the voltage of TP16. This voltage is automatically set by the gain switch S1C and is determined by the resistive divider composed of R137 through R140. Q36 shunts the output of A9 when a positive logic INB (inhibit) signal is applied to its base. This defeats the auto threshold when a preamp reset pulse causes a large negative signal at TP7. The VAR THRESHOLD circuit is an adjustable resistive divider made up of R177, R178 and RV9. Enabling this circuit allows the user to manually set the threshold covering a range of approximately +50 to +200 mV.

The restorer gate circuit comprises A10, A11, Q37, and Q38. When a positive signal (greater than the threshold) appears at TP7, the output of comparator A11 goes low, shutting off Q37. C112 ac couples the signal to transistor A5c which gates the restorer circuit off. The ac coupling prevents potential restorer latchup problems. The negative restorer gate A10 operates in the same manner for large negative signals such as preamp reset pulses. The negative threshold is set to approximately -500 mV by resistive divider R174 and R175. Q38 is turned on by large negative signals and brings the positive threshold at TP18 to approximately 0 V. Both comparator signal inputs are protected by the diode clamps D36 and D37.

5.2.9 Restorer

The restorer circuit consists of transistor array A5, Q31 through Q33, Q48, Q51, and Q52. S5a selects the SYMmetrical or ASYMmetrical MODE and S6 selects the AUTO or High RATE. The restorer is a transconductance amplifier which develops a current of the correct polarity as its output (junction of Q32 collector and A5 pin 15). The correction voltage developed on C110 is buffered by FET Q31 and summed in at A4 pin 3, forcing TP7 to 0 V, maintaining the baseline.

Jumper plug J7 selects the Linear or Exponential restorer response. In the L mode, the restorer operates with maximum gain and provides the hard response necessary for faster shaping time constants. When J7 is in the E position, the restorer gain is greatly reduced and provides a softer response necessary for the slower shaping time constants. In the AUTO RATE position, the source and sink currents for holding capacitor C110 are set by R156. As the count rate increases, extra source and sink current is provided by C106 and D30. The HIGH RATE position switches Q48 on, which increases the source and sink current by a factor of four. In the SYMmetrical MODE, the source and sink currents applied to C110 are equal. When S5a is switched to the ASYMmetrical MODE, Q51 turns on and enables Q52 to conduct for positive signals at TP7. This reduces the sink current applied to C110 by a factor of 0.1, which provides a softer restorer response for positive output (only) excursions.

5.3 PUR/LTC CIRCUIT DESCRIPTION (Drawing B-17873)

5.3.1 Signal Discriminator

The amplifier signal from Amp 3 is attenuated, delay line shaped and discriminated from noise by comparator A1 or A2, depending on the position of the INPUT POLARITY switch. When the signal exceeds the variable threshold set by the DISC pot (RV8), the selected comparator generates a positive logic pulse.

Q42, Q43, RV8 and associated resistors form current sources which develop a voltage on the reference pins of A1 and A2. The proper current source is selected by the INPUT POLARITY switch S3c.

The front panel DISC adjustment sets the reference voltage just above the noise threshold. Diode D45 provides temperature compensation for Q42 and Q43. The output of A1 and A2 (TP19) is connected to monostable A12b, which provides the system trigger and drive signal for LED DS1, a user aid in setting the Pileup Rejector discriminator.

5.3.2 Reject/Dead Time Logic

The system trigger pulse simultaneously triggers A16a and flip-flop A18a/A18b. A18 pin 6 is set to a logic high. No change takes place in A16a since its 'D' input was initially at a logic low. However, A16a will toggle if a subsequent system trigger should occur.

A18 pin 6 also drives A17d setting DT (dead time not) to a logic low (true). A17b and A13d buffer the logic high signal from A16a pin 5. If LG enables A14d, REJect is set to a logic high (true). The REJect signal operates on the ADC, initiating a reject sequence. The logic signal at A16a pin 6 is delayed by R234 and C131, inverted by A13c and connected to A16b pin 12. Provided A16a was not cleared, the positive transition of the LG (ADC linear gate signal) clocks A16b pin 8 to a logic low. A17c and A17d are open collector NAND gates connected together forming a NOR function. If A16b was set, its output would contribute addi-

tional time, via A14 and A17, to the DT signal. The LG signal is buffered by A13f and A13e. When the UNIPOLAR OUTPUT signal returns to the baseline, the pulse former (A13a and A14a) generates a negative logic pulse clearing A18a/A18b and A16a. Once those flip-flops are reset, A16b will be clocked reset at the next LG signal. The INB signal (positive true) or INB signal (negative true) can also clear A16a, A16b, and A18a/A18b and will keep DT low via A14 and A17c.

5.4 SEQUENCE OF EVENTS

For the following discussion, refer to the timing diagram. The philosophy of the PUR/LTC design is predicated on the following conditions:

1. The system input must be statistically random.
2. For each block of dead time generated by the PUR/LTC, an uncontaminated pulse must be processed and accepted by the ADC.
3. All contaminated pulses that occur during the processing sequence will be rejected.

The processing sequence begins with the first input from Amp 3 and ends when the UNIPOLAR OUTPUT of an uncontaminated signal returns to the baseline.

To clarify the operation, the sequence of events will be described for 3 cases: (1) No pileup, (2) trailing edge pileup, and (3) leading edge pileup.

5.4.1 CASE 1: No Pileup

For this case there is no pileup: a single pulse from Amp 3 results in just one system trigger in the processing sequence. The sequence is initiated by the system trigger setting flip-flop A18a/A18b and the DT signal to the logic low (true) state. When the UNIPOLAR OUTPUT signal returns to the baseline, A15 pin 10 provides a clear pulse, clearing A18a/A18b and ending the DT signal. Since A16a was never set, A16b is not set and contributes no dead time when clocked by LG.

5.4.2 CASE 2: Trailing Edge Pileup

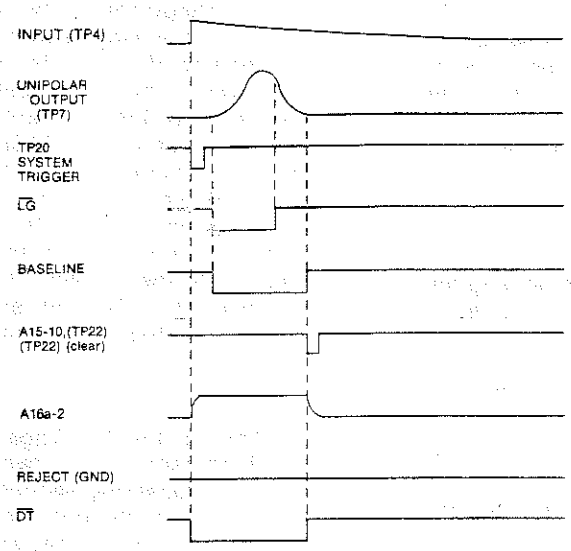
Case 2 is distinguished by two or more pulses from Amp 3 within the processing sequence, with the second pulse beginning after the LG pulse. For this case there are two system triggers, the first one sets flip-flop A18a/A18b while the second sets A16a. A18a/A18b sets DT to a logic low (true) while A16a enables A16b. The LG pulse ended prior to the second system trigger, therefore A16b was clocked prior to A16a being set. Once again, there is no contribution of dead time from A16b. At the conclusion of the processing sequence, when the UNIPOLAR OUTPUT signal returns to the baseline, A15 pin 10 provides a clear pulse, clearing A18a/A18b and A16a. The DT signal is reset to its logic high (false) state. REJect was not set since LG did not enable A14d during the second pulse from Amp 3.

5.4.3 CASE 3: Leading Edge Pileup

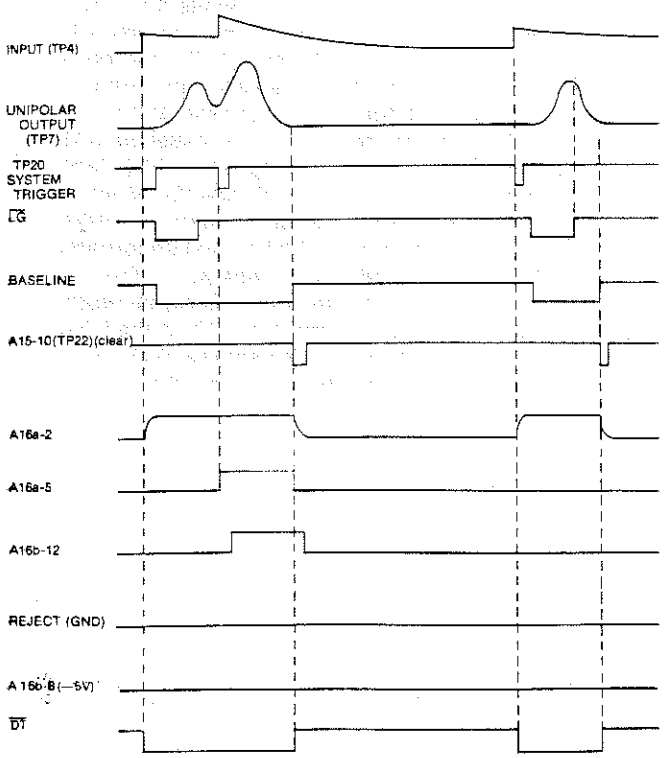
Case 3 is characterized by two or more pulses from Amp 3 within the processing sequence, with the second pulse occuring prior to the positive transition of the LG pulse. Both pulses are convoluted and are rejected. With the LG signal acting as a leading edge pileup detector, the dead time (DT) begins at the first signal from Amp 3 and ends at the conclusion of the next uncontaminated input.

As in Case 2, there are two system triggers. The first one sets flip-flop A18a/A18b while the second sets A16a. A18a/A18b sets DT to a logic low (true) while A16a sets REJect to a logic high (true). Since A16a was set, LG clocks A16b to its set state. A17c and A17d are open collector NAND gates connected in parallel, providing a NOR signal contributing additional dead time. When the UNIPOLAR OUTPUT signal returns to the baseline, A15 pin 10 provides a clear pulse, clearing A18a/A18b and A16a. The REJect signal returns to a logic low (false) when LG goes high. However, the DT signal remains at a logic low (true) since A16b remains set. With the next uncontaminated input, the sequence will take place as outlined in Case 1. Since A16a is now reset, the next LG signal resets A16b and ends its dead time contribution. When the UNIPOLAR OUTPUT signal returns to the baseline, A15 pin 10 will clear A18a/A18b and A16a, ending the dead time (DT) signal. The sequence is now complete.

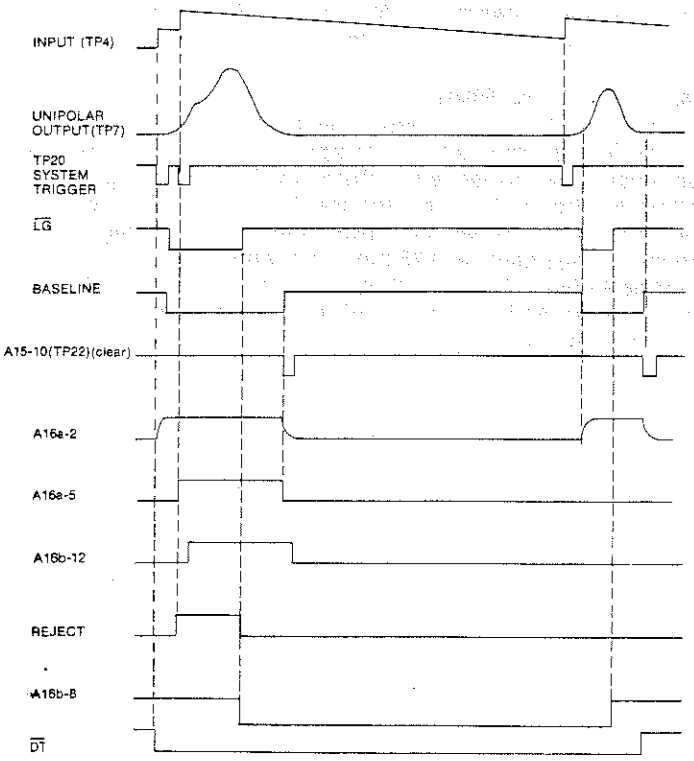
CASE 1 - No Pileup



CASE 2 - Trailing Edge Pileup



CASE 3 - Leading Edge Pileup



Appendix A. Specifications

A.1 INPUTS

INPUT - Accepts positive or negative pulses from an associated preamplifier; amplitude: ±10 V divided by the selected gain, ±12 v maximum; rise time: less than SHAPING time constant; decay time constant: 40 μs to ∞ for 0.25, 0.5, 1, 1.5, 2, 3, and 4 μs shaping time constants, 100 μs to ∞ for 5, 6, 8, 10 and 12 μs shaping time constants; input impedance: ≈ 1 kilohm; front and rear panel BNC connectors.

LG (LINEAR GATE) - Receives a standard TTL logic signal from the ADC. Indicates to the Model 2020 that the ADC has accepted and is processing an event; input is TTL compatible, logic low when ADC accepts input, returning to a logic high at the conclusion of the ADC acquisition cycle; accessible through rear panel PUR Connector.

PUR INHIBIT - Receives a standard TTL logic signal from associated pulsed optical feedback preamplifier used to extend the Model 2020 DT signal, inhibit and reset the pileup rejector during the preamplifier's reset cycle; internal jumper selects the option of either positive true or negative true logic pulses; rear panel BNC connector.

A.2 OUTPUTS

UNIPOLAR OUTPUT - Provides positive, linear actively filtered near-Gaussian shaped pulses; amplitude linear to +10 V, 12 V max.; dc restored; output dc level factory calibrated to 0 ± 5 mV, front panel output impedance less than 1 ohm or ≈ 93 ohms, internally selectable; rear panel output impedance ≈ 93 ohms; short circuit protected; prompt or delayed 2 μs (4 μs with 2020-4 option); front and rear panel BNCs.

BIPOLAR OUTPUT - Provides prompt positive lobe leading linear active filter bipolar shaped pulses; amplitude linear to +10 V, 12 V max., negative lobe is approximately 70% of positive lobe; dc coupled; output dc level ± 25 mV; front panel output impedance <1 ohm or ≈ 93 ohms; internally selectable; rear panel output impedance ≈ 93 ohms; short circuit protected; front and rear panel BNCs.

DT (DEAD TIME) - Provides a negative logic signal and when "OR"ed together with the ADC dead time, at the ADC's live timer, provides live time correction for the amplifier and pileup rejector. Open collector with 1 kilohm pull up resistor through 47 ohm output resistor. Logic low when system is busy, logic high otherwise. BNC connector located on rear panel.

REJECT - Provides a standard TTL logic signal used to initiate an ADC reject sequence for corresponding piled up events; internal jumper selects positive true or negative true logic pulse; 50 ohm output impedence. Accessible through rear panel PUR Connector.

ICR (INCOMING COUNT RATE) - Provides a standard TTL logic signal corresponding to input count rate, positive true, width nominally 150 ns, 50 ohm output impedance; rear panel BNC connector. PUR must be selected.

A.3 FRONT PANEL CONTROLS

COARSE GAIN - 6-position rotary switch selects gain factors of X10, X30, X100, X300, X1000 and X3000.

FINE GAIN - Ten-turn locking dial precision potentiometer selects variable gain factor of X0.3 to X1.3; resetability ≤ 0.03%.

SUPER FINE GAIN - 22-turn screwdriver potentiometer to select gain with an adjustment resolution of better than 1 in 16 000 or 0.0063%.

INPUT POLARITY - 2-position toggle switch to set the Model 2020 for the polarity of the incoming preamplifier signal.

P/Z - 22-turn screwdriver pole zero potentiometer to optimize amplifier baseline recovery and overload performance for the preamplifier fall time constant and the Model 2020's pulse shaping chosen; 40 μs to ∞ for 0.25, 0.5, 1, 1.5, 2, 3 and 4 μs SHAPING time constants, 100 μs to ∞ for 5, 6, 8, 10 and 12 μs SHAPING time constants.

SHAPING TIME - 6-position rotary switch; provides 0.25, 1, 1.5, 4, 5 and 6 μs basic shaping time constants.

MULTIPLIER - Multiplies SHAPING TIME setting by X1 or X2 giving additional shaping time constants of 0.5, 2, 3, 8, 10 and 12 μs, a total of 12 shaping time constants.

RESTORER RATE - 2-position toggle switch to set the baseline restorer rate (slew rate); AUTO: the baseline restorer rate is automatically optimized by internal circuitry as a function of unipolar output signal duty cycle and count rate; High: when selected sets the baseline restorer to a fixed high rate.

RESTORER MODE - 2-position toggle switch to select SYMmetrical or ASYMmetrical baseline restorer modes.

THRESHOLD AUTO/VAR - 2-position toggle switch to set the baseline restorer threshold; AUTO: the baseline restorer threshold is automatically optimized by internal circuitry as a function of the unipolar output signal noise level; VARiable: provides a manual variable baseline threshold adjustment range of 0 V to 200 mV dc. The negative (referenced to the UNIPOLAR OUTPUT) threshold is set at -500 mV dc. An LED indicator is provided as a user-aid for set up convenience.

PUR ON/OFF - 2-position toggle switch to enable (ON) or disable (OFF) the pileup rejector and live time corrector.

PUR DISC - 22-turn screwdriver adjustment potentiometer for optimizing the pileup rejector discriminator threshold level. Provides a variable range of 0 to 550 mV. An LED indicator is provided to aid the user when setting the PUR DISC just above the system noise.

A.4 INTERNAL CONTROLS

UNIPOLAR DELAY - 2 jumper plugs provided to select UNIPOLAR output to prompt (OUT) or delayed 2 μs (IN), or 4 μs on option 2020-4. Shipped in the prompt (OUT) position.

UNIPOLAR Z_{out} - Jumper plug provides $Z_{out} \leq 1$ ohm or $\approx$ 93 ohms for the front panel BIPOLAR output. Shipped in the ≤ 1 ohm position.

BIPOLAR Z_{out} - Jumper plug provides $Z_{out} \leq 1$ ohm or ≈ 93 ohms for the front panel BIPOLAR output. Shipped in the ≤ 1 ohm position.

INB-INB/ - Jumper plug J5 allows the PUR INHIBIT input to accept either positive true or negative true logic signals. Shipped in the INB (positive true) position.

REJ-REJ/ - Jumper plug J6 allows the reject output to be a positive true or negative true logic signal. Shipped in the REJ (positive true) position.

L/E - Jumper plug J7 selects a linear or exponential restorer response. Shipped in the L (linear) position.

A.5 AMP PERFORMANCE

GAIN RANGE - Continuously variable from X3 to X3900.

OPERATING TEMPERATURE RANGE - 0 to 50° C.

GAIN DRIFT - $\leq \pm$ 0.0075%/° C.

DC LEVEL DRIFT - UNIPOLAR output: $\leq \pm 10$ μV/° C; BIPOLAR OUTPUT: $\leq \pm 50$ μV/° C.

INTEGRAL NON-LINEARITY - $\leq \pm$ 0.05%, over total output range for 2 μsec shaping.

CROSSOVER WALK - BIPOLAR output: $\leq \pm 3$ ns for 50:1 dynamic range and 2 μs shaping when used with Canberra Model 2037A Edge/Crossover Timing Single Channel Analyzer.

OVERLOAD RECOVERY - UNIPOLAR (BIPOLAR) output recovery to within $\pm$ 2% (1%) of full scale output from X1000 overload in 2.5 (2.0) non-overloaded pulse widths, at full gain, any shaping time constant and pole-zero cancellation properly set.

NOISE CONTRIBUTION - ≤ 3.2 μV true rms UNIPOLAR (7.1 μV BIPOLAR) output referred to input, 3 μs shaping and amplifier gain ≥ 100.

PULSE SHAPING - Near-Gaussian shape; one differentiator (two for bipolar), two active filter integrators; UNIPOLAR time to peak: 2.35X shaping time; pulse width: 7.3X shaping time; BIPOLAR time to crossover: 2.8X shaping time, time to peak, pulse width and crossover times measured at 0.1% of full scale output.

RESTORER - Active gated.

*SPECTRUM BROADENING - The FWHM of a ^{60}Co 133 MeV gamma peak for an incoming rate of 2 kcps to 100 kcps and a 9 V pulse height will typically change less than 14% for 2 μs shaping, AUTO Restorer Rate, AUTO Restorer Threshold and ASYM Restorer Mode.

COUNT RATE STABILITY - The peak position of a ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 100 kcps and 9 V pulse height will typically shift less than 0.024% for 2 μs shaping, AUTO Restorer Rate, AUTO Restorer Threshold and ASYM Restorer Mode.

*Note: These results may not be reproducible if associated detector exhibits an inordinate amount of long rise time signals.

A.6 PUR/LTC PERFORMANCE

PULSE PAIR RESOLUTION - $\leq$ 500 ns.

MINIMUM DETECTABLE SIGNAL - Limited by detector/preamp noise characteristics.

ADC INTERFACE - Compatible Canberra ADCs are available and can be ordered using the following designations:

Model 8075
Model 8076
Model 8077
Series 35 PLUS MCA

A.7 CONNECTORS

With the exception of the PUR and PREAMP POWER connectors, all signal connectors are BNC type.

PUR - Molex plug 03-06-1031.

PREAMP POWER - Rear panel, Amphenol, type 17-10070.

ACCESSORIES - C1514 PUR/LTC and DT cables.

A.8 POWER REQUIREMENTS

+24 V dc — 130 mA +12 V dc — 150 mA
-24 V dc — 165 mA -12 V dc — 80 mA

A.9 PHYSICAL

SIZE - Standard double-width NIM module 6.86 $\times$ 22.12 cm (2.70 $\times$ 8.71 inches) per TID-20893 (rev.)
NET WEIGHT - 1.3 kg (2.9 lbs.)
SHIPPING WEIGHT - 2.3 kg (5.0 lbs.)

Model 2020
Spectroscopy Amplifier

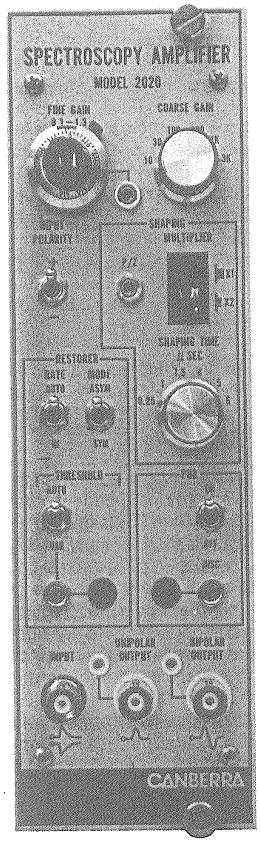
Features

- Pile up rejection/Live time correction
- 12 selectable shaping time constants
- Super Fine Gain Control
- Unique active baseline restorer with:
  1. Automatic or fixed restorer rates
  2. Automatic or manual threshold
  3. Selectable symmetry
- Noise ≤ 3.4 μV
- DC drift ≤ ±10 μV/°C

Description

The Canberra Model 2020 Spectroscopy Amplifier offers the modern spectroscopist more performance, features and flexibility than any other nuclear pulse amplifier available today. Functionally, the Model 2020 provides in a double width NIM module an exceptional spectroscopy amplifier, a gated active baseline restorer, a pulse pileup rejector and a live time corrector.

Canberra's near-Gaussian filter shaping, well known and now emulated by others in the industry, has been refined in the Model 2020 for improved pulse symmetry, minimum sensitivity of output amplitude to variations in detector rise time, and maximum signal to noise ratio. For a given shaping time constant, the improved pulse symmetry minimizes the pulse dwell time by tucking in the trailing skirt of the unipolar pulse shape. This allows a faster return to the baseline. The result is superior energy resolution, count rate, and throughput performance. Unipolar shaping is achieved with one differentiator and two active filter integrators. The differentiator is placed early in the amplifier to insure good overload recovery. The integrators are placed late to minimize noise contribution from the gain stages. The amplifier offers 12 front panel switch selectable pulse SHAPING time constants of 0.25, 0.5, 1, 1.5, 2, 3, 4, 5, 6, 8, 10 and 12 μs.



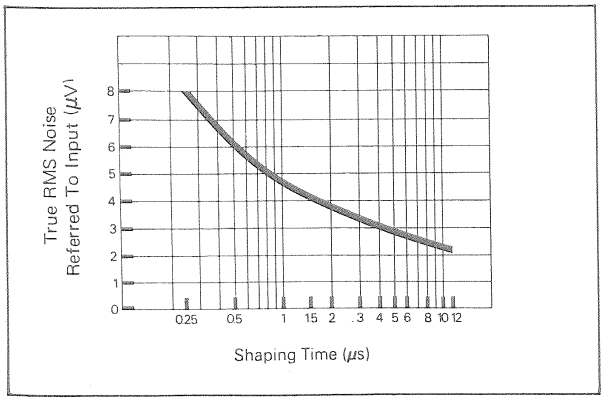


Figure 1.
Typical Model 2020 Unipolar Output True rms Noise (referred to input for gain of 100) vs. Shaping Time constant.

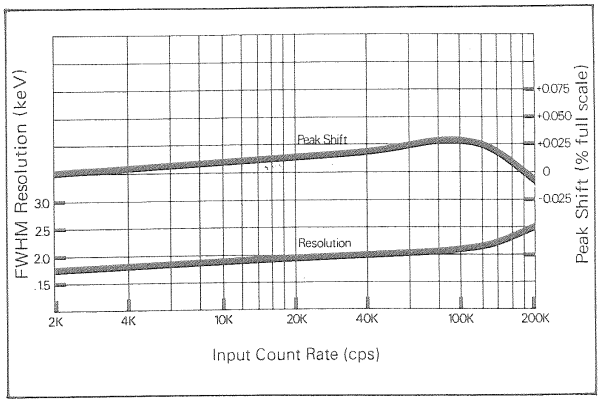


Figure 2.
Typical Model 2020 Resolution and Peak Shift Stability vs. Counting Rate for 2 μs shaping, AUTO Restorer Rate, AUTO Restorer Threshold, ASYM Restorer Mode and a 1.33 MeV ^{60}Co Gamma Peak.

The gated dc restorer offers automatic features on both the restorer threshold and restorer rate, assuring the best possible low and high count rate performance. Amplifier performance is very much dependent on the restorer rate and threshold settings, so the 2020 includes circuitry which continuously samples the amplifier output noise and count rate, and automatically sets the respective restorer threshold and rate with precision for optimum performance. The restorer is also flexible: the discriminating researcher can overide the automatic restorer features. Setting the RESTORER RATE and THRESHOLD switches to their manual positions High and VARiable respectively, allows manual optimization. A front panel LED is provided as a user aid when setting the restorer threshold manually.

The flexibility of the restorer is further enhanced by providing SYMmetrical or ASYMmetrical restorer modes. The symmetrical restorer mode is used for detector systems which exhibit baseline discontinuities resulting from excessive noise and/or high voltage effects, preamp reset pulses and preamp secondary time constants. The asymmetrical restorer mode virtually eliminates charge accumulation and correlated noise on the restorer holding capacitor. This restorer mode is especially suited for use with high resolution detector systems that exhibit minimal baseline discontinuities and whose signals have a clean monotonic return to the baseline. The result is superior resolution/count rate performance when compared to more conventional methods.

Simultaneous UNIPOLAR and BIPOLAR outputs are available at both front and rear panel BNC connectors. The unipolar signal can be delayed 2 μs, or with the 2020-4 option by 4 μs. The bipolar output can be used for counting, timing, or gating.

The internal live time corrector and pileup rejector allows quantitative gamma spectrum analysis nearly independent of system count rate. By connecting the ADC's Linear Gate (LG) signal to the Model 2020 and connecting the Model 2020's REJECT and Dead Time (DT) signals to the ADC and live timer, the Model 2020 and associated ADC together perform pileup rejection and live time correction. During the amplifier and ADC processing time, the Model 2020 inspects for pileup and permits the ADC to convert only those detector signals resulting from a single energy event. To compensate for rejected pulses and amplifier and ADC dead times, a system dead is generated by the live time correction function. The system dead time is the composite dead time of the ADC and Model 2020, extending the collection time by the appropriate amount. A front panel LED is provided as a user aid when setting the PUR DISCriminator.

The Model 2020's exceptional dc stability and ultra low noise ensure that optimum performance is realized. Together with its broad gain range (X3 to X3900), 12 shaping time constants, pileup rejection and live time correction, the Model 2020 offers uncompromising performance when used with Germanium, Silicon, Scintillation, Gas Proportional and Surface Barrier detectors.

Specifications

INPUTS

INPUT - Accepts positive or negative pulses from an associated preamplifier; amplitude: $\pm$10 V divided by the selected gain, $\pm$12 v maximum; rise time: less than SHAPING time constant; decay time constant: 40 μs to ∞ for 0.25, 0.5, 1, 1.5, 2, 3, and 4 μs shaping time constants, 100 μs to ∞ for 5, 6, 8, 10 and 12 μs shaping time constants; input impedance: $\approx$ 1 kilohm; front and rear panel BNC connectors.

LG (LINEAR GATE) - Receives a standard TTL logic signal from the ADC. Indicates to the Model 2020 that the ADC has accepted and is processing an event; input is TTL compatible, logic low when ADC accepts input, returning to a logic high at the conclusion of the ADC acquisition cycle; accessible through rear panel PUR Connector.

PUR INHIBIT - Receives a standard TTL logic signal from associated pulsed optical feedback preamplifier used to extend the Model 2020 DT signal, inhibit and reset the pileup rejector during the preamplifier's reset cycle; internal jumper selects the option of either positive true or negative true logic pulses; rear panel BNC connector.

OUTPUTS

UNIPOLAR OUTPUT - Provides positive, linear actively filtered near-Gaussian shaped pulses; amplitude linear to +10 V, 12 V max.; dc restored; output dc level factory calibrated to 0 $\pm$ 5 mV, front panel output impedance less than 1 ohm or $\approx$ 93 ohms, internally selectable; rear panel output impedance $\approx$ 93 ohms; short circuit protected; prompt or delayed 2 μs (4 μs with 2020-4 option); front and rear panel BNCs.

BIPOLAR OUTPUT - Provides prompt positive lobe leading linear active filter bipolar shaped pulses; amplitude linear to +10 V, 12 V max., negative lobe is approximately 70% of positive lobe; dc coupled; output dc level $\pm$ 25 mV; front panel output impedance $<$1 ohm or $\approx$ 93 ohms; internally selectable; rear panel output impedance $\approx$ 93 ohms; short circuit protected; front and rear panel BNCs.

DT (DEAD TIME) - Provides a negative logic signal and when "OR"ed together with the ADC dead time, at the ADC's live timer, provides live time correction for the amplifier and pileup rejector. Open collector with 1 kilohm pull up resistor through 47 ohm output resistor. Logic low when system is busy, logic high otherwise. BNC connector located on rear panel.

REJECT - Provides a standard TTL logic signal used to initiate an ADC reject sequence for corresponding piled up events; internal jumper selects positive true or negative true logic pulse; 50 ohm output impedence. Accessible through rear panel PUR Connector.

ICR (INCOMING COUNT RATE) - Provides a standard TTL logic signal corresponding to input count rate, positive true, width nominally 150 ns, 50 ohm output impedance; rear panel BNC connector. PUR must be selected.

FRONT PANEL CONTROLS

COARSE GAIN - 6-position rotary switch selects gain factors of X10, X30, X100, X300, X1000 and X3000.

FINE GAIN - Ten-turn locking dial precision potentiometer selects variable gain factor of X0.3 to X1.3; resetability $\leq$ 0.03%.

SUPER FINE GAIN - 22-turn screwdriver potentiometer to select gain with an adjustment resolution of better than 1 in 16 000 or 0.0063%.

INPUT POLARITY - 2-position toggle switch to set the Model 2020 for the polarity of the incoming preamplifier signal.

P/Z - 22-turn screwdriver pole zero potentiometer to optimize amplifier baseline recovery and overload performance for the preamplifier fall time constant and the Model 2020's pulse shaping chosen; 40 μs to ∞ for 0.25, 0.5, 1, 1.5, 2, 3 and 4 μs SHAPING time constants, 100 μs to ∞ for 5, 6, 8, 10 and 12 μs SHAPING time constants.

SHAPING TIME - 6-position rotary switch; provides 0.25, 1, 1.5, 4, 5 and 6 μs basic shaping time constants.

MULTIPLIER - Multiplies SHAPING TIME setting by X1 or X2 giving additional shaping time constants of 0.5, 2, 3, 8, 10 and 12 μs, a total of 12 shaping time constants.

RESTORER RATE - 2-position toggle switch to set the baseline restorer rate (slew rate); AUTO: the baseline restorer rate is automatically optimized by internal circuitry as a function of unipolar output signal duty cycle and count rate; High: when selected sets the baseline restorer to a fixed high rate.

RESTORER MODE - 2-position toggle switch to select SYMmetrical or ASYMmetrical baseline restorer modes.

THRESHOLD AUTO/VAR - 2-position toggle switch to set the baseline restorer threshold; AUTO: the baseline restorer threshold is automatically optimized by internal circuitry as a function of the unipolar output signal noise level; VARiable: provides a manual variable baseline threshold adjustment range of 0 V to 200 mV dc. The negative (referenced to the UNIPOLAR OUTPUT) threshold is set at -500 mV dc. An LED indicator is provided as a user-aid for set up convenience.

PUR ON/OFF - 2-position toggle switch to enable (ON) or disable (OFF) the pileup rejector and live time corrector.

PUR DISC - 22-turn screwdriver adjustment potentiometer for optimizing the pileup rejector discriminator threshold level. Provides a variable range of 0 to 550 mV. An LED indicator is provided to aid the user when setting the PUR DISC just above the system noise.

INTERNAL CONTROLS

UNIPOLAR DELAY - 2 jumper plugs provided to select UNIPOLAR output to prompt (OUT) or delayed 2 μs (IN), or 4 μs on option 2020-4. Shipped in the prompt (OUT) position.

UNIPOLAR Z_{out} - Jumper plug provides $Z_{out} \leq 1$ ohm or ≈ 93 ohms for the front panel BIPOLAR output. Shipped in the ≤ 1 ohm position.

BIPOLAR Z_{out} - Jumper plug provides $Z_{out} \leq 1$ ohm or ≈ 93 ohms for the front panel BIPOLAR output. Shipped in the ≤ 1 ohm position.

INB-INB/ - Jumper plug J5 allows the PUR INHIBIT input to accept either positive true or negative true logic signals. Shipped in the INB (positive true) position.

REJ-REJ/ - Jumper plug J6 allows the reject output to be a positive true or negative true logic signal. Shipped in the REJ (positive true) position.

L/E - Jumper plug J7 selects a linear or exponential restorer response. Shipped in the L (linear) position.

PERFORMANCE

Amplifier

GAIN RANGE - Continuously variable from X3 to X3900.

OPERATING TEMPERATURE RANGE - 0 to 50°C.

GAIN DRIFT - $\leq \pm 0.0075\%/°C$.

DC LEVEL DRIFT - UNIPOLAR output: $\leq \pm 10$ $\mu V/°C$; BIPOLAR OUTPUT: $\leq \pm 50$ $\mu V/°C$.

INTEGRAL NON-LINEARITY - $\leq \pm 0.05\%$, over total output range for 2 μsec shaping.

CROSSOVER WALK - BIPOLAR output: $\leq \pm 3$ ns for 50:1 dynamic range and 2 μs shaping when used with Canberra Model 2037A Edge/Crossover Timing Single Channel Analyzer.

OVERLOAD RECOVERY - UNIPOLAR (BIPOLAR) output recovery to within $\pm$ 2% (1%) of full scale output from X1000 overload in 2.5 (2.0) non-overloaded pulse widths, at full gain, any shaping time constant and pole-zero cancellation properly set.

NOISE CONTRIBUTION - ≤ 3.2 μV true rms UNIPOLAR (7.1 μV BIPOLAR) output referred to input, 3 μs shaping and amplifier gain ≥ 100.

PULSE SHAPING - Near-Gaussian shape; one differentiator (two for bipolar), two active filter integrators; UNIPOLAR time to peak: 2.35X shaping time; pulse width: 7.3X shaping time; BIPOLAR time to crossover: 2.8X shaping time, time to peak, pulse width and crossover times measured at 0.1% of full scale output.

RESTORER - Active gated.

*SPECTRUM BROADENING - The FWHM of a ^{60}Co 133 MeV gamma peak for an incoming rate of 2 kcps to 100 kcps and a 9 V pulse height will typically change less than 14% for 2 μs shaping, AUTO Restorer Rate, AUTO Restorer Threshold and ASYM Restorer Mode.

COUNT RATE STABILITY - The peak position of a ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 100 kcps and 9 V pulse height will typically shift less than 0.024% for 2 μs shaping, AUTO Restorer Rate, AUTO Restorer Threshold and ASYM Restorer Mode.

*Note: These results may not be reproducible if associated detector exhibits an inordinate amount of long rise time signals.

Pileup Rejector/Live Time Corrector

PULSE PAIR RESOLUTION - ≤ 500 ns.

MINIMUM DETECTABLE SIGNAL - Limited by detector/preamp noise characteristics.

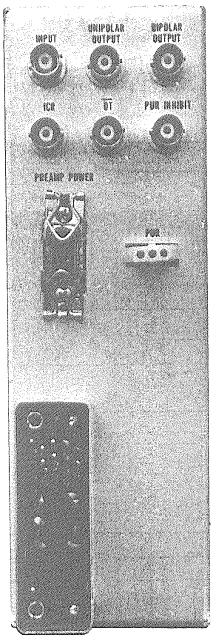
ADC INTERFACE - Compatible Canberra ADCs are available and can be ordered using the following designations:

Model 8075
Model 8076
Model 8077
Series 35 PLUS MCA

For use with older Canberra systems, detailed instructions are provided in the 2020 manual to allow the user to adapt his ADC to interface with the Model 2020 for pileup rejection and live time correction.

CONNECTORS

With the exception of the PUR and PREAMP POWER connectors, all signal connectors are BNC type.



PUR - Molex plug 03-06-1031.

PREAMP POWER - Rear panel, Amphenol, type 17-10070.

ACCESSORIES - C1514 PUR/LTC and DT cables.

POWER REQUIREMENTS

+24 V dc — 130 mA	+12 V dc — 150 mA
-24 V dc — 165 mA	-12 V dc — 80 mA

PHYSICAL

SIZE - Standard double-width NIM module 6.86 X 22.12 cm (2.70 X 8.71 inches) per TID-20893 (rev.)

NET WEIGHT - 1.3 kg (2.9 lbs.)

SHIPPING WEIGHT - 2.3 kg (5.0 lbs.)

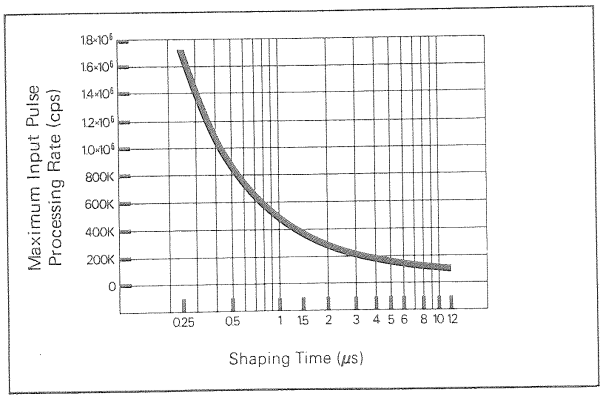


Figure 3.
Typical Model 2020 Maximum Input Pulse Processing Rate versus shaping time constant.

*Maximum Input Pulse Processing Rate: Maximum amplifier input count rate (pulses per second) for which the amplifier's dc restorer maintains the baseline at ground reference.

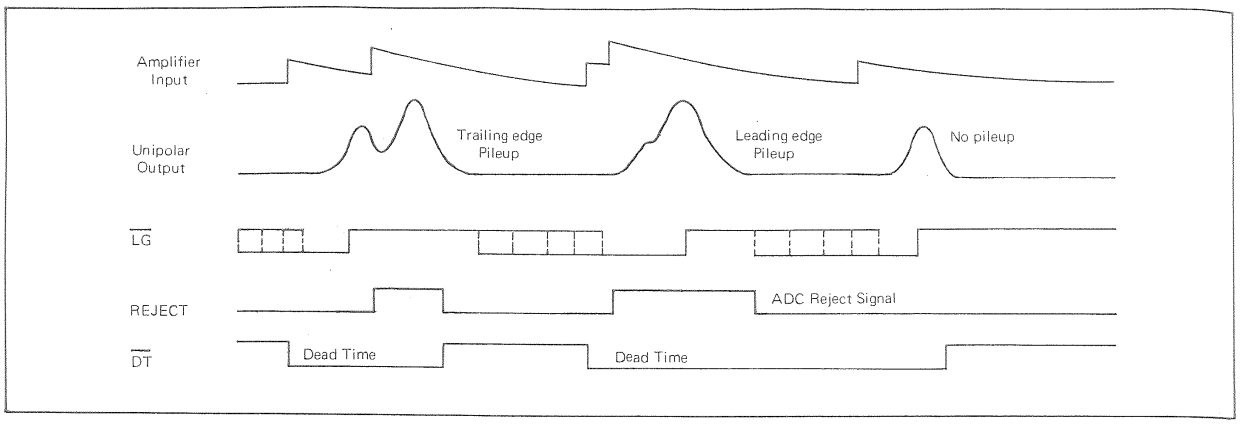


Figure 4.
Relationship of Amplifier and Pileup Rejector Signals.

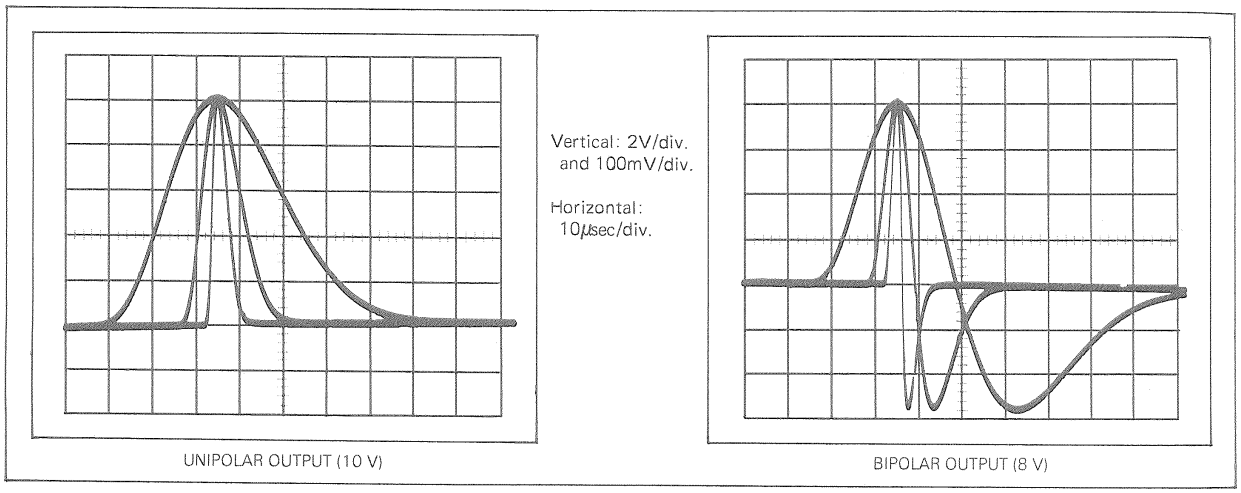


Figure 5.
Model 2020 SHAPING selected for 12, 4 and 1.5 μs.

During the amplifier and ADC processing time, the Model 2020 inspects for pileup and permits the ADC to convert only those detector signals resulting from a single energy event, see Figure 6.

Note the reduction in amplitude of both sum peaks and background. Also note the improved resolution of the sum peaks. The background reduction and improved resolution are directly indicative of the Pileup Rejector's capabilities, since only sum peak pulses which are indeed 100% in coincidence should be processed.

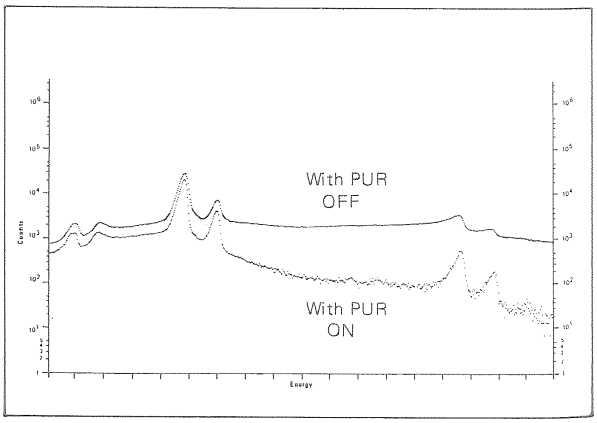


Figure 6.
^{57}Co spectrum at 80 kcps and 4 μs shaping.

Detector: Canberra Model GC2020
MCA: Canberra Model 9102
Amplifier: Canberra Model 2020
Spectrum: ^{57}Co at 60 kcps

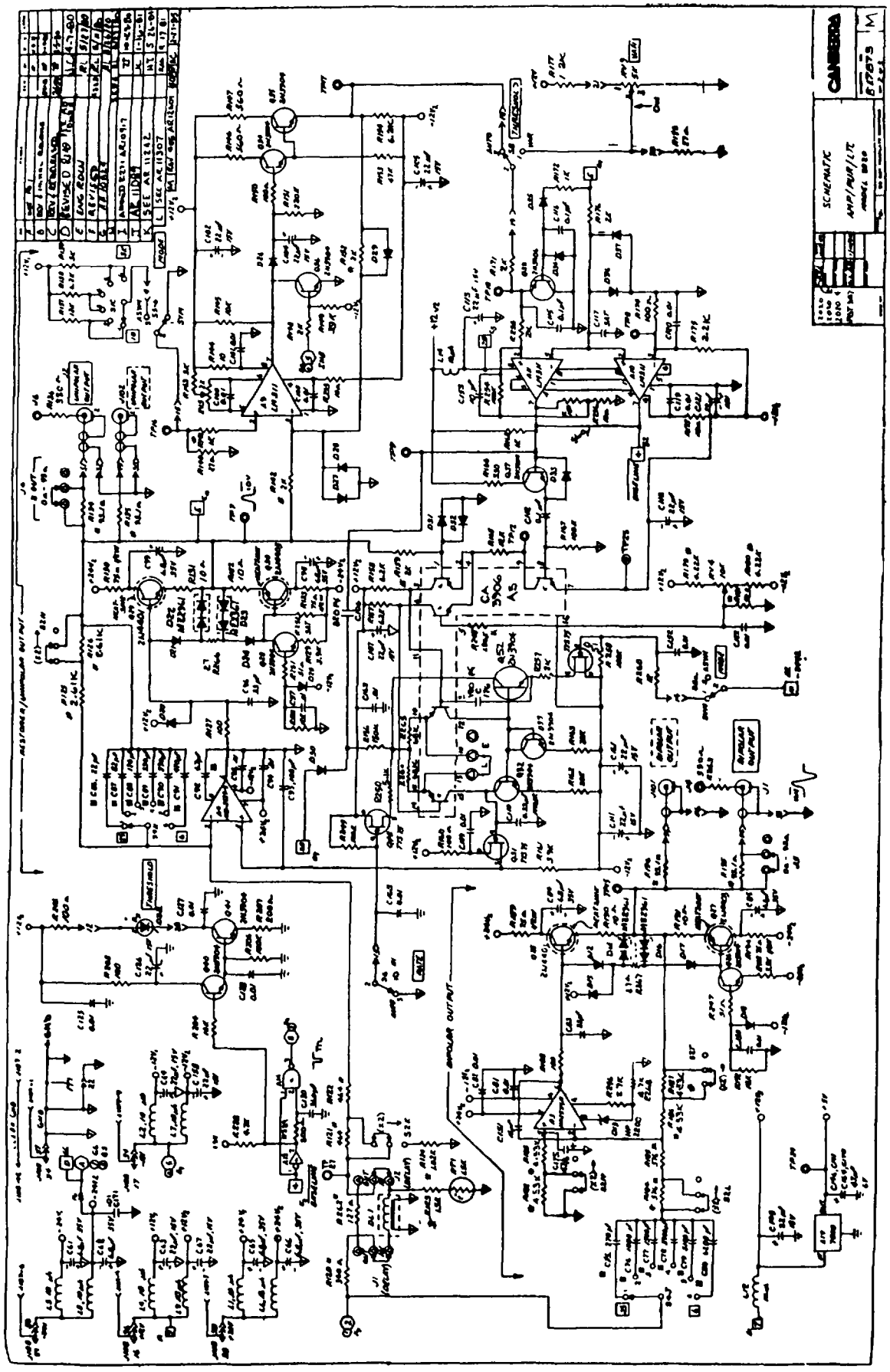


Fig. 6.23a: Spectroscopy amplifier circuit diagram

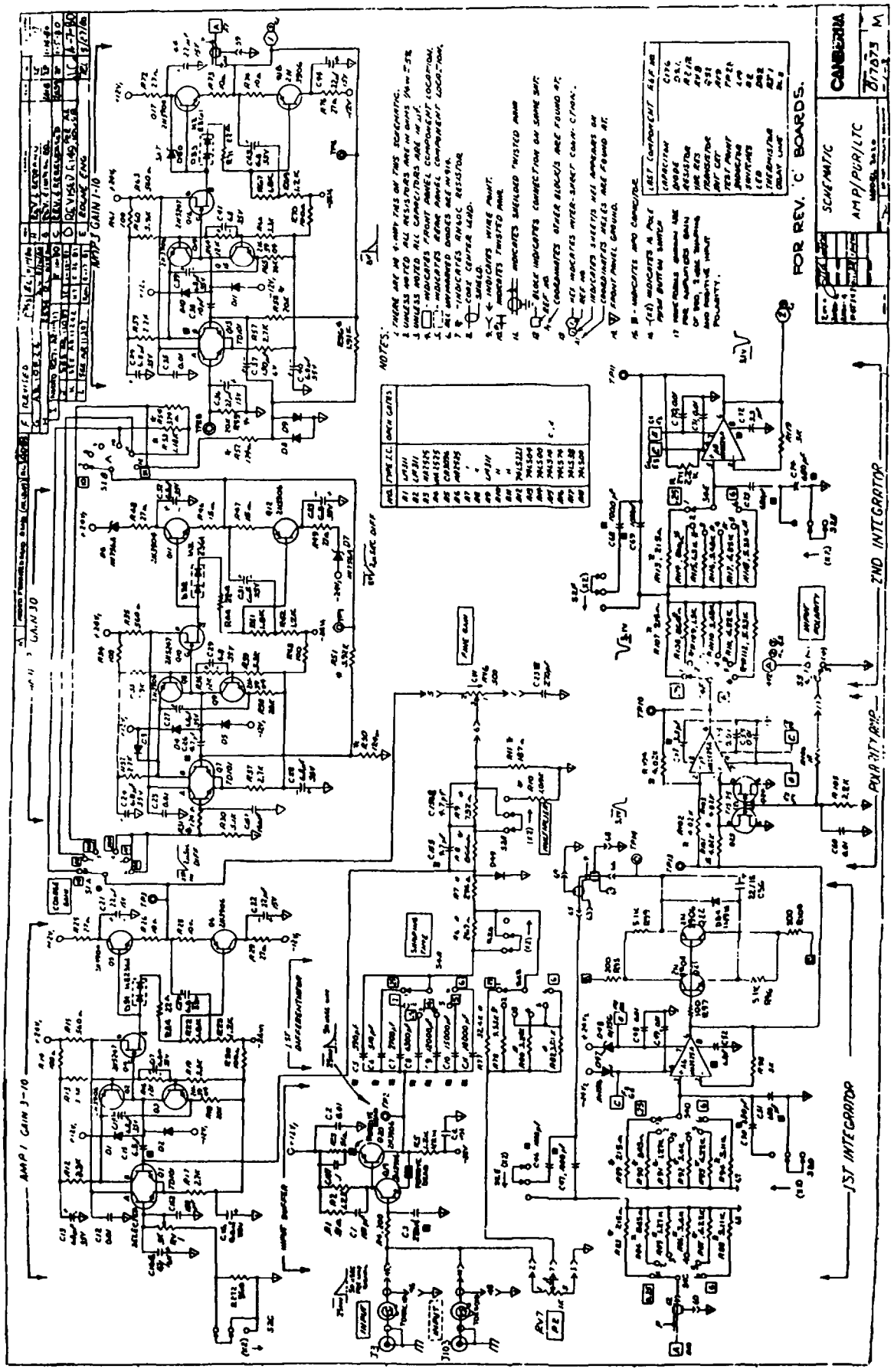


Fig. 6.23b: Spectroscopy amplifier circuit diagram