Model 1520
Integrated ADC-Mixer/Router

User's Manual

0290A

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Canberra Industries, Inc., 800 Research Parkway, Meriden, CT 06450
Tel: (203) 238-2351 Telex: 643251 FAX: 203-235-1347

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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

Printed in the United States of America.

Addendum to the 1520 Manual

If you are using the optional Model C1545A Shielded ADC-MCA Interface Ribbon Cable with the Model 1520 Integrated ADC-Mixer/Router, you must attach the "pigtail" leads at each end of the cable to a nearby grounding screw for reliable system operation.

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1. INTRODUCTION

The Canberra Model 1520 Integrated ADC-Mixer/Router offers Multichannel Analyzer users a research-grade 100 MHz ADC and 16-Input Mixer/Router in a low profile, self-contained instrument. The 1520 is compatible with Canberra System 100 and conventional type MCAs. When used with the System 100, the 1520 provides independent start, stop and presets for each input or groups of inputs.

The Model 1520 features a high quality, high resolution 13-bit (8192 channel) Wilkinson type analog-to-digital converter and a 16-input, acquisition mode selectable Mixer/Router. All components are integrated into a compact, low noise, EMI/RFI-resistant chassis that is less than five centimeters (two inches) tall. The 1520 is suitable for bench mount, rack mount or integration with personal computer (PC) based MCAs. The shielded design allows the 1520 to be placed between a PC chassis and CRT monitor in personal computer based MCA systems without degradation of performance.

The 1520 may be used to satisfy a variety of multiple-input applications such as alpha spectroscopy, beta spectroscopy and low to medium count rate gamma spectroscopy with NaI(Tl) or HPGe detectors. When used with the Canberra Model 7404 Quad Alpha Spectrometer or Model 7401 Single Alpha Chamber, the 1520 provides users with a cost effective solution for alpha spectroscopy applications.

ADC
The ADC is a Wilkinson-type counter/ramp converter with a 100 MHz clock rate, providing high throughput rate with exceptional linearity and accuracy.

A direct-coupled input of 0 to 10 volts, provided by the internal Mixer/Router or by an external amplifier, is digitized according to the front panel GAIN control and acquisition mode selection, into binary code of 8 through 13 bits (256 through 8192 channels).

A choice of Pulse Height Analysis (PHA) or Sampled Voltage Analysis (SVA) is offered. Conversion in PHA mode is initiated automatically using an internal peak detect. The falling edge of the pulse applied to the ADC GATE input initiates the SVA conversions.

Conversions may be universally enabled or disabled by a rear panel BNC connector for Coincidence/Anticoincidence gating and acceptance criteria programmed by the Lower Level (LLD) and Upper Level (ULD) Discriminators.

All inputs share the same Digital Offset and ADC Range. By adjusting these parameters, a corresponding portion of all spectra may be expanded to provide high resolution with limited memory.

The ADC is compatible with the Canberra System 100 and conventional stand-alone MCAs using the external ADC interface option designated for each unit. The TTL-compatible interface logic may be set for positive true (logic high) or negative true (logic low), ensuring compatibility with many other MCA and Memory systems.

A ten-segment front panel LED indicator displays the ADC's average dead time.

Mixer/Router
The Mixer/Router may be used to route 1, 2, 4, 8 or 16 analog output signals from compatible amplifiers to the integrated ADC. A front panel mounted rotary memory switch allows the 1520 to address input memory sizes of 256, 512, 1K, 2K, 4K, 8K or 16K channels.

Three data acquisition modes are selectable via a front panel mounted rotary switch: Route, Sum and Route/Sum Modes.

In Route Mode, the enabled inputs are stored in corresponding segments of selected memory. That is, Input 1 is stored into the first memory segment, input 2 is stored into the second memory segment, and so forth, for all the selected number of enabled inputs.

Sum Mode allows enabled inputs to be stored into a single, common, memory segment. That is, all inputs are combined into a single spectrum. No routing occurs.

Route/Sum Mode combines the counting features of both Route Mode and Sum Mode. In Route/Sum Mode, the selected memory is divided into the number of input groups (N). Inputs 2 through N are stored in corresponding memory segments 2 through N, as in Route Mode. Input number 1 is not stored; memory segment 1 is used to sum Inputs 2 through N.

The operation of the 1520 is further enhanced by sixteen bi-colored front panel LEDs indicating the status of each enabled input. A red LED indicates the corresponding input is enabled, and the color changes to Green as the rate of accepted pulses increases. Thus, by watching the ADC Dead Time LED and Status LEDs, users have the ability to study overall system throughput.

The Model 1520 offers System 100 Multichannel Analyzer users the ability to provide independent start/stop and preset control for each input or groups of inputs. The operation of the 1520 with the System 100 requires the addition of a Model 4612 or Model 4622 Control Interface.

When used with conventional type MCAs, the 1520 offers users the ability to provide a single start/stop and preset control for all inputs.

Applications
The Model 1520 Integrated ADC-Mixer/Router was designed to be easily integrated into spectroscopy systems and applications providing high performance signal processing hosting a wide variety of MCAs. The 1520 offers

a variety of configuration possibilities: rack mounting, bench mounting, or integration into MCA/display systems, i.e., between the MCA (conventional or PC-based) and associated graphics display.

Hardware And Accessories
Accessories included with the 1520 for basic system integration and operation are: line cord, a 25-pin ribbon interface cable with D-type connectors, and rack-mounting hardware.

The 1520 has been designed to operate with conventional and PC-based MCA systems which use raster type monitors, both monochrome and enhanced color graphics types. When placed between the MCA and display as intended, it is subject to very intense electromagnetic and electrostatic noise, but the 1520 has been engineered to operate cleanly in this most demanding application. However, the external low level signal cables must be kept away from the display because coax cables offer little shielding from the effects of electromagnetic noise.

2. OPERATIONS

This section outlines the setup and operation of the Model 1520 Integrated ADC-Mixer/Router. Following these procedures will make you familiar enough with the instrument to be able to use it effectively in any situation.

2.1 LINE POWER SELECTION
Power is applied to the Model 1520 with the ac power switch on the signal processor's rear panel. Before applying power, check the voltage selection card inside the fuse compartment located on the rear panel. This is easily done by moving the plastic fuse shield to the left and looking directly under the fuse, the operating voltage will be visible. The 1520 is compatible with four line voltage ranges. Verify fuse is compatible with selected line voltage. To select a different operating voltage, please refer to Appendix B.1.

2.2 INTERNAL CONTROLS
Internal board jumper plugs are provided for added flexibility allowing application optimization and compatibility with equipment other than Canberra's. The jumper plugs are factory set for general purpose applications and for compatibility with Canberra MCA products and accessories. Please refer to Appendix B.2 for jumper plug access and Appendix B.3 for jumper plug functions.

2.3 CABLE CONNECTIONS
See Appendix D.5 for connector signals and Appendix F for details on the interface cables.

2.4 SETTING UP THE MIXER/ROUTER
Figure 4.1 represents a typical Mixer/Router setup. The rear panel ADC INPUTS switch must be set to M/R. In Route or Sum Modes, The amplifiers' outputs are connected to Mixer/Router Inputs starting with Input 1. For Route-Sum Mode, connections should be made to the Mixer/Router starting with Input 2, since MCA Memory Segment one is used to sum all the inputs. The following procedure demonstrates one way that the system may be set up and adjusted with a System 100 MCA. In this procedure, each external amplifier's gain is adjusted to establish a matching energy per channel.

To permit maximum resolution, set the INPUTS control to the smallest number that will allow all inputs to be used. Set the 1520's GAIN and MCA MEMORY SIZE as required for the experiment.

For ease in matching each amplifier's gain, set the MODE to SUM. After the gains have been matched, the MODE switch can be set to another position if necessary.

Set the 1520's controls to:

LLD: 0.05
ULD: fully clockwise (until the control clicks)
Digital Offset: all OFF

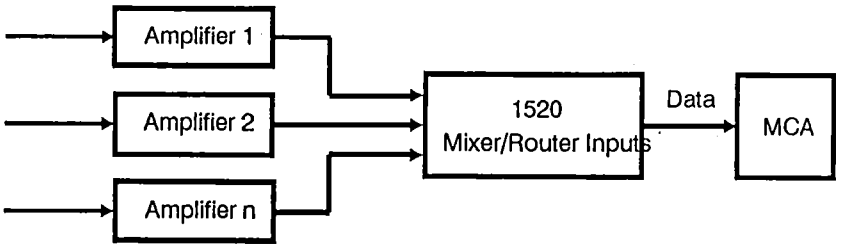
Using the System 100's Menu, enable the first input and start data acquisition, using a radioactive source such as ^{60}Co. Note the LED for the selected ACTIVE INPUT turns green, indicating accepted pulses. The %DT indicator will show the average dead time in increments of ten percent.

Adjust the amplifier's gain so that the spectrum is positioned conveniently on the display.

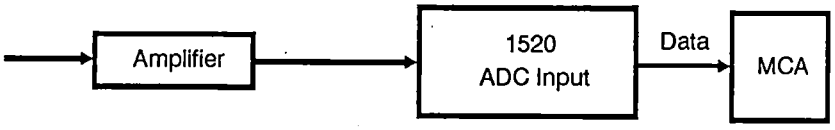
Using the same radioactive source, acquire a spectrum through each remaining input. Adjust each amplifier's coarse and fine gain so that each input's peak matches the location of the first input's peak. For high precision, use an amplifier equipped with an SFG (super fine gain) control.

2.5 USING INPUT TERMINATORS
In systems requiring less than the selected number of active inputs, it may be necessary to terminate the unused inputs when operating with the LLD set at its low end. The terminator should be a 50 ohm BNC type, such as the Canberra Model CA131 BNC Terminator.

2.6 ADC GATE
With the ADC set for PHA, the conversion of a linear input signal can be enabled or disabled by applying a signal to the GATE connector after the signal crosses the LLD setting but before the signal reaches its peak. The Gate signal pulse should be at least 250 ns wide.



Mixer/Router Setup



Single ADC Input Setup

Figure 2.1 Typical Model 1520 Setups

Depending on the criteria for the experiment in progress, the Gate input can be used in the factory-set COINCidence mode or, with a simple jumper change, can be used in the ANTIcoincidence mode. See Appendix B.3.

Coincidence Mode Gating
In the COINCidence mode, a signal at the GATE connector will act on the ADC in this way:

1. A low logic level (0 to 0.8 V) at the GATE connector will disable the ADC. It will neither accept nor process any linear signals while the Gate input is low.

2. A high logic level (2.5 to 5.5 V) at the GATE connector will enable the ADC. It will accept and convert all linear signals received while the Gate input is high.

3. If the Gate input is left open (unconnected), the ADC will act as if the input were high and will accept and convert all linear signals received.

Anticoincidence Mode Gating
In the ANTIcoincidence mode, the logic is reversed. That is, a low logic level will enable the ADC and a high level (or an open input) will disable the ADC.

2.7 SAMPLED VOLTAGE ANALYSIS (SVA)

To use the Sampled Voltage Analysis (SVA) mode, the Mixer/Router must be disabled by setting the rear panel ADC INPUTS switch to EXT, and by changing the PHA/SVA jumper on the 1520's ADC board to the SVA position. See Appendix B. To return to the PHA mode, the 1520's jumper must be restored to the PHA position.

In the Sampled Voltage Analysis mode, analog voltages (dc or slowly changing ac voltages) can be sampled by the ADC, resulting in an amplitude distribution curve. The input signal must be between 20 mV and 10 V in amplitude and must be between the LLD and ULD settings, which can be used to set an amplitude acceptance window if desired.

The Gate input, which is used as the sampling signal, must be coincident with the voltage to be sampled. Sampling occurs when the GATE input is high; conversion is initiated at the input's high to low transition.

The Gate sampling period or pulse width must be equal to or greater than 1 μs, but must be narrower than the voltage pulse width being sampled.

2.8 POWER ON SEQUENCE

When the 1520 is used with conventional MCAs (that is, any MCA that issues only a single start/stop command to the Mixer/Router), the MCA must be turned on first. The 1520 must find the MCA's Interface Bus in a known state so that at power on it can properly initialize its input control registers. On a System 100 with a Model 4612 or 4622 Control Interface this is not a problem since the System 100 will initialize the 1520's input control registers.

3. CIRCUIT DESCRIPTION

Throughout the following circuit descriptions, please refer to the indicated block diagram.

3.1 ANALOG-TO-DIGITAL CONVERTER (ADC)

The 1520 uses a Wilkinson-type ADC (Figure 3.1), which captures the input signal on a holding capacitor then determines the signal's amplitute by discharging the capacitor at a constant rate while counting clock pulses into an address register.

Prior to the acquisition mode, the ADC stretcher is normally active and will track and follow signals present at the input. If no conversions are in progress and the input signal threshold is exceeded, the Busy flip-flop will be set. Linear Gate (LG) is enabled, indicating the ADC is acquiring a signal and the stretcher will detect the peak of the input signal. When the input signal reduces to 90% of its peak value, and provided the SCA and coincidence requirements are met, a conversion will be initiated. The start convert flip-flop is set, Linear Gate (LG) ends, and the ADC conversion begins.

The precision ramp-down current source and counters are synchronously enabled. A binary counter, driven by a 100 MHz clock, is enabled for the duration of the ramp down sequence. When the stretcher voltage reaches the ADC zero reference, the ramp and counters are gated off ending the conversion. The resultant digital address in the counter represents the magnitude of the ADC input.

The converted address is loaded into the tri-state bus drivers and DATA READY request is set initiating data transfer.

In response to DATA READY, the MCA or computer sets ENABLE DATA true, which activates and enables the tri-state bus drivers allowing the ADC address to be presented on the data bus. At the conclusion of the Data Storage Cycle, DATA ACCEPTED is enabled clearing the DMA Ready flip-flop.

If the pulse was not within the LLD/ULD window, or if the GATE criterion was not met or REJECT was set, the stretcher ramp down sequence would have been aborted. The stretcher capacitor would be reset, quick discharge (dump) to prepare for a new input.

3.2 MIXER/ROUTER

The Mixer/Router (Figure 3.2) has two main sections, the Input Multiplexer and the Digital Router. Valid input pulses are multiplexed through the Input Multiplexer and sent to the ADC. Pulses converted by the ADC are routed to the proper MCA Memory Segment by the Digital Router. The Mixer/Router also has an External Control Interface. It is through this interface that the System 100 can individually start and stop data collection on each input.

Input Multiplexer

Each Mixer/Router input has a separate Threshold Detector. All Threshold Detectors have a common threshold voltage which is designed to track the ADC's Lower Level Discriminator (LLD) voltage. When an Input's pulse exceeds the threshold, its Threshold Detector triggers the Input Select Logic. If that input is Active, (Collect ON for it) a Select Code identifying the input is generated. This four bit Select Code addresses the Input Multiplexer, causing it to steer the selected input signal into the ADC.

When the Select Code is generated, the unit becomes Busy, locking out all other inputs until the selected input signal has been converted and Routed to the MCA. To provide zero resolving time between detected inputs, a priority encoder circuit is used. When two or more input pulses are detected at the same time, the priority encoder resolves the conflict by selecting the higher input number.

Digital Router

The Digital Router uses the Select Code and the front panel switch settings to route pulses converted by the ADC to the MCA Memory Segment for the detected input. It consists of a Range Generator and a Segment Address Generator.

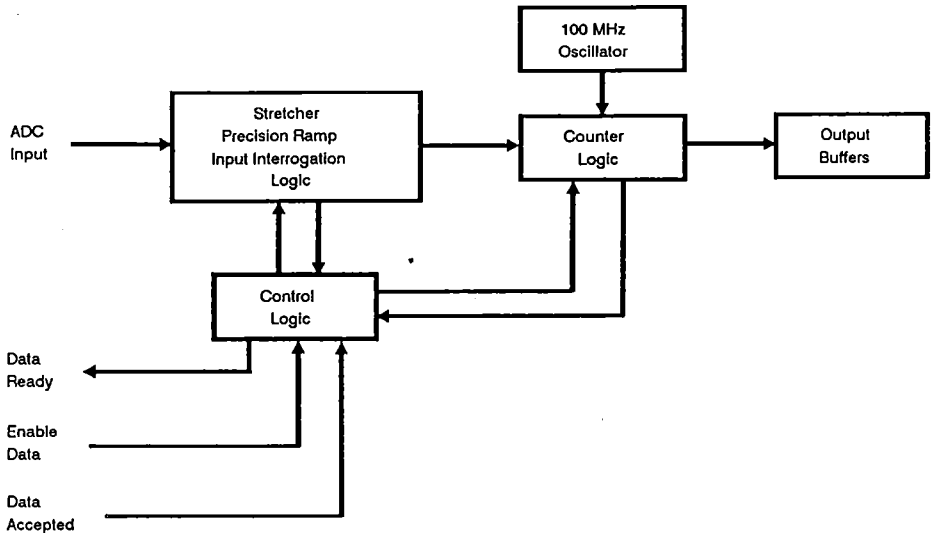


Figure 3.1 ADC Block Diagram

Range Generator
The Range Generator gets its input from the MCA Memory Size, Inputs and Mode control switches. The Range is used by the ADC and the Segment Address Generator. The Range Generator provides an enable control for each input. In Route and Route-Sum Modes, Range is equal to the selected MCA MEMORY SIZE divided by the selected number of INPUTS, and is between the limits of 256 channels and 8192 channels.

If the selected switch combinations were to result in a Range of less than 256 Channels, the Range Generator outputs a Range Code of 256 and starting with input 1, enables only those inputs that will allow a 256 channel MCA Memory Segment for each enabled input. For example, with the MCA MEMORY SIZE switch set to 1K, and the INPUTS switch set to 8, the Range code is set to 256 channels (1024/8 = 128, but the minimum possible Range is 256) and allows only the first four inputs (1-4) to be enabled.

If the MCA MEMORY SIZE is set to 16K and the INPUTS switch is set to 1, the Range code is set to 8192 channels, the maximum possible Range. In the Sum Mode, the Range is equal to the MCA Memory Size up to the limit of 8192 channels.

Segment Address Generator
The Segment Address Generator is used to place each input pulse converted by the ADC into its associated memory segment. The Segment Address Generator gets its input information from the Range Code, the Input Select Code, and the five most significant bits (MSB) from the ADC conversion. From the Range Code, the Segment Address Generator determines the most significant bit from the ADC. With this information and the Input Select Code, the Segment Address Generator pads in the remaining Address Bits to the MCA. For example, with INPUTS switch set to 8 and MCA MEMORY SIZE switch set to 16K, the Range for each Input is 2K channels. Therefore, the MSB from the ADC is 2^{10}. With this setup, the Segment Address Generator pads in Address bits 2^{11} through 2^{13}, so that a converted pulse from Input 1 bits 2^{11} through 2^{13} are set to all zeros and for Input 8 they are set to all ones.

In Route-Sum Mode, the Segment Address Generator generates a two cycle memory transfer to the MCA for each ADC conversion. The first cycle updates data to the Sum Segment (memory segment one) and the second cycle

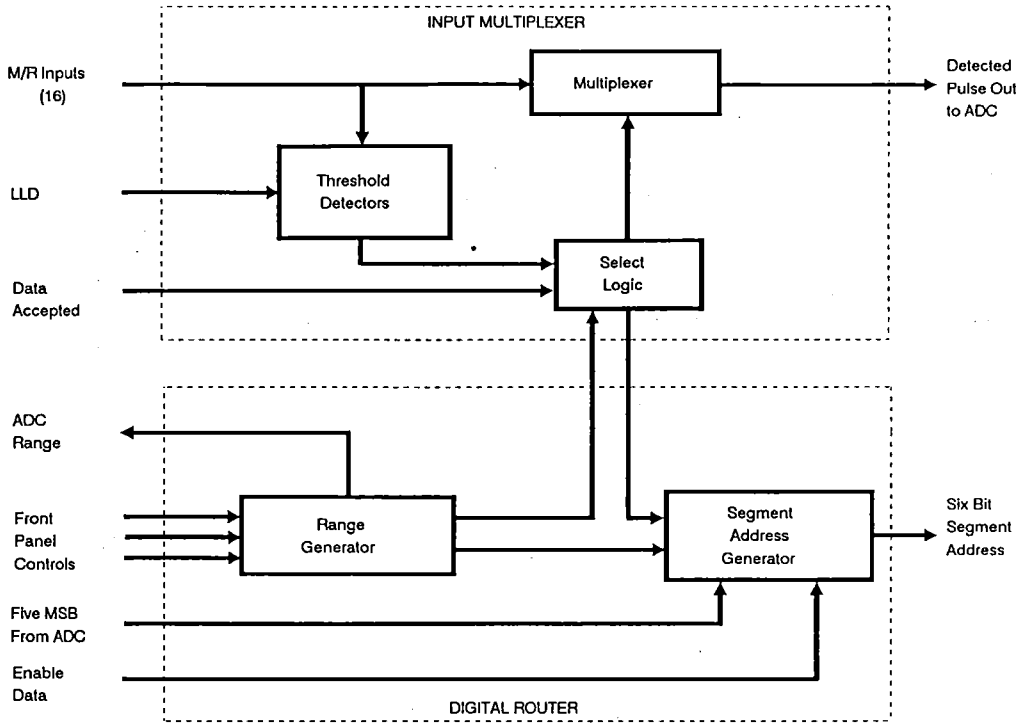


Figure 3.2 Mixer/Router Block Diagram

updates data in the memory segment corresponding to the detected input.

External Controls

Each Mixer/Router input has a separate Active Control Register. This allows MCAs, such as the System 100 with a Model 4612 or 4622 Control Interface, to individually start and stop the collection of data on each input. The Model 1520 will also operate with any Canberra MCA that has an External ADC Interface. With these MCAs, the Model 1520 will set all inputs enabled by the Range Generator to active. This allows the MCA to start and stop collection on all active inputs with a single command.

A. SPECIFICATIONS

A.1. MIXER/ROUTER

INPUTS

MIXER/ROUTER IN – Sixteen inputs, rear panel BNC connectors. Accepts positive unipolar or bipolar (positive lobe leading) pulses; amplitude 0 to +10 V, ±12 V maximum; minimum rise time 1 μs; pulse width 2 μs to 100 μs; Z_{in} = 1.22 kilohms; direct coupled.

OUTPUTS

MIXER/ROUTER OUT – Rear panel mounted toggle switch selects internal connection to ADC IN (M/R setting) or ADC EXTERNAL (EXT setting).
DATA OUT – Provides TTL-compatible address lines on rear mounted 25-pin D-type connector for proper routing of the data (shared with ADC).

FRONT PANEL CONTROLS

MCA MEMORY SIZE – Seven-position rotary switch selects MCA Memory Segment Size, 256, 512, 1K, 2K, 4K, 8K or 16K channels, for all enabled inputs. The selected Memory Size is divided by the user-selected number of inputs to obtain the Memory Segment Size for each input.
INPUTS – Five-position rotary switch selects the number of enabled inputs: 1, 2, 4, 8 or 16.
MODE – Three-position rotary switch selects ROUTE, SUM or ROUTE/SUM acquisition mode. ROUTE permits enabled inputs to be routed into corresponding segments of selected MCA Memory Size. SUM allows enabled inputs to be stored in selected memory (no routing). In ROUTE/SUM MODE the selected memory is divided by the number of inputs (N). Inputs 2 through N are stored into corresponding memory segments 2 through N, as in Route Mode. Input number 1 is not stored; memory segment number 1 is used to sum Inputs 2 through N.

FRONT PANEL INDICATORS

INPUT – Sixteen bi-colored LEDs, one for each INPUT. Red indicates input is enabled; color changes to green as rate of accepted pulses increases.
POWER – Front panel LED.

PERFORMANCE

GAIN – Unity ± 2%
DYNAMIC RANGE – 0 to +10 V.
INTEGRAL NON-LINEARITY – < ± 0.05% of full scale over the top 98% of range.
GAIN DRIFT – < ± 0.02% of full scale/°C, after a 60 minute warm-up.
ZERO DRIFT – < ± 300 μV/°C, after a 60 minute warm-up.
RESOLVING TIME – 0 ns via priority encoder.
MINIMUM GROUP SIZE – 256 channels.
THRESHOLD – Minimum detectable signal tracks with ADC's LLD control.

A.2. 100 MHz ADC

INPUTS

ADC IN – Accepts positive unipolar or bipolar (positive lobe leading) pulses; amplitude 0 to +10 V, ±12 V maximum; rise time 0.25 to 100 μs; width 0.5 μs minimum; Z_{in} = 5 kilohms, direct coupled; rear panel BNC connector with rear panel toggle switch to select M/R or EXT.
ADC GATE – Internal jumper plugs provided for selecting Coincidence/Anticoincidence and PHA/SVA. PHA Mode: With Coincidence (Anticoincidence) selected, a positive (negative) TTL level during time-to-peak will enable conversion and storage of a pulse, logic low (high) will cause pulse to be rejected; factory set to Coincidence. Sampled Voltage Analysis (SVA) Mode: GATE IN signal is used to sample ADC EXT signal; accepts positive TTL logic pulse or dc level; SVA pulse width ≥ 1 μs. Coincidence/SVA loading: 4.7 kilohm pull-up resistor to +5 V. Rear panel BNC connector.

OUTPUTS

DATA – Provides 13 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 25-pin D-type connector. Data Lines are negative true; shared with Mixer/Router.

FRONT PANEL CONTROLS

GAIN – Six-position rotary switch to select full scale resolution of input signal; selection of 256, 512, 1K, 2K, 4K and 8K channels for a 10 V pulse.
OFFSET – Six rocker DIP switches to provide suppression of the digital zero; 0 to 8064 channels in multiples of 128 channels.
LLD – Ten-turn locking-dial precision potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range 0.02 to +10 V dc.
ULD – Screwdriver adjusted 22-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range 0.02 to +10.5 V dc.
ZERO – Screwdriver adjusted 22-turn potentiometer sets the ADC's analog zero intercept level; range ± 5% of input range; resolution 0.005% of full scale.

FRONT PANEL INDICATORS

% DT – Ten-segment LED indicator displays the average Dead Time (DT) of the converter.

INTERNAL CONTROLS

PHA/SVA – Jumper plug J1 selects PHA or SVA acquisition mode. Factory set to PHA.
COINC/ANTI – Jumper plug J2 selects Coincidence or Anticoincidence gating mode. Factory set to COINC.
ENABLE CONVERTER POS/NEG – Jumper plug J3 selects polarity of the command signal; factory set to positive true.
DATA BUFFER ENABLE/DISABLE – Jumper plug J4 enables or disables the data buffer; factory set to enable.
READY – Jumper plug J8 selects polarity of Data Ready signal; factory set to negative true.
DATA ACCEPTED – Jumper plug J9 selects polarity of Data Accepted signal; factory set to negative true.
ENABLE DATA – Jumper plug J10 selects polarity of Enable Data signal; factory set to negative true.

DEAD TIME POLARITY – Jumper plug J11 selects polarity of Dead Time signal; factory set to positive true.

PERFORMANCE

INTEGRAL NON-LINEARITY – < ± 0.025% of full scale over the top 99.5% of range, including effects from tilt.
DIFFERENTIAL NON-LINEARITY – < ± 0.7% over the top 99.5% of range.
DRIFT, GAIN – < ± 0.009% of full scale/°C, after a 60 minute warm-up.
DRIFT, ZERO – < ± 0.0025% of full scale/°C, after a 60 minute warm-up.
DRIFT, LONG TERM – < ± 0.005% of full scale/24 hours at a constant temperature.
PEAK SHIFT – < ± 0.025% of full scale at rates up to 50 kHz.
ADC DEAD TIME – The sum of Linear Gate Time, Conversion Time and Memory Cycle Time.
CONVERSION TIME – 1.5 μs + 0.01 (N + X) μs where N is the Address Count, and X is the effective digital offset.
CHANNEL PROFILE – Typically flat over 90% of channel width.

A.3. SYSTEM

STANDARD ACCESSORIES

A22540 – Rack mount hardware, included with 1520.
C1547-1 – Ribbon cable, 25-pin D-type connectors, 0.5 m (1.5 ft). Mates with the Canberra System 100, Series 35 PLUS, Series 90 and Series 95 ADC interface input connectors, included with 1520. Consult factory for possible compatibility with other MCAs.

OPTIONAL ACCESSORIES

C1547-4 – Ribbon cable, 25-pin D-type connectors, 1.2 m (4.0 ft); may be ordered in place of C1547-1 cable at no extra charge; specify with order.
C1545A – Shielded ADC/MCA interface ribbon cable, 3.0 m (10.0 ft). Available at extra cost.
Control Interface required for System 100 independent start/stop. Model 4612 for PC bus MCA; Model 4622 for Micro Channel bus MCA.

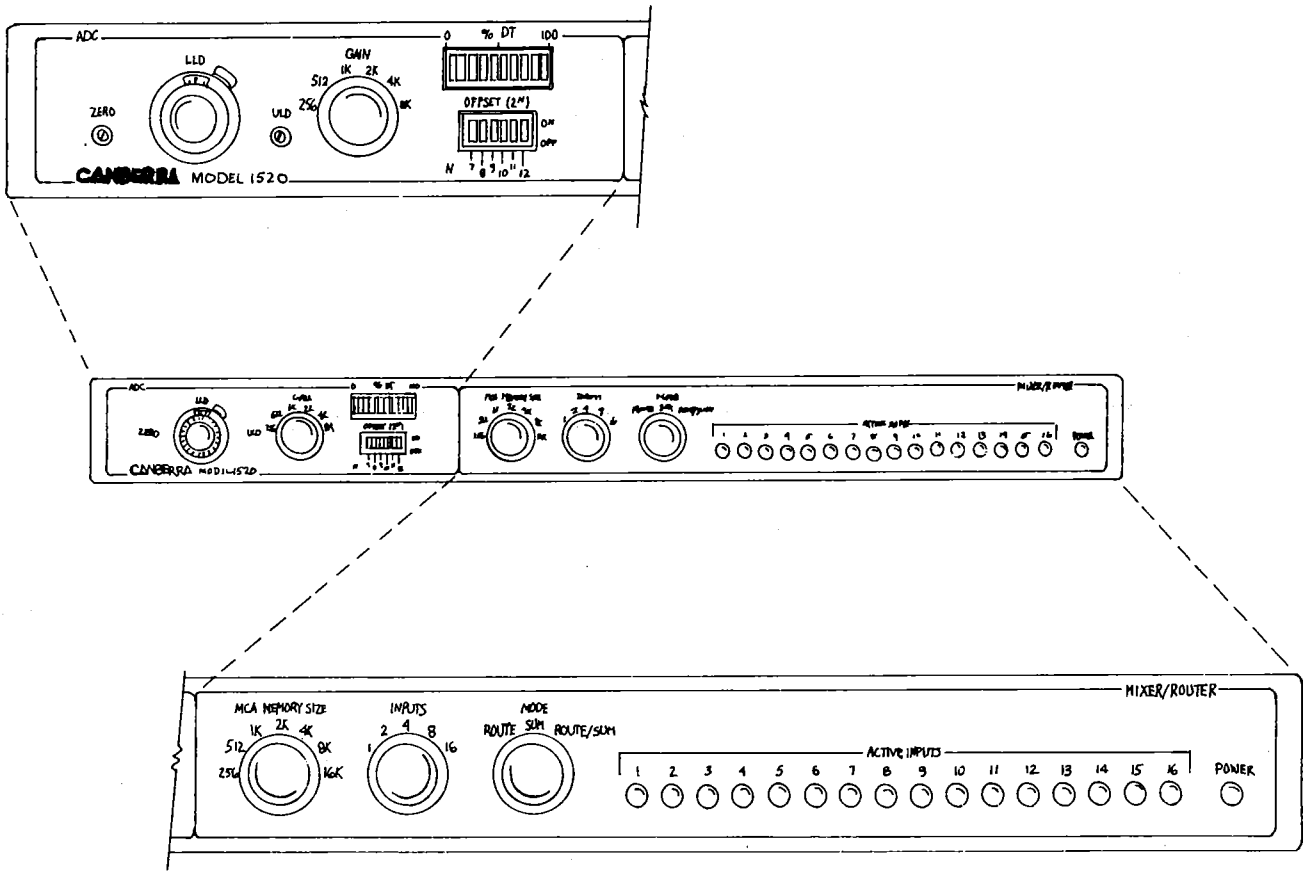


Figure A.1 Model 1520 Front Panel

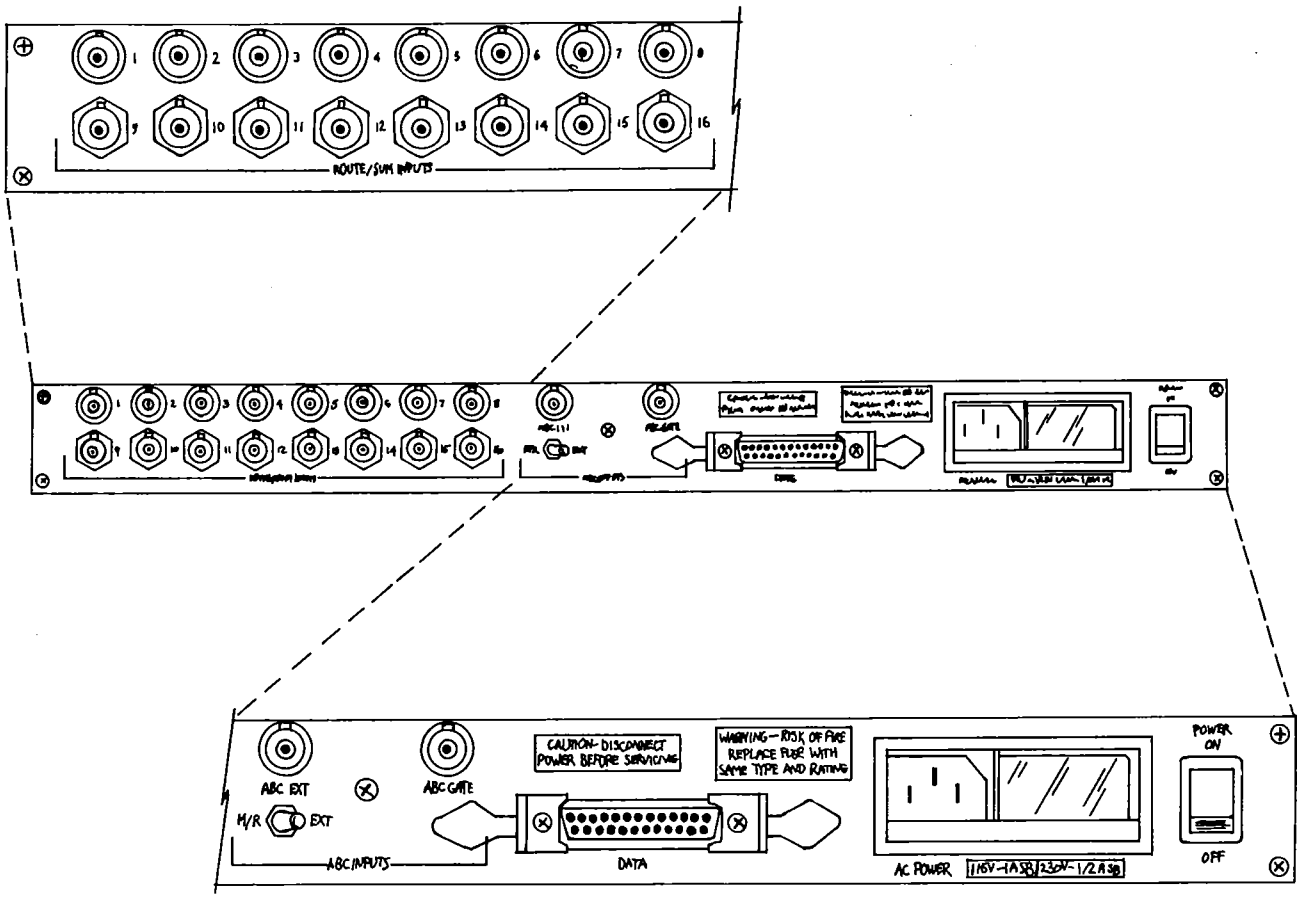


Figure A.2 Model 1520 Rear Panel

PHYSICAL

SIZE – 4.45 x 42.5 x 39.1 cm (1.75 x 16.75 X 15.38 in), height x width x depth.
WEIGHT – 5 kg (11 lbs)
SHIPPING WEIGHT – Approximately 7.3 kg (16 lbs)
AC POWER – 90 to 110 V, 105 to 125 V, 195 to 235 V and 210 to 250 V; rear panel jumper plug selectable; 50 to 60 Hz; approximately 35 W. Front panel LED ON/OFF indicator, rear panel ON/OFF switch.
OPERATING TEMPERATURE – 0 to 40 °C, ambient.

B. INTERNAL CONTROLS

B.1. LINE VOLTAGE SELECTION

To change the operating voltage of the 1520, slide the plastic fuse shield, next to the ac line cord socket, to one side. The voltage selection printed circuit card is located just below the fuse. The operating voltage that the 1520 is set for will be visible on the card. Figure B.1.

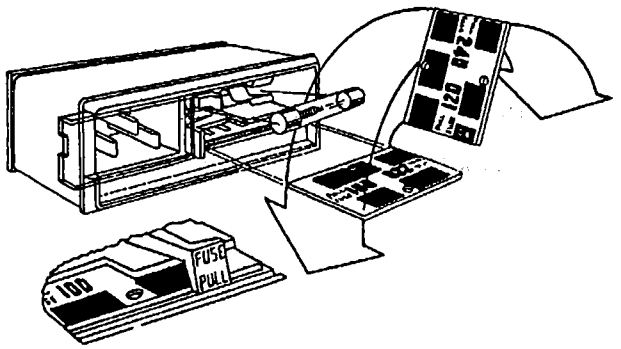


Figure B.1 Voltage Selection

Be sure to change the fuse when changing the operating voltage. Use 1 A SB for 95-125 V. Use ½ A SB for 195-250 V.

To change between 120 V and 240 V or to change to low-line voltage,(100 V or 220 V), pull the selector card out of its socket and replace it so that the desired voltage is visible beneath the fuse. A pair of needle-nose pliers is useful here.

B.2. CASE REMOVAL

Remove the 1520 from its case to gain access to the jumper plug options.

WARNING

Hazardous voltages are present inside the 1520.

Turn off the ac power and remove the ac line cord from the rear of the 1520 before opening the case.

1. Remove the following knobs:

   MCA MEMORY SIZE
   INPUTS
   MODE

2. Remove the two case securing screws on top of the case.

3. On the 1520 front panel, align the LLD control's locking tab with the corresponding cutout in the front panel.

4. Begin pushing the 1520 out of the case, to the rear, by pressing firmly on the LLD knob. The knob may need to be jiggled slightly to get it to pass through its mounting hole.

5. With the 1520 slightly out of the case, grasp the rear panel and heat sink and pull the 1520 out of the case.

6. To reassemble, slide the 1520 into its case from the rear. Align the LLD control's locking tab with the cutout on the control's front panel mounting hole. The LLD knob may need to be jiggled slightly to get it to move through its front panel mounting hole. When the 1520 is properly reassembled, the LEDs and the %DT display should protrude slightly through the front panel.

7. Reinstall the knobs and the two securing screws.

B.3. ADC INTERNAL JUMPERS

The ADC jumper plugs have been factory preset for common applications and for compatibility with all Canberra MCAs. For other MCAs and special applications, please consult the user manual for the intended instrument's requirements. Figure B.2 shows jumper plug locations.

J1, PHA/SVA

Sets the data acquisition mode to PHA or SVA. Shipped in the PHA mode.

J2, ANTI/COINC

Selects COINCidence or ANTIcoincidence ADC Gate control. Shipped in the COINCidence mode.

J3, Enable Converter

Set the polarity of the Enable Converter signal, pin 18 on the ADC Data Connector. Shipped in the POSitive true (enable) position. For more details, please refer to Appendix D, Model 1520 Interfacing and Data Transfer.

J4, Data Buffer

Enables (B) or disables ($\overline{B}$) the ADC Data Buffer. Shipped in the enabled (B) position. For more details, please refer to Appendix D, ADC Interfacing and Data Transfer.

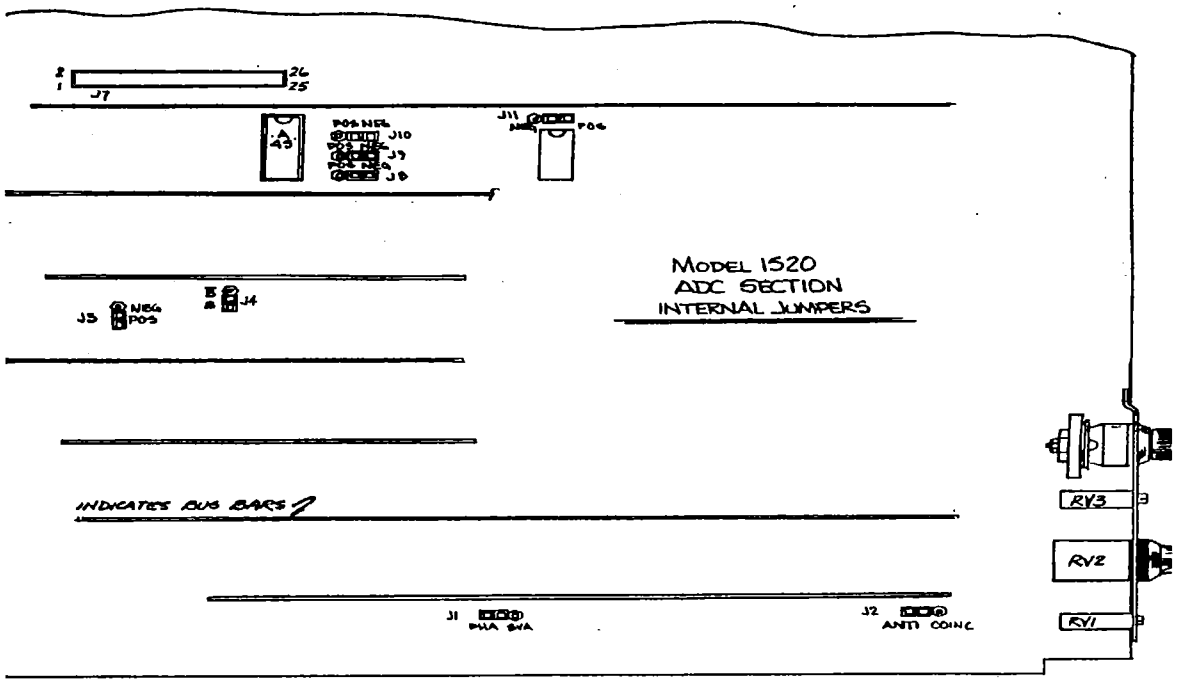


Figure B.2 ADC Internal Jumpers

J8, Data Ready
Sets the polarity of the DATA READY signal, pin 14 on the ADC Data Connector. Shipped in the NEGative true (enable) position.

J9, Data Accepted
Sets the polarity of the DATA ACCEPTED signal, pin 17 on the ADC Data Connector. Shipped in the NEGative true (enable) positin.

J10, Enable Data
Sets the polarity of the ENABLE DATA signal, pin 22 on the ADC Data Connector. Shipped in the NEGative true (enable) position

J11, Dead Time Polarity
Sets the polarity of the dead time MCA transfer signal, pin 21 on the ADC Data Connector. Shipped in the POSitive position.

C. ADC ZERO ADJUSTMENT

The Zero control varies the zero intercept of the ADC conversion function so that zero energy is stored in channel zero of the memory. The Model 1520 is shipped with the ADC Zero set for a Gain of 8192 and with inputs to the ADC from the Mixer/Router. For other ADC Gains or for ADC inputs from an external signal, a slight adjustment of the Zero control may be necessary for precise energy calibration, but is not critical.

For accurate setting of the Zero control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. To adjust the ADC Zero for operations through the External ADC input, the 1520's rear panel switch must be set to EXT. Connect the 8210 Pulser's SIGNAL OUT to 1520's ADC EXT connector.

To adjust the ADC Zero for operations with the Mixer/Router section, the rear panel switch must be set to M/R. Connect the 8210 Pulser's SIGNAL OUT to the 1520's ROUTE/SUM input 1 and set the 1520's front panel SUM switch to SUM.

2. Set the 1520's GAIN control to the desired position. Set the 1520's MCA MEMORY SIZE switch to equal MCA's Memory Size.
3. Set the Pulser to HI, 0°, +, and 0.5 μs Rise Time.
4. Set all binary switches on the 8210 to the ON (right-hand) position, turn ON the RELAY, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.
5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be switched in on the 1520. For instance, if the memory is 4K channels and the GAIN is set for 8K, an OFFSET of 4K (2^{12} switch ON) must be added so that conversion can take place in the highest channel of the memory.
6. Turn all binary switches on the Model 8210 OFF, except the 1/64 switch, which should be left ON.
7. Set all OFFSET switches on the 1520 to the OFF position.
8. Adjust the 1520's front panel ZERO control so that counts are being collected in the proper channel, as follows:

ADC GAIN	CHANNEL
8K	128
4K	64
2K	32
1K	16
512	8
256	4

9. Steps 4 through 8 are interactive, so they should be repeated until no further adjustments are necessary.

D. MODEL 1520 INTERFACING AND DATA TRANSFER

This Appendix will provide information that will be helpful when interfacing the ADC to an MCA.

D.1. ADC-MIXER/ROUTER DATA TRANSFER

A typical conversion for input multiplexing and data transfer sequence is illustrated in Figure D.1.

1. Enabled input into Mixer/Router is detected.
2. Detected input signal is multiplexed to the ADC.
3. ADC recognizes input signal and captures peak value.
4. If the SCA and Gate conditions are met, the ADC automatically initiates conversion when the input signal falls to 90% of its peak value.

   From the Range and Input Select Code the Router generates the Segment portion of the address.
5. When a valid conversion is complete, the 1520 issues the DATA READY signal. With the Data Buffer enabled, the 1520 can start processing another input while the last conversion is being transferred to the MCA's memory.
6. MCA enables the 1520 address data.
7. MCA issues DATA ACCEPTED, resets DATA READY, and releases the 1520, allowing subsequent data transfer cycles.

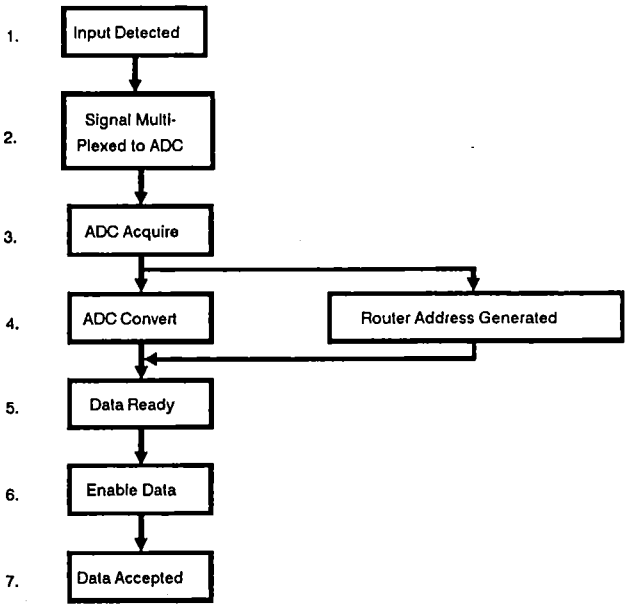


Figure D.1 Typical Conversion Sequence

The result of the ADC Conversion is a coded number or address having a maximum number of bits, determined by the ADC Gain setting. The Digital Router inserts the remaining most significant bits so that the combined result is a 14 bit address code. At the conclusion of the conversion, the address data is transferred into a holding register and the data transfer signal DATA READY is set true. The address data is now valid and can be accessed and used by the MCA or CPU.

If the Data Buffer is enabled, the ADC can begin the next conversion even though data transfer to the memory unit is still in process. If the Data Buffer feature is disabled, the ADC is not allowed to begin subsequent conversions until the data transfer sequence concludes.

The address lines are driven by tri-state drivers activated by ENABLE DATA initiated by the data memory device.

When transfer is complete, the memory device sets DATA ACCEPTED true, releasing the ADC to begin the next transfer sequence.

D.2. DEPENDENT ADC APPLICATIONS

Data Buffer Hold Time

The ADC and Router data buffers have a maximum hold time of 1 ms. Normally this does not present a problem, since MCA data transfer times are 1 to 20 μs. However, for longer ADC service times that could be experienced with computer-based data acquisition systems, incorrect conversion values can result.

Multiparameter Applications

In multiparameter applications involving multiple ADCs, coincident events are acquired for PHA and List Storage. In this case, using the data buffer might let the ADCs get out of synchronization, allowing data transfer for non-coincident events.

Disabling the Buffer

To insure proper coincident data collection and synchronization, and in applications involving long ADC service times, it is advisable to disable the ADC Data Buffer. See Appendix B.3, jumper J4.

D.3. INVALID FLAG

It may sometimes be necessary to record all inputs whether valid or not. "Invalid Flag Conditions", below, describes the conditions which will set the INValid flag output (signal INV on Data Connector pin 20). Because of the ADC Data Buffer operation, the ADC can begin a second conversion even though the first event was not yet accepted by the memory storage device. If a second conversion is completed and is found to be invalid prior to the transfer of the first conversion, there is no way to determine which event, the first or the second, is invalid. Thus, without using the GATE or ENABLE CONVERTER inputs, there is no INValid/DATA synchronization.

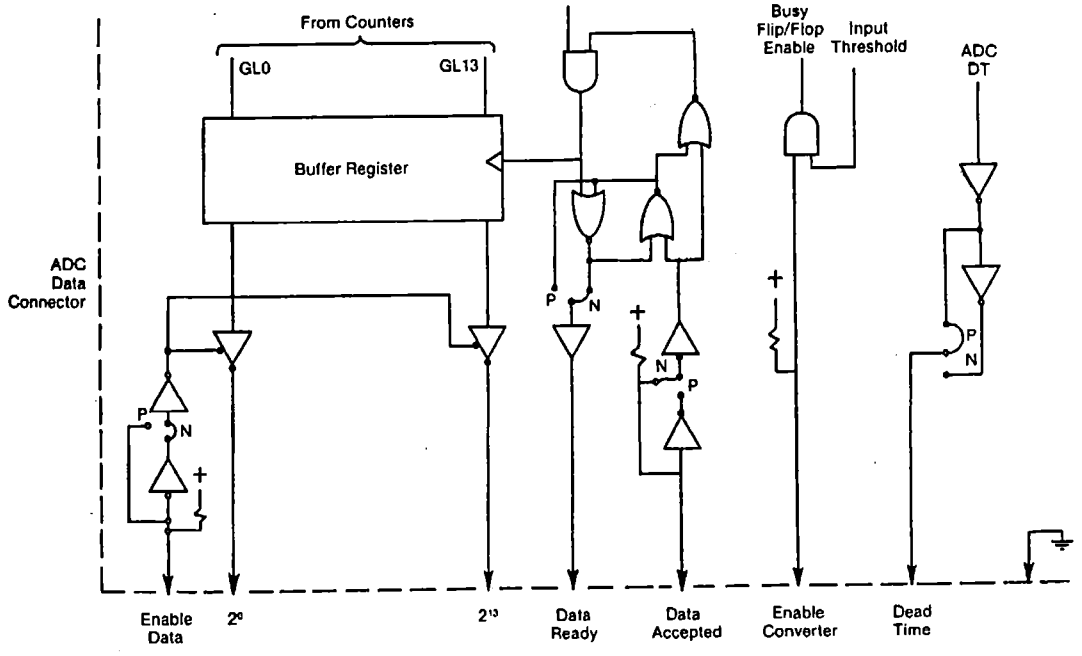


Figure D.2 Interfacing Logic

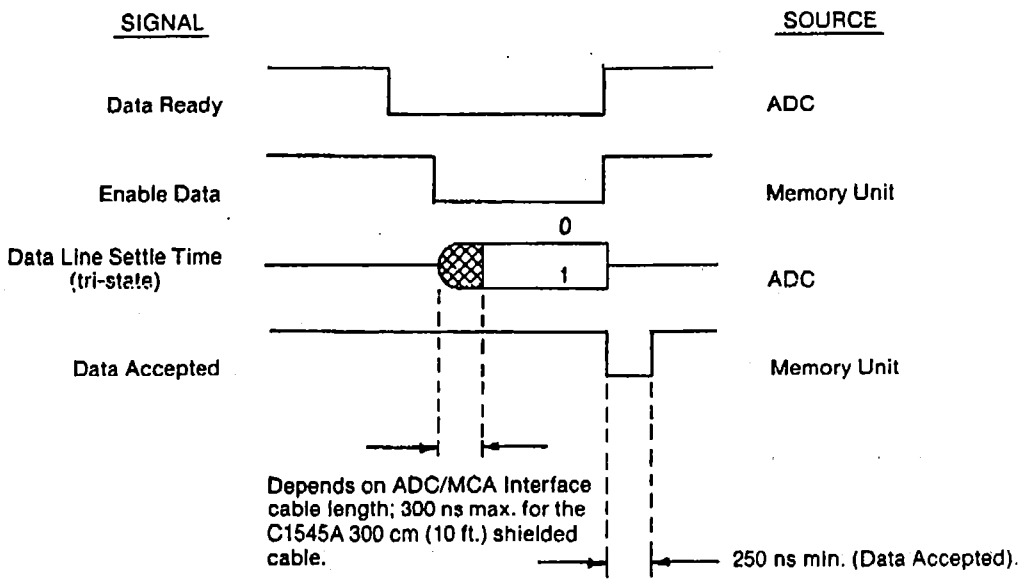


Figure D.3 Data Transfer Timing Diagram

Invalid Flag Conditions
For a conversion to be accepted, it must meet all of the following criteria. When any criterion is violated, the INValid flag (Data Connector pin 20) will be set.

SCA Window – Pulses not in the SCA's analog window will be rejected, initiating a dump cycle. An LLD or a ULD violation will generate the INValid flag. Both states are interrogated at the 90% point.

Baseline – Input pulses exceeding the LLD but not the ADC ZERO baseline will be rejected, initiating a dump cycle. The condition is interrogated at the 90% point, setting the INValid flag when violated.

Digital Underflow – Input pulses resulting in a numeric conversion less than the counter back-bias or less than the digital offset, or both, will be rejected by inhibiting ADC READY. The INValid flag will be set at EOC (end of conversion).

Digital Overflow – Input pulses resulting in a numeric conversion greater than the ADC RANGE will be rejected by inhibiting ADC READY. The INValid flag will be set at EOC (end of conversion).

Late Coincidence/Anticoincidence – The GATE pulse width must be at least 250 ns wide and be true (high or open circuit for coincidence, low for anticoincidence) for at least 100 ns prior to the 90% point or the end of Linear Gate. Otherwise the conversion is aborted by initiating a dump cycle. The INValid flag will be set at the 90% point.

D.4. DEAD TIME
The Dead Time output is the sum of the ADC conversion time. The ADC dead time component begins when an input signal crosses the input threshold, 20 mV to 100 mV controlled by the LLD, and ends at the conclusion of conversion.

D.5. ENABLE CONVERTER
The ENABLE CONVERTER input (DATA connector pin 18) can be used to inhibit a later conversion allowing synchronization of multiple ADCs. If a conversion is in process when the signal is received, it will be allowed to finish its data transfer.

D.6. J102 DATA CONNECTOR SIGNALS

Pin	Signal	In/Out
1	2^0	Output
2	2^1	Output
3	2^2	Output
4	2^3	Output
5	2^4	Output
6	2^5	Output
7	2^6	Output
8	2^7	Output

9 2^8 Output
10 2^9 Output
11 2^{10} Output
12 2^{11} Output
13 2^{12} Output
15 2^{13} Output

Pins 1-13 and 15 are gated binary address output data. Negative true (0 V) as standard: TTL Tri-state outputs are enabled by setting ENABLE DATA (pin 22) to a logic 0. $V_O > 3$ V at 20 mA (High); $V_O < 0.9$ V at 20 mA (Low)

14 DATA READY Output
Signals external memory storage unit that a conversion is complete; positive true or negative true logic, set by internal jumper J8; shipped in negative true.

17 DATA ACCEPTED Input
Feedback signal from the memory storage unit which acknowledges data acceptance. This pulse resets the ADC and clears the INValid flag, if set. Positive true or negative true logic set by internal jumper J9; shipped in negative true. TTL hysteresis input with a 4.7 kilohm pull-up resistor to 5 V.

18 ENABLE CONVERTER Input
Used to gate the ADC on or off. Pulses in progress prior to initiation of this signal will be allowed to finish the output sequence; further inputs will be ignored. Positive true or negative true logic set by internal jumper J3; shipped in positive true. TTL hysteresis input with a 4.7 kilohm pull-up resistor to 5 V.

20 $\overline{\text{INV}}$ Output
Invalid; set by digital under or overflow (OVF) if the ADC input is not within the SCA window or does not exceed the ZERO intercept setting. Invalid may also be set if the linear input with a COINC Gate signal is not large enough to cause conversion. Reset by the DATA ACCEPTED signal. Negative true logic. TTL output with a 4.7 kilohm pull-up resistor to 5 V.

21 DEAD TIME Output
Used to enable live time circuitry to control storage periods. Positive true or negative true logic, set by internal jumper J11; shipped in positive true. TTL output with a 4.7 kilohm pull-up resistor to 5 V.

22 ENABLE DATA Input
Used to gate the 13-bit data onto the output lines. Positive true or negative true logic, set by internal jumper J10; shipped in negative true; TTL hysteresis input with a 4.7 kilohm pull-up resistor to 5 V.

23 $\overline{\text{IOACK}}$ Output
Acknowledge strobe from the Mixer/Router, in response to an Input-Output command from the MCA (S100). See Appendix G for details.

24 GND
Ground.

25 $\overline{\text{I/OCMD}}$ Input
Input-Output command from the MCA (S100) to the Mixer/Router. Used to read Mixer/Router setup status and to enable and disable Mixer/Router inputs. See Appendix G for details.

E. RACK MOUNT HARDWARE

Rack mount brackets and hardware are included in the 1520 accessory package. Using the supplied number 10-32 × 1/4 pan-head screws, attach the left and right brackets as shown in Figure E.1.

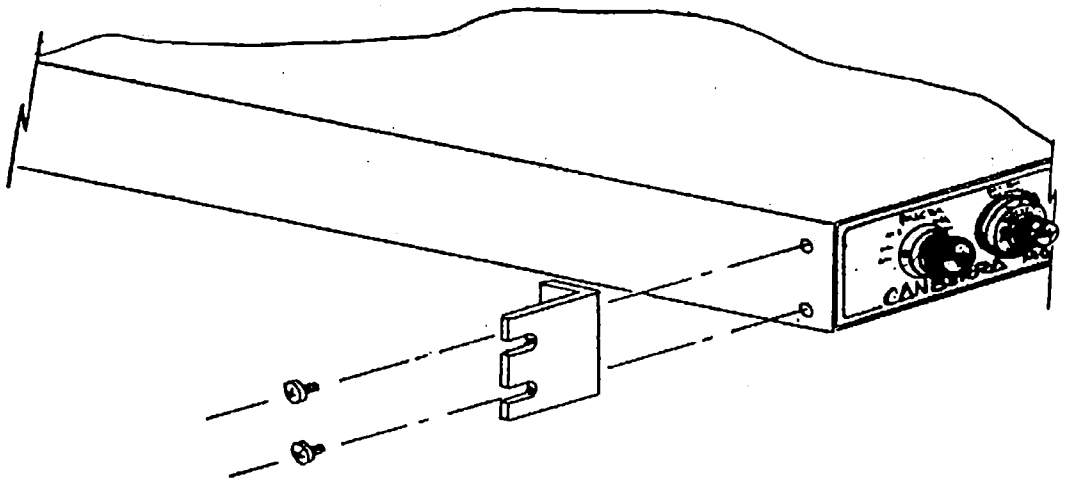


Figure E.1 Installing the Rack Mount Hardware

F. INTERFACE CABLES

This Appendix provides information regarding the available 1520/MCA interface cable options and connector retaining hardware assembly.

F.1. HARDWARE INSTALLATION

The MCA end of the C1547-1 interface cable does not have the retaining hardware installed. A small bag containing the hardware is included as part of the 1520 accessory package.

Two connector retaining methods commonly employed are jack screws and catch set (spring clips).

Since the retaining method your application uses is unknown, both types of hardware are provided to allow compatibility.

Two connector retaining methods commonly used are jack screws and a catch set (spring clips).

Since you application may use either method, both types of hardware have been provided to allow compatibility.

Determine which method is to be used on the intended MCA and assemble the appropriate hardware as shown in Figure F.1.

F.2. C1547-4 INTERFACE CABLE

A 1.2 m (4 ft.) version of the interface cable is available which allows the Model 1520 to operate in applications requiring a longer cable length.

If this cable was specified with the order, it will be provided without additional cost instead of the standard 0.5 m (1.5 ft.) C1547-1 cable.

F.3. C1545A INTERFACE CABLE

A 3 m (10 ft.) shielded cable is available to allow operation with an MCA separated from the 1520 by up to 3 m (10 ft.)

Connect the flying ground leads at each end to a nearby chassis ground screw.

This cable is available at extra cost, please consult the factory.

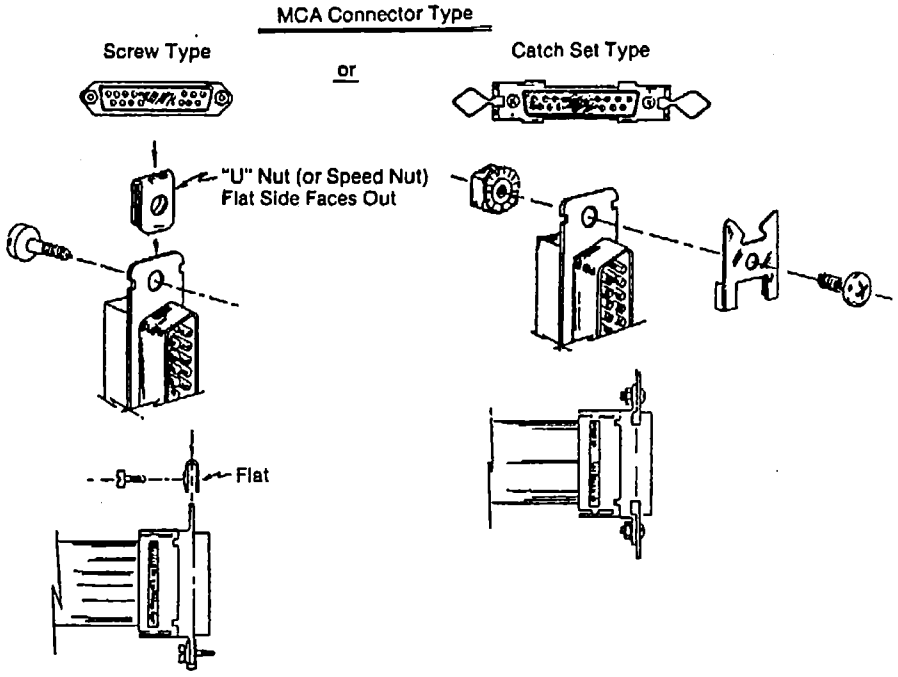


Figure F.1 Assembling the Connector Hardware

G. I/O INTERFACE

The I/O Interface allows the System 100 MCA with 4612 or 4622 Control Interface to control the start-stop of each input or group of inputs and to read the setup status of the Mixer/Router. The I/O Interface consists of two 8-bit Input Control Registers, one 8-bit Status word and Bus Control Logic. Data is transferred via the MCA/1520 data cable on bits 2^0 through 2^7, where bit 2^0 is the LSB.

In the following description all reference to "Logic One" or "True" is understood to be zero volts into or from the 1520.

G.1. STATUS REGISTER

The 8-bit Status Register gives the MCA the Range, Number of Inputs and Mode setting of the 1520 as follows:

Data Bits 2^2 2^1 2^0	Range
0 0 0	256 channels
0 0 1	512 channels
0 1 0	1K channels
0 1 1	2K channels
1 0 0	4K channels
1 0 1	8K channels

Data Bits 2^5 2^4 2^3	Number of Inputs
0 0 0	1
0 0 1	2
0 1 0	4
0 1 1	8
1 0 0	16

Data Bits		Mode
2^7	2^6	
0	0	Disabled*
0		Sum
1		Route/Sum
1	1	Route

*When the rear panel EXT-M/R toggle switch is in EXT, the Mixer/Router Inputs are disconnected from the ADC. In this condition, the Number of Inputs status is always 1 regardless of the INPUTS switch setting.

G.2. INPUT CONTROL REGISTERS

The two 8-bit Input Control Registers gives the 1520 a separate control for each of the 16 Mixer/Router inputs. A Logic One to the associated Control Register bit will enable the input and a Logic Zero will disable it.

Control Register One controls inputs 1 through 8, where bit position 2^0 controls input 1. Likewise Control Register Two controls inputs 9 through 16, and bit position 2^0 controls input 9.

At power on, both control registers are set so that all inputs are enabled. This is to allow MCAs that are not equipped

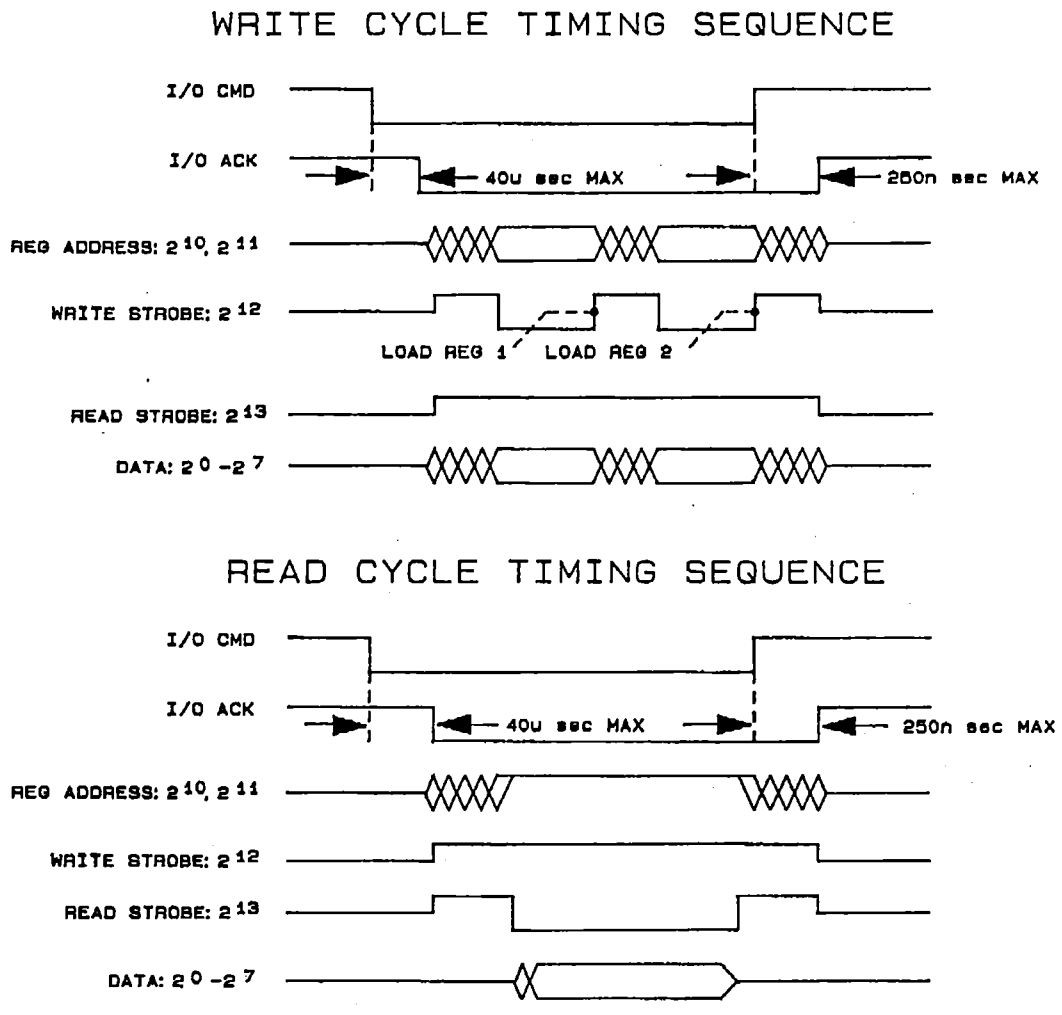


Figure G.1 I/O Interface Timing

with a Control Interface to start and stop all inputs with a single command.

G.3. BUS CONTROL LOGIC

The MCA initiates a Read or Write to the 1520 by asserting (zero volts) control signal I/OCMD. If the data bus is NOT Busy (no data transfer in progress from the Digital Router and/or the ADC, to the MCA) the 1520 asserts (zero volts out) signal I/OACK. When the MCA receives the I/OACK, it outputs the Read or Write address control on data bus bits 2^{10} through 2^{13}. The following table lists the command codes from the MCA, where 1 is zero volts.

Bus Bits				Function
2^{13}	2^{12}	2^{11}	2^{10}	
0	1	1	0	Load Control Register 1
0	1	0	1	Load Control Register 2
1	0	0	0	Read Status

Figure G.1 shows a diagram of the Read and Write (Load) timing sequence.

Request for Schematics

Schematics for this unit are available directly from Canberra. Write, call or FAX:

Training and Technical Services Department
Canberra Industries
800 Research Parkway, Meriden, CT 06450
Telephone: (800) 255-6370 or (203) 639-2467
FAX: (203) 235-1347

If you would like a set of schematics for this unit, please provide us with the following information.

Your Name _____

Your Address _____

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Unit's model number _____

Unit's serial number _____

Note: Schematics are provided for information only; if you service or repair or try to service or repair this unit without Canberra's written permission you may void your warranty.

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We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

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