Model 1510
Integrated Signal Processor

3/95

User's Manual

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Table of Contents

List of Figures

1. Introduction

The Canberra Model 1510 offers multichannel analyzer users research-grade front end signal conditioning and processing electronics in a low profile, self contained instrument. The 1510 is compatible with both conventional and PC-based multichannel analyzers.

The 1510 contains a high quality, high resolution spectroscopy amplifier with pile-up rejection and live-time correction, a 13-bit (8192 channel) Wilkinson-type ADC, and a versatile low noise bias supply suitable for use with all types of detectors. All components are integrated into a compact, low noise, EMI/RFI resistant chassis that is less than five cm (two in.) tall. The 1510 is suitable for bench mount, rack mount, or integration with personal computer based MCAs.

The 1510 is designed for spectroscopy applications in physics, education, environmental work, nuclear chemistry, and health physics. The advanced design ensures excellent performance in electronically noisy environments. Because of this, it is possible to place the 1510 between a Personal Computer chassis and a CRT monitor with little or no degradation in performance. Additionally, the 1510 has built-in protection against the most common types of ground loops that sometimes plague conventional high resolution systems.

The 1510 ADC/MCA interface is jumper plug configurable for compatibility with all Canberra MCA products. To receive the 1510 properly configured for the intended Canberra MCA application, the configuration must be ordered using one of these three Model numbers:

1510-01	The -01 option is for use with the Series 35, Series 35 Plus, Series 40, Series 80, Series 85, Series 88, Series 90, Series 95 and System 100 MCAs.
1510-02	The -02 option is for use with the AccuSpec/B and AccuSpec/MC MCAs.
1510-03	The -03 option is for use with the Model 556 Acquisition Interface Module (AIM).

1.1 High Voltage Bias Supply

The high voltage bias supply features low noise, low ripple and excellent stability. It accommodates all types of detectors providing either positive or negative bias at selectable regulated voltages of 15 to 2000 V dc at 1 mA or 30 to 5000 V dc at 300 µA.

The bias supply will withstand an overload or a direct output short-circuit for an indefinite period and resume normal operation when the fault is removed. The output voltage may be turned On or Off remotely through the HVPS INH connector.

A convenient rear panel programming module provides selection of range and polarity. Polarity status is indicated by a front panel LED which can be previewed prior to activation of the power supply.

A front panel LED indicates an inhibit condition if the Bias Supply is inhibited by an LN_2 monitor or other external control.

1.2 Spectroscopy Amplifier

The amplifier provides unipolar shaping with active, complex-pole filter networks optimized for superior pulse symmetry, overload recovery, and signal to noise ratio ensuring the highest resolution and throughput. A wide choice of front panel selectable Shaping time constants (0.5, 1, 2, 4, 8 and 12 µs) allows optimum matching of detector and count rate requirements.

A gated baseline restorer is employed with features and flexibility found only in top-of-the-line amplifiers. Automatic restorer rate and threshold remove the guesswork from setup ensuring optimal performance over a wide range of system and count rate conditions. Flexibility and performance are further enhanced with a choice of asymmetrical or symmetrical restoration.

Amplifier gain can be set precisely with the super fine gain control, which provides resolution better than 1 in 16 000 (0.006%).

The 1510 amplifier's exceptional dc stability, ultra low noise, optimum pulse shaping, and high performance baseline restorer offer uncompromising performance when used with germanium, Si(Li), scintillation, gas proportional, or silicon charged-particle detectors.

1.3 Pile-up Rejection/Live-time Correction

The Live-Time Corrector and Pile-Up Rejector allows quantitative gamma spectrum analysis nearly independent of system count rate. Special circuitry interrogates for pile-up and permits only those detector signals resulting from single energy events to be processed.

To compensate for rejected pulses and processing times, a system dead time is generated which extends the collection time by an appropriate amount.

A front panel LED is provided as a user aid when setting the PUR discriminator.

1.4 ADC

The ADC is a Wilkinson type counter/ramp converter with a clock rate of 100 MHz, providing high throughput rate along with exceptional linearity and accuracy.

A direct-coupled input of 0 to 10 volts, provided by the 1510 or from an external amplifier, is digitized according to the front panel GAIN control into a binary code of 8 through 13 bits (256 through 8192 channels).

A choice of Pulse Height Analysis (PHA) or Sampled Voltage Analysis (SVA) are offered. Conversion in PHA mode is initiated automatically using an internal peak detector. The falling edge of a pulse applied to the ADC GATE input initiates the SVA conversion.

Conversions may be enabled or disabled by Coincidence/Anticoincidence gating or acceptance criteria programmed by the Lower Level (LLD) and Upper Level (ULD) discriminators.

Digital OFFSET and ADC RANGE can be employed to expand a portion of the input maintaining high resolution with limited memory.

The ADC is compatible with all Canberra MCAs and PC-based MCAs using the external interface options designated for each unit. The binary TTL-compatible interface logic can be set for positive (logic high) true or negative (logic low) true ensuring compatibility with many other MCA and memory systems.

2. Applications, Hardware and Accessories

The Model 1510 Integrated Signal Processor was designed to be easily incorporated into spectroscopy systems and applications providing high performance signal processing on a wide variety of MCAs. The 1510 configurations include: rack mounting, bench mounting, or integration into MCA/display systems between the MCA (conventional or PC-based) and its graphics display.

2.1 Hardware and Accessories

Accessories included with the 1510 for basic system integration and operation are: a line cord, an ADC to MCA interface cable, two 1.5 m (5 ft) BNC coax cables, one 0.2 m (0.5 ft) BNC coax cable, one 1.5 m (5 ft) SHV high voltage coax cable, one BNC barrel connector, one SHV barrel connector, one 1.5 m (5 ft) preamp power extender cable, and rack-mounting hardware.

2.2 Applications

Figure 2.1 shows a typical application for a NaI(Tl) Detector System and Figure 2.2 shows a typical Ge Detector System application.

The 1510 has been designed and engineered to operate in conventional and PC-based MCA system environments that use raster type monitors, conventional monochrome and enhanced color graphics types. When installed between the MCA and display as intended, it is subject to very intense magnetic and electrostatic noise.

The 1510 provides effective resistance to the effects of this most demanding application. However, careful attention must also be given to the low level signal cables external to the 1510 as ordinary coax cables offer little shielding from the effects of electromagnetic noise.

The AMP IN signal cable is a special 1.5 m (5 ft) flying lead cable terminated with a BNC connector. The SHV high voltage coax cable, HVPS INH, and preamp power extender cables are provided and installed to facilitate a neat cable assembly when connected to the detector cable set. The cables have been bundled together, maintaining maximum performance under these demanding EMI conditions.

The 1510 Amplifier's selection of shaping-time constants allows it to be used in surface barrier, PIPS proportional counter, NaI and Ge detector applications. The choice of shapings also allows the best possible performance by tailoring the system for the conflicting requirement of optimum signal-to-noise ratio and high count-rate performance. The excellent stability and low noise contribution enhances the use of this amplifier in most applications.

Nuclear spectroscopy with high count rates can be made more accurate by testing for pulse pileup and rejecting contaminated pulses. Pulse pileup produces distortions in the higher

ranges of the spectrum because successive shaped amplifier pulses tend to merge, and cause aberrations in the precise amplitudes as measured by the ADC. Since many spectra have higher count rates at the lower energies, the pileup of these pulses strongly affects the less intense higher energy counts and can result in significant errors. A pileup reject circuit provides substantial improvement to the spectrum.

If pulses are rejected from further analysis by the circuitry, the system is "dead" for some portion of time. It is customary to correct for dead or busy time in the ADC; this dead time should also be activated when a pileup reject circuit is operated with the ADC. The Model 1510 can extend the system dead time to compensate for pulses thrown away due to pileup rejection.

Typical applications are shown in Figure 2.1 for a system with a Ge detector and Figure 2.2 for a system with a NaI(Tl) detector.

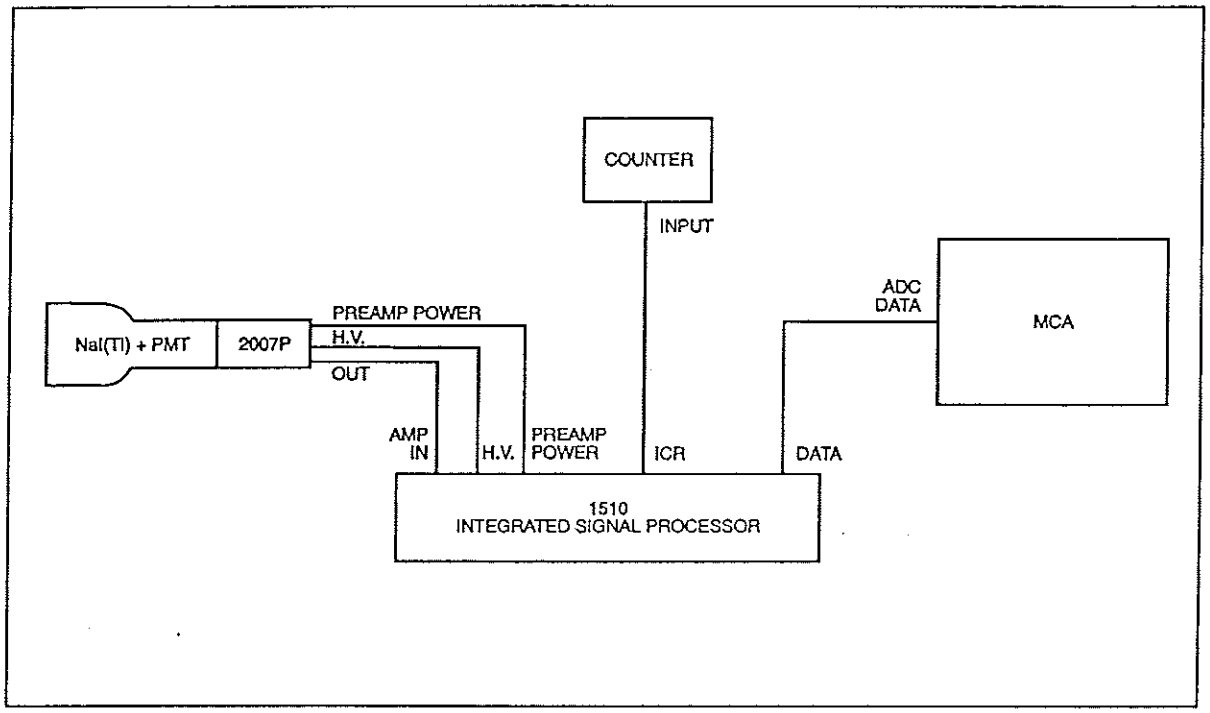

Figure 2.1 A Typical Nal(Tl) System

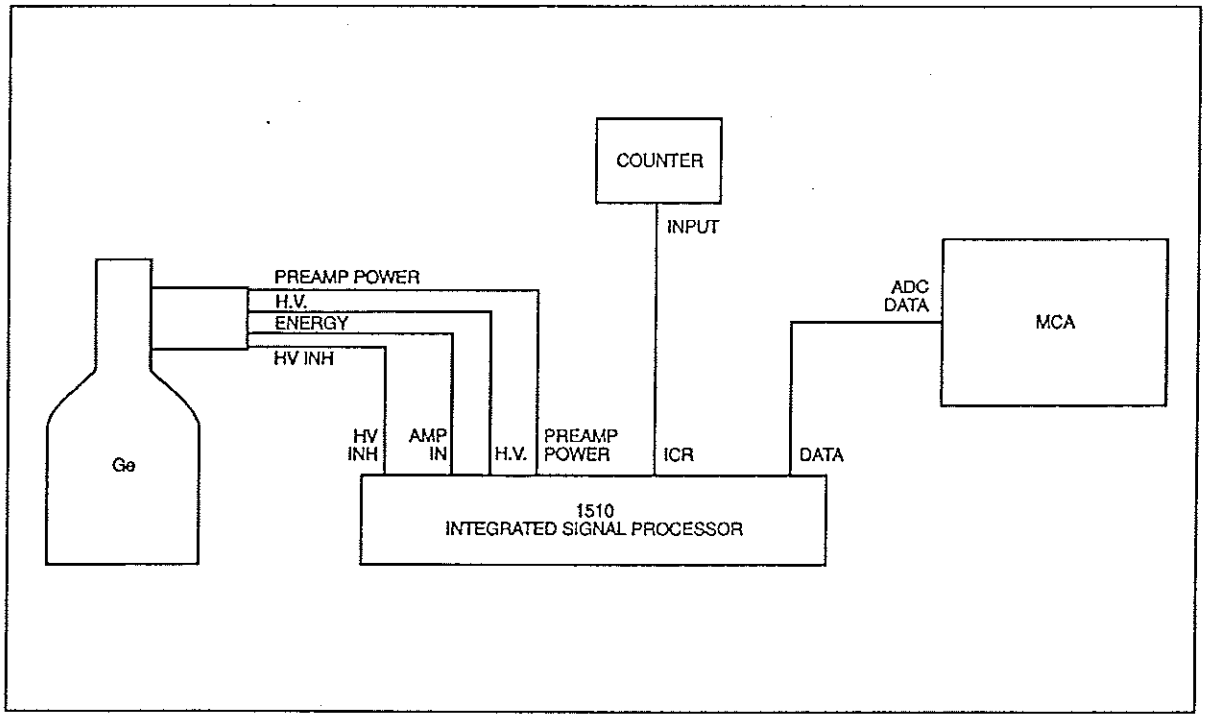

Figure 2.2 A Typical Ge System

3. Setup

This section describes how to connect the system, how to set the internal controls, and how to select ac power and high voltage options.

3.1 Setting Internal Controls

Internal jumper plugs are provided for added flexibility and compatibility with all Canberra MCA products. Jumper plugs associated with the 1510 Spectroscopy Amplifier are factory set for general purpose applications. Jumper plugs associated with the ADC are factory set specific to the 1510 Model number and the intended Canberra MCA interface. The 1510 model numbers and MCA applications are listed below:

1510-01	The -01 option is for use with the Series 35, Series 35 Plus, Series 40, Series 80, Series 85, Series 88, Series 90, Series 95 and System 100 MCAs.
1510-02	The -02 option is for use with the AccuSpec/B and AccuSpec/MC MCAs.
1510-03	The -03 option is for use with the Model 556 Acquisition Interface Module (AIM).

Please refer to Appendix C for jumper plug access and detailed information for your specific 1510 model.

3.2 Selecting the Proper AC Power Option

Power is applied to the Model 1510 with the rear panel ac power switch. Before applying power, check the voltage selection card inside the fuse compartment located on the rear panel. This is easily done by moving the plastic fuse shield to the left and looking directly under the fuse; the operating voltage will be visible. The 1510 is compatible with four line voltage ranges. Be sure that the fuse is compatible with selected line voltage. To select a different operating voltage, please refer to Appendix C.1.

3.3 Selecting the High Voltage Range and Polarity

High Voltage range and polarity are conveniently selected by the programming module located on the rear panel. The 1510's High Voltage Power Supply is factory set for the positive 30 to 5000 V (300 μA, max) range, which is compatible with most Ge detector applications. If your detector requires negative polarity and/or the higher current (1 mA, max; 15 to 2000 V range), refer to Appendix B for instructions. Please consult your detector's manual for its specific bias requirements.

CAUTION Excessive voltage and/or incorrect polarity can permanently damage the detector system.

The LEDs in the 1510's front panel HVPS section indicate polarity status when the 1510 is turned on and provide a polarity selection preview, whether the 1510 High Voltage Bias Supply is on or off.

Please refer to Appendix B for instructions on changing the 1510's high voltage polarity or voltage range.

4. System Integration and Connections

This section provides basic installation instructions for integrating the 1510 with the spectroscopy system's MCA and detector.

4.1 Installation

Install the 1510 for the intended application: rack mount, bench mount or integration into an MCA graphics display system.

For rack-mount applications, the rack-mount hardware must first be installed, as described in Appendix G.

The instructions that follow will primarily focus on integration into MCA/graphics display systems using the System 100 or Series 95 MCAs and a Ge detector, with the 1510 on top of the MCA, between the MCA and the monitor.

4.2 Cable Connectors

Before installing the C-1547-4 ADC/MCA interface cable, you must first determine which of two types of connector retaining methods is to be used (See Figure 4.1). The System 100 uses screws while the Series 90 and Series 95 use spring clips. To provide compatibility, both spring clips and screws have been included.

For retainer installation illustrations and instructions, please refer to Appendix H.

Note: It is not necessary to install the retaining hardware, but is advised to prevent an accidental disconnection during system operation.

4.3 Cabling

Install the ADC/MCA interface cable, connecting the data transfer link. The 1510 uses the spring clip retaining method. The ADC/MCA interface cable is 1.2 m (4 ft) long, which will accommodate most installations. If your installation requires a longer cable, an optional 3 m (10 ft) cable is available for the 1510-01.

Referring to Figure 2.1 as a guide for germanium detector systems, or to Figure 2.2 for sodium iodide detector systems, connect the 1510 cable assembly to the detector's preamplifier. For germanium detectors, note that the 1510's cable set connects to the detector's cable set, not to the preamplifier.

The 1510 cable set, shown in Figure 4.2, consists of the SHV high voltage cable (1), the AMP IN cable (2), the preamp power cable (3), and the HVPS INH cable (4). The figure also shows how the cable assembly must be routed away from the MCA system's monitor.

Note: Do not let the 1510 cable bundle get near the system's monitor as noise will be induced in the low level signal cables, degrading the 1510's resolution performance.

Verify that the 1510's adjacent rear panel AMP OUT and ADC IN signals are connected with the supplied 0.5 ft BNC coax cable.

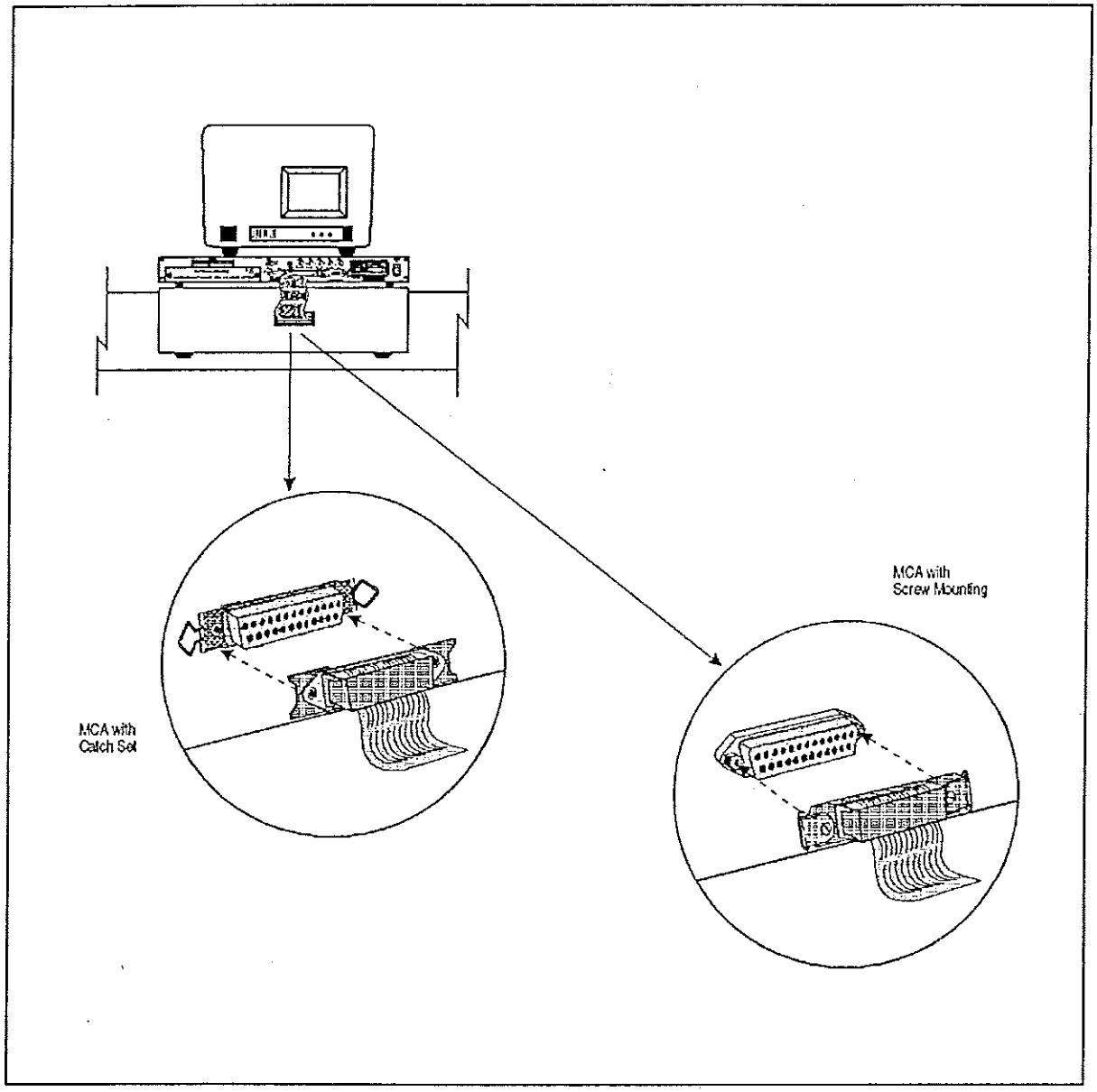

Figure 4.1 Attachment of ADC/MCA Interface Cable

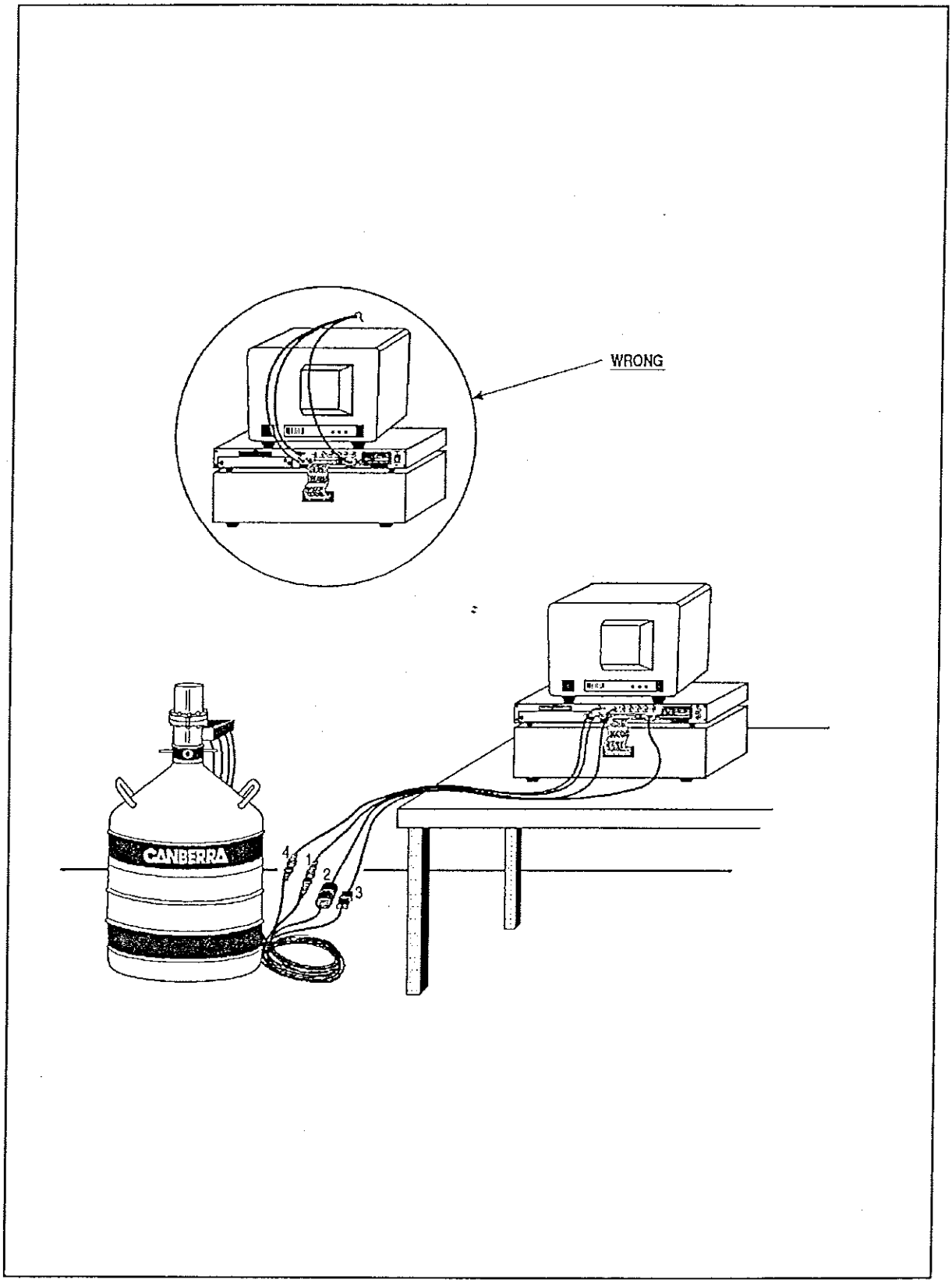

Figure 4.2 Model 1510 Cable Installation and Cable Routing

5. Operation

This section outlines the operation of the Model 1510 Integrated Signal Processor. Following these procedures will make you familiar enough with the instrument to be able to use it effectively in most situations.

5.1 Pre Turn-On

Verify that the High Voltage bias supply programming module is properly installed (see Section 3.3 and Appendix B). Please refer to your Detector's User's Manual for its required polarity and range.

Verify that the HV ON/OFF Switch is *off* and the VOLTAGE Control is set to 0.00 (fully counter-clockwise).

Verify that the 1510's ac input selection is compatible with the intended ac line power (see Section 3.2 and Appendix C.1).

Connect the Model 1510 as shown in Figure 5.1 (the counter is optional).

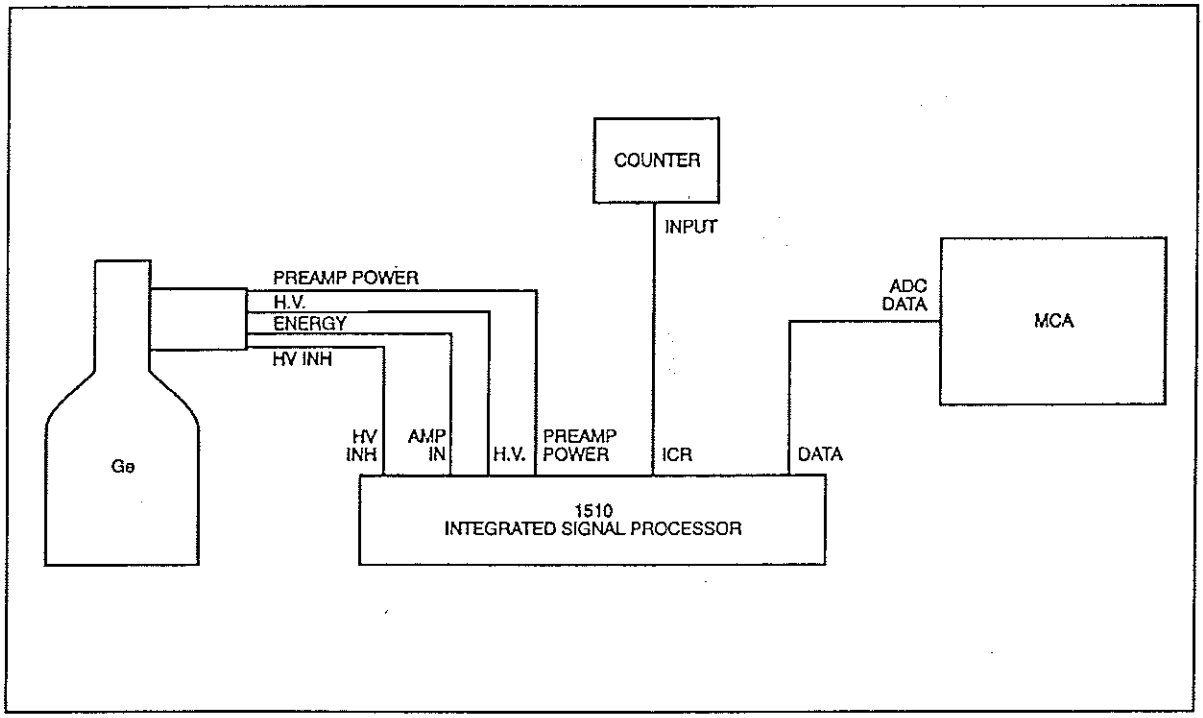

Figure 5.1 PUR/LTC System Setup

5.2 Turn On

Connect the 1510 to a compatible ac power source and set the 1510's rear panel Power On/Off switch to *on*.

Verify that the proper front panel High Voltage polarity LED (POS or NEG) is illuminated. The detector High Voltage bias polarity and range were previously selected in Section 5.1.

CAUTION Incorrect High Voltage bias and/or polarity can permanently damage the system's detector.

Verify that no segments of the High Voltage Indicator are illuminated.

Set the front panel HV ON/OFF Switch to *on*. The first segment of the High Voltage Indicator should now illuminate.

Note: Illumination of the High Voltage Indicator's first segment indicates that the high voltage supply is active.

Slowly increase the VOLTAGE control until the operating voltage of the system detector is attained.

The High Voltage Indicator should illuminate at 600 V per segment, showing the voltage present at the rear panel HVPS OUT connector.

Note: High Voltage control is provided by a direct-reading precision 10-turn dial. For the 5 kV range, the bias supply will respond up to 5.00 + 10%. The bias supply will limit and not respond to further increases of the dial's setting.

With the 2 kV range selected, the bias supply will likewise respond only up to 2.00 + 10%. Again, the supply will limit and not respond to further increases of the dial's setting.

5.3 Amplifier Setup

For a detailed explanation of the Amplifier's Front Panel Controls, please refer to Appendix A.1.3.

Set the amplifier controls as indicated below:

Shaping	4 µs
Coarse Gain	100
Fine Gain	7.2
PUR On/Off	OFF

Set the amplifier Polarity switch to match the preamp's output polarity; positive (+) for a Canberra Model 2001 or 2002 preamp.

Place a radioactive source such as ^{60}Co near the face of the detector.

Monitor the amplifier output signal on the 1510 front panel P/Z Insp test point using a oscilloscope and scope probe. Connect the probe ground to the PUR ON/OFF switch body.

Semi-Gaussian shaped pulses approximately 9 V in amplitude should be observed when using a preamp gain of 100 mV/MeV and ^{60}Co radioactive source.

5.4 Pole/Zero (P/Z) Adjustment

For more detail on and an illustration of the P/Z adjustment procedure, please refer to Appendix D.1.

The P/Z trim is extremely critical for good high count-rate resolution performance. Adjust the radioactive source for a count rate between 2 kcps and 25 kcps.

Set the oscilloscope vertical sensitivity for 50 mV/div.

Press the inspect button while monitoring the amplifier's output at the 1510 front panel P/Z Insp test point with an oscilloscope. This will clamp the unipolar signal, preventing scope overload that might otherwise occur with the higher vertical sensitivity.

Adjust the Pole/Zero so that the trailing edge of the unipolar pulse returns to the baseline with no over- or under-shoots.

5.5 ADC Setup

For a detailed explanation of the ADC's Front Panel Controls, please refer to Appendix A.2.3.

Set the ADC GAIN and RANGE equal to the MCA's memory group size. For instance, set the ADC RANGE and GAIN to 4096 for an MCA with 4096 memory size.

Set the ADC controls as indicated below:

Lower Level Discriminator (LLD)	0.02 V (ccw)
Upper Level Discriminator (ULD)	10.5 (cw)
Digital Offset	all OFF

5.6 Spectroscopy Operation

Please refer to your MCA Operator's Manual for MCA operating directions.

Start MCA COLLECT with the ^{60}Co radioactive source previously placed near the detector. A spectrum should begin collecting on the MCA.

Note the % DT indicator. This 10-segment LED display shows the average dead time in increments of ten percent and will change proportionately with system count rate.

Adjust the Amplifier's COARSE GAIN so that the spectrum (data being displayed) is positioned conveniently on the display.

Use the Amplifier's SFG (Super Fine Gain) control when matching gains of several detectors or when establishing a specific gain (energy per channel). This control provides 100 times more resolution than the Fine Gain control.

5.7 PUR/LTC Operation

When selected, the 1510's PUR (PileUp Rejector) allows the ADC to convert only those detector signals resulting from single energy events. During the amplifier and ADC processing time, the Pileup Rejector inspects for pulse pileup and, when detected, initiates an ADC reject sequence, aborting the associated conversion process.

To compensate for dead time associated with rejected pulses and amplifier processing times, the Model 1510 generates a dead time signal which extends the collection time by the appropriate amount. The dead time signal is included in the MCA/ADC transfer signals and gates the MCA's live time clock.

The following instructions apply to obtain maximum performance when utilizing the Model 1510. Please refer to the operator's manuals regarding questions and use of the detector and MCA.

Connect the Model 1510 as shown in Figure 5.1 (the Counter is optional).

Set the 1510 Amplifier controls as follows:

COARSE GAIN 300
FINE GAIN 4.4
POLARITY . . . . . (+)
SHAPING . . . . . 4 µs

Set the 1510 ADC controls as follows:

GAIN . . . . . 8 K
RANGE . . . . . As required by MCA
OFFSET . . . . . Equal to the MCA's memory size
ULD . . . . . Fully clockwise (+10.5 V)

Set the 1510 HVPS voltage and polarity compatible with detector requirements (see Section 3.3).

5.8 Performance Adjustments

1. Monitor the 1510 amplifier output signal at the P/Z Insp test point and adjust the P/Z control (see Appendix D.1). The 122 keV ^{57}Co peak will be approximately 1.65 V in amplitude.
2. IMPORTANT! Remove all excitation sources from the vicinity of the detector.
3. Set the MCA to Collect.
4. Set the Model 1510 ADC'S LLD threshold just above the system noise level.
5. The following steps will optimize the discriminator sensitivity and insure that the discriminator threshold is set just above the noise level.
   a. Adjust the 1510 Amplifier PUR DISC control fully counterclockwise. The DISC LED indicator will continuously glow and the ADC's % Dead Time Indicator will show 100%.
   b. Adjust the PUR DISC control clockwise until the DISC LED indicator begins to blink.
   c. The PUR Discriminator Threshold is now properly set.
6. The % Dead Time Meter should now be at zero with only occasional flashing when a transient or spurious event is received.
7. IMPORTANT! If the Amplifier GAIN or SHAPING or the Detector or Preamplifier are changed, the PUR DISC control must be checked and possibly readjusted.

5.9 Incoming Count Rate (ICR)

With a nuclear counter connected to the 1510's rear panel ICR output, the average total input count rate can be monitored. The PUR must be set *on* and PUR Disc adjusted as in Section 5.8, step 5.

5.10 Pileup Rejection With a Live Source

1. Bring a source such as ^{57}Co near the detector. Adjust the source for an input count rate of approximately 50 kcps.
2. Set the MCA's memory to first half.
3. Set the MCA to Collect. Adjust the 1510's Amplifier gain to allow collection of the primary and sum peaks. If a gain adjust was necessary, readjust the PUR Disc as described in Section 5.8, step 5.
4. Set the MCA's preset to 60 Live seconds.
5. Disable Collect, clear Data, then re-enable Collect and accumulate a spectrum.
6. Set the MCA's memory to second half.

7. Accumulate a spectrum with the 1510 PUR ON/OFF switch *off*. Enable the MCA's Overlap function and compare the first half of the memory (PUR On) to that of the second half (PUR Off) (see Figure 5.2). Note the reduction in amplitude of both the sum peaks and the background. Also note the improved resolution of the sum peaks. The background reduction and improved resolution are directly indicative of the Pileup Rejector's capabilities, since only sum peak pulses which are indeed 100% in coincidence should be processed.

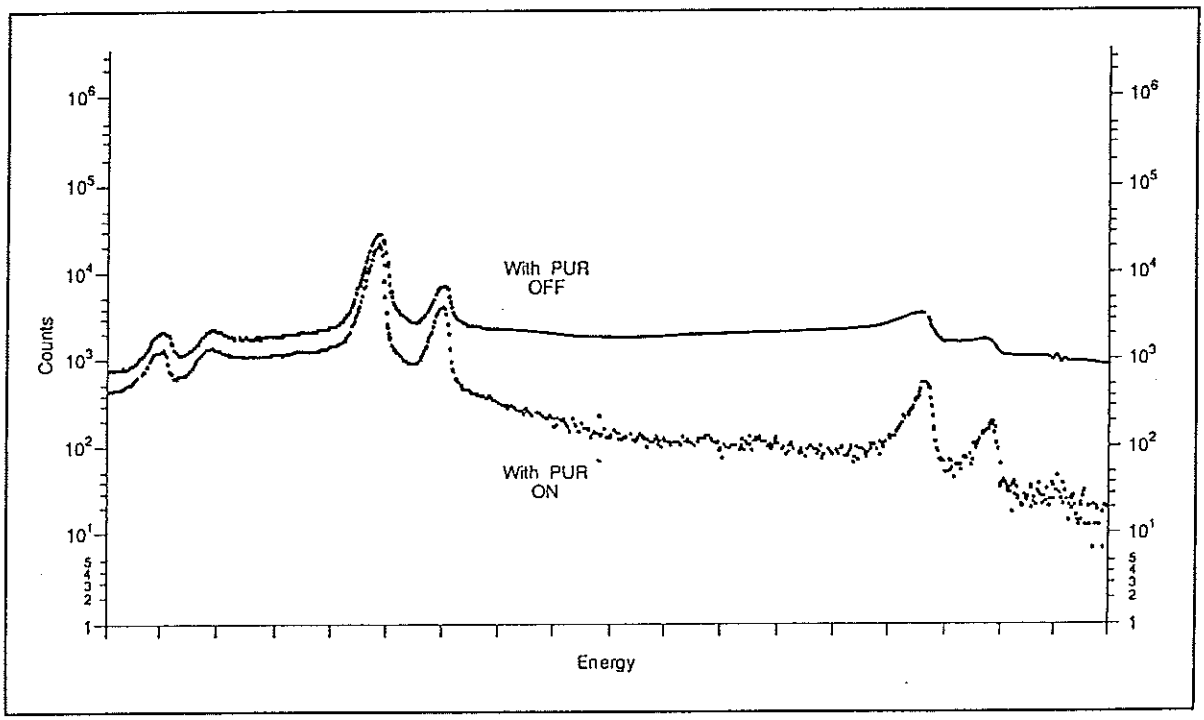

Figure 5.2 ^{60}Co Spectrum: PUR On vs. PUR Off

5.11 Live Time Correction With a Live Source

Live time correction (LTC) may vary and is dependent on factors such as ADC type, ADC calibration, spectrum energy distribution and detector characteristics such as geometry, size and ballistic deficit.

To achieve the highest performance of the Live Time Corrector, it may be necessary to adjust the LLD control.

The amplifier and ADC work together, forming an integral system when performing PUR/LTC. As a result, performance is very dependent on the ADC and in particular on the ADC's LLD setting.

Normally, the ADC's LLD control is set just above the system noise level. This is required so that the ADC and the amplifier's PUR discriminator operate over the same signal dynamic

range. Note that setting the ADC's LLD control too low can cause undercorrection and setting it too high can result in overcorrection.

The reference peak area deviation should remain under 5% for system dead times up to 50%. If you want to improve the results, adjust the LLD control slightly and repeat the test outlined in steps 3 through 8, below.

The following LTC optimizing process assumes that source *A* is ^{60}Co and source *B* is ^{137}Cs. The 1173.2 keV peak of ^{60}Co will be used as a reference. The upper peak, at 1332.5 keV, is not a good choice because a sum peak of ^{137}Cs at $2 \times 661.6 = 1323.2$ keV would interfere with the measurement.

1. Set up the equipment as indicated in Section 5.7.
2. Confirm performance adjustments indicated in Section 5.8.
3. Set the MCA's preset to 500 Live seconds.
4. Position radioactive source *A* near the Ge detector and adjust for an incoming count rate of 2 to 5 kcps. Once in place, the source should not be moved or altered in any way for the remainder of the experiment.
5. Collect a spectrum for 500 Live seconds.
6. To source *A*, add approximately 25 kcps of source *B* to make the total incoming rate 30 kcps.

   Note: Each time the background (source *B*) is changed, allow the detector to stabilize a few minutes before collecting the spectrum.

7. Collect a new spectrum for 500 Live seconds and record the net area of source *A*.
8. Compare the net area in steps 5 through 7 and compute the percentage change.
9. If you feel improvement is desirable, try adjusting the LLD control 1% or 2% higher. Repeat steps 4 through 8 until an optimum setting is achieved.
10. Set the PUR ON/OFF switch to *off*. Repeat steps 3 through 8.
11. Compare the deviation of source *A*'s spectrum when the PUR is *on* and the PUR is *off*.

Since the detector-source geometry was maintained and the preset Live Collection time was held constant, the ^{60}Co (1173.2 keV) net area can be used as a standard when comparing the effect of background (^{137}Cs) count rate.

With the PUR *off*, large changes will be observed in the reference net peak area as a function of count rate. With the pileup rejector set *on*, changes in the reference peak net area will be significantly reduced. The Live Time corrector extends the collection time, compensating for amplifier processing time and events rejected due to pileup.

CAUTION The 1510's PUR/LTC function is integral to both the internal amplifier and ADC. It is possible to use the 1510 with

an external amplifier or ADC, but in this case the 1510's PUR must be switched *off*, to prevent possible system malfunction.

5.12 ADC Gate

The GATE function allows the operator to enable or disable the ADC for acceptance and conversion of linear signals at its input. Depending on the criteria for the experiment in progress, the operator may use the GATE input in the factory-set Coincidence Mode or may change the function to the Anticoincidence Mode by moving a jumper on the ADC board (see Appendix C.5).

In order for the linear input signal to be considered by the ADC, it must be coincident in time with the GATE input signal.

A low logic level (0 to 0.8 V) at the GATE connector will disable the ADC. It will neither accept nor process any linear signals while the GATE is low.

A high logic level (2.5 to 5.5 V) at the GATE connector will enable the ADC. It will accept and convert all linear signals received while the GATE input is high.

If the GATE input is left open (unconnected), the ADC will act as if the GATE input is high and will accept and convert all linear signals received.

In the Anticoincidence mode, the logic is reversed. That is, a low logic level will enable the ADC and a high level (or an open input) will disable the ADC.

5.13 Sampled Voltage Analysis (SVA)

In the Sampled Voltage analysis (SVA) mode, analog voltages (dc or slowly changing ac voltages) can be sampled by the ADC, resulting in an amplitude distribution curve. The input signal must be between 20 mV and 10 V in amplitude and fall between the settings of the LLD and ULD controls to be considered.

The GATE input is used as the sampling signal, which must be coincident with the voltage to be sampled. Sampling occurs when the gate is high, conversion is initiated at the high to low transition.

The GATE sampling period or pulse width must be equal to or greater than 1 µs. However, for pulse inputs (rather than dc levels or slowly changing ac signals), the GATE input signal must be narrower than the input pulse width.

The sampling rate should be at least twice the frequency of the input signal for accurate sampling.

To use the Analyzer in the SVA mode, the factory set PHA/SVA jumper on the ADC board must be changed to the SVA position (see Appendix C.5). To return the Analyzer to the PHA mode, the jumper must be restored to the PHA position.

6. Circuit Description

This section describes the Model 1510 Integrated Signal Processor's circuits. Throughout the circuit description, please refer to the respective block diagrams.

6.1 Amplifier

Block Diagram – Sheet 4

The input signal is accepted by the rear panel BNC and cable assembly, is differentiated by C110 through C114 and resistor R192. Pole/zero compensation is performed by potentiometer RV3 and resistors R186 through R190. The time constants are selected by shaping switch S2A and S2B.

The differentiated signal is amplified by AMP1, AMP2, and AMP3 or by AMP1 and AMP3 only, depending on the COARSE GAIN switch (S1) selection. The output of AMP3 drives active filter integrators A70 and A68 and the PUR/LTC circuit.

The active filters produce complex pole pairs providing pulse shape and a sharp frequency cutoff characteristic for optimal signal to noise ratio. The time constants are selected by the shaping switch section S2C, S2D, S2E, S2F and associated resistors and capacitors.

The output of the second integrator drives the unipolar output amplifier A71; the unipolar AMP OUT signal is provided on the rear panel BNC connector J105. Baseline restoration is performed by A67 and associated circuits. For optimum performance the restorer is gated off during an event and the restorer threshold is automatically set. The restorer gate signal also provides a timing reference for the pileup rejector circuit.

6.1.1 Restorer

The baseline restorer uses a transconductance amplifier which develops a correction voltage at its output, is summed with the Unipolar Signal at A71, referencing the AMP OUT signal to 0 volts, maintaining the baseline.

The restorer symmetry is selectable using jumper plugs JA and JB. For the symmetrical restorer mode, positive and negative slew rates are equal. When asymmetrical is selected, the negative slew rate is reduced by a factor of 0.1, providing a softer restorer response for positive output signals.

6.1.2 Restorer Gate and Auto Threshold

The Auto threshold circuit peak-detects the negative noise excursions of the AMP OUT signal, generating a positive reference equal to the average value of the AMP OUT noise level. This automatic reference voltage, proportional to the AMP OUT noise level, enables precision restorer gating.

Baseline correction is prevented during AMP OUTPUT signal intervals. Comparators A64 and A65 monitor the AMP OUTPUT signal and disable the baseline restorer when the restorer threshold is exceeded.

6.2 Pileup Rejection

Block Diagram – Sheet 2

The Pileup Rejector (PUR) monitors the number of amplifier input events during a pulse processing sequence, which starts with an AMP IN signal and ends when the AMP OUT signal returns to the baseline. If two or more events occur during a processing sequence and the ADC is in the acquisition mode, Linear Gate (LG) is set true, the events are considered to be piled up and the pending ADC conversion is aborted.

The signal from gain amp A3 is shaped and discriminated from noise by the PUR discriminator. A fast timing pulse (system trigger) is produced for input signals that exceed the PUR DISC threshold.

The system trigger simultaneously clocks the Busy and Reject flip-flops. For the case of no pileup, only the Busy flip-flop will get set, since the "D" input of the Reject flip-flop was initially false. However if a subsequent AMP IN signal arrives before the conclusion of the processing sequence (pileup) the Reject flip-flop and REJECT signal will be set true. If the ADC is in the acquisition mode (LG true), a Reject will initiate an ADC reject sequence, the pending ADC conversion will be aborted and the events thrown away. At the conclusion of the processing sequence, the AMP OUT signal returns to the baseline and the training edge of the restorer gate signal clears the Busy and Reject flip-flops.

6.3 Live Time Correction

Block Diagram – Sheet 2

Live time correction is accomplished by extending the collection time (stopping the MCA live time clock) for the AMP OUT signal processing time, as determined by the busy and the Dead Time Extension (DTE) flip-flops, to allow replacement of events thrown away in the event of pileup.

Piled up events will produce multiple system triggers within the processing sequence. As before, the first trigger sets the Busy flip-flop, and the second trigger sets the Reject flip-flop. Reject is set true and the ADC aborts the conversion in process. The ADC Linear Gate (LG) ends prematurely and its positive transition clocks the DTE (Dead Time Extension) flip-flop true, adding a dead time component to the ADT signal via the OR gate.

When the AMP OUT signal returns to the baseline, the Busy and Reject flip-flops are cleared as before. However, the DTE flip-flop remains set and its Dead Time contribution continues.

For the next non-piled up processing sequence, the Reject flip-flop will not be set and the positive transition of the associated ADC LG signal will clock the DTE flip-flop reset, ending its dead time contribution. At the conclusion of the AMP OUT signal, the Busy flip-flop is cleared, ending its dead time component. When the sequence has ended, the ADT signal goes false and the MCA Live Time clock resumes.

6.4 Analog-To-Digital Converter (ADC)

Block Diagram – Sheet 3

The 1510 ADC is a Wilkinson-type ADC; the input signal is captured on a holding capacitor and discharged at a constant rate while counting clock pulses into a address register.

Prior to the acquisition mode, the ADC stretcher is normally active and will track and follow signals present at the input. If no conversions are in progress and the input signal threshold is exceeded, the Busy flip-flop will get set. Linear Gate (LG) is enabled, indicating the ADC is acquiring a signal and the stretcher will now peak-detect the corresponding input signal. When the input signal reduces to 90% of its peak value, and if the SCA and coincidence requirements are met, a conversion will be initiated. The start convert flip-flop is set, the Linear Gate (LG) closes, and the ADC conversion begins.

The precision ramp-down current source and counters are synchronously enabled. A binary counter, driven by a 100 MHz clock, is enabled for the duration of the ramp down sequence. When the stretcher voltage reaches the ADC "zero" reference, the ramp and counters are gated off, ending the conversion. The resultant digital address in the counter represents the magnitude of the ADC input.

The converted address is loaded into the tri-state bus drivers and DATA READY request is set, initiating data transfer.

In response to DATA READY, the MCA or computer sets ENABLE DATA true, which activates and enables the tri-state bus drivers allowing the ADC address to be presented on the data bus. At the conclusion of the Data Storage Cycle, DATA ACCEPTED is enabled clearing the DMA Ready flip-flop.

If the pulse was not within the LLD/ULD window, or if the GATE criterion was not met or REJECT was set, the stretcher ramp down sequence would have been aborted. The stretcher capacitor would be reset; that is, quickly discharged to prepare for a new input.

6.5 High Voltage Power Supply (HVPS)

Block Diagram – Sheet 1

The High Voltage Power Supply provides positive and negative 15 to 2000 volts and 30 to 5000 volts. The polarity and range are determined by the programming module which selects a half wave rectifier or voltage tripler network and the polarity orientation of the respective rectification/multiplier networks.

The dc/dc inverter runs at a natural frequency of approximately 30 kHz, determined by the primary's inductance and capacitance.

The output voltage is proportional to the inverter input control voltage provided by Integrator A78D. The output voltage is sampled, attenuated, fed back, and compared with a fraction of the reference voltage determined by A77 and the HV voltage control. Integrator A78D drives the dc/dc inverter until the output voltage matches the selected reference.

Current limiting is provided by comparators A79B and A79C. When a fault or overcurrent condition is sensed, the comparator output disables the dc/dc inverter input control voltage.

6.6 Low Voltage Power Supply (LVPS)

The Low Voltage Power Supply provides +5 V, ± 12 V and ± 24 V. It is a conventional linear supply using full wave rectifiers from an ac tapped transformer with capacitive input filters. Three-terminal regulators provide each of the regulated supply voltages. Each of the supplies is factory calibrated using potentiometers RV19 through RV23.

A. Specifications

A.1 Spectroscopy Amplifier

A.1.1 Inputs

AMP IN - Accepts positive or negative tail pulses from an associated preamplifier; amplitude ±10 V divided by the selected gain, ±12 V maximum; rise time: less than shaping time constant; decay time constant: 40 µs to ∞; Z_{in} = 750 Ω; rear panel BNC connector and 1.5 m (5 ft) cable assembly.

PUR INH - Receives a standard TTL logic signal from associated reset preamplifier; extends the Dead Time signal, inhibit and reset the pileup rejector during the preamplifier's reset cycle; positive true or negative true internally selectable; rear panel BNC connector.

A.1.2 Outputs

AMP OUT - Provides positive, linear, actively filtered, near-Gaussian shaped pulses; amplitude linear to + 10 V, 12 V max.; dc restored; output dc level factory calibrated to 0 ±5 mV; Z_{out} <1 Ω or = 93 Ω internally selectable; short circuit protected; rear panel BNC connector.

ICR (Incoming Count Rate) - Provides a standard TTL logic signal; frequency corresponds to input count rate; positive true; width = 150 ns, Z_{out} = 50 Ω; rear panel BNC connector.

A.1.3 Front Panel Controls

COARSE GAIN - Six-position rotary switch selects factors of X20, X50, X100, X200, X500 and X1000.

FINE GAIN - Ten-turn locking dial precision potentiometer selects variable gain factor of X0.5 to X1.5; resettability ≤0.03%.

SFG (super fine gain) - Multi-turn screwdriver potentiometer selects gain with an adjustment resolution of better than 1 in 16 000 (0.0063%).

POLARITY - Two-position toggle switch sets the amplifier for the polarity of the incoming preamplifier signal.

P/Z - Multi-turn screwdriver-adjustable pole/zero potentiometer optimizes amplifier baseline recovery and overload performance for the preamplifier's fall time constant and the amplifier's chosen shaping time; range: 40 µs to ∞.

P/Z INSP - Momentary pushbutton switch clamps the AMP OUT signal viewed on the test point to approximately ±300 mV, minimizing scope overload for precise pole/zero adjustment.

SHAPING - Six-position rotary switch; providing 0.5, 1, 2, 4, 8 and 12 µs shaping time constants.

PUR ON/OFF - Two-position toggle switch enables (ON) or disables (OFF) the pileup rejector and live-time corrector.

PUR DISC - Multi-turn screwdriver adjustable potentiometer optimizes the pile-up rejector discriminator threshold level; provides a variable range of 0 to 500 mV; LED indicator aids in setting the threshold.

A.1.4 Internal Controls

INH/-INH - Jumper plug selects PUR INH polarity compatibility; factory set for positive true logic.

ASYM-SYM - Jumper plug selects ASYMmetrical or SYMmetrical baseline restorer modes; factory set to SYMmetrical.

AMP Z_{OUT} - Jumper plug provides Z_{out} <1 Ω or ≈ 93 Ω; factory set for <1 Ω.

A.1.5 Performance

Amplifier

GAIN RANGE - Continuously variable from X10 to X1500.

OPERATING TEMPERATURE - 0 to 33 °C.

GAIN DRIFT - ≤±0.0075%/°C, after a 30 minute warm-up.

DC LEVEL DRIFT - ≤±10 µV/°C, after a 30 minute warm-up.

INTEGRAL NON-LINEARITY - ≤±0.05%, over total output range for 2 µs shaping.

OVERLOAD RECOVERY - Recovers to within ±2% of full scale output from X1000 overload in 2.5 non-overloaded pulse widths, at full gain, any shaping time constant, with pole-zero cancellation properly set.

NOISE CONTRIBUTION - ≤4.0 µV true rms referred to input, 2 µs shaping, and amplifier gain ≥100.

PULSE SHAPING - Near-Gaussian shape: one differentiator, two active filter integrators; time to peak: 2.35X shaping time; pulse width: 7.3X shaping time; time to peak and pulse width measured at 0.1% of full scale output.

RESTORER - Active gated.

UNIPOLAR COUNT RATE STABILITY - For 2 µs shaping, the FWHM of a ^{60}Co 1.33 MeV gamma peak for an incoming rate of 2 kcps to 100 kcps and 9 V pulse height will typically change less than 14%; the peak position will typically shift less than 0.024%.

Note: These results may not be reproducible if the associated detector exhibits an inordinate amount of long rise time signals.

Pileup Rejector/Live Time Corrector

PULSE PAIR RESOLUTION - <500 ns.

MINIMUM DETECTABLE SIGNAL - Limited by detector/preamp noise characteristics.

A.2 100 MHz ADC

A.2.1 Inputs

ADC IN - Accepts positive unipolar or bipolar (positive lobe leading) pulses; amplitude 0 to + 10 V, + 12 V maximum; rise time 0.25 to 100 µs maximum; width 0.5 µs minimum; Z_{in} = 1 kΩ; direct coupled; rear panel BNC.

ADC GATE - Internal jumper plugs provided for selecting Coincidence/Anti-coincidence and PHA/SVA. PHA Mode: With Coincidence (Anti-coincidence) selected, a positive (negative) TTL level during the time-to-peak interval will enable conversion and storage of pulse, logic low (high) level will cause pulse to be rejected. Sampled Voltage Analysis (SVA) Mode: GATE IN used as a sampling signal; accepts positive TTL logic pulse or dc level; SVA pulse width ≥1 µs; Coincidence/SVA loading: 4.7 kΩ pull-up resistor to + 5 V; rear panel BNC connector.

A.2.2 Outputs

DATA - Provides 13 binary TTL-compatible output lines and the data transfer commands required for MCA interface; rear panel 25-pin D-type connector. Data Lines are negative true unless specified for positive true.

A.2.3 Front Panel Controls

GAIN - Six-position rotary switch selects full scale resolution of input signal; selection of 256, 512, 1K, 2K, 4, or 8K channels for a 10 V input pulse.

RANGE - Six-position rotary switch selects 256, 512, 1024, 2048, 4096 or 8192 channels as the overflow limit.

OFFSET - Six DIP switches to provide suppression of the digital zero; 0 to 8064 channels in multiples of 128 channels.

LLD - Ten-turn locking-dial precision potentiometer sets the Lower Level Discriminator for minimum input acceptance voltage; range 0.02 to + 10 V dc.

ULD - Screwdriver adjusted multi-turn potentiometer sets the Upper Level Discriminator for maximum input acceptance voltage; range 0.02 to + 10.5 V dc.

ZERO - Screwdriver adjusted multi-turn potentiometer sets the ADC's analog zero intercept level; range ±5% of input range; resolution 0.005% of full scale.

A.2.4 Internal Controls

DATA BUFFER ENABLE/DISABLE - Jumper plug to enable or disable data buffer; factory set to enable.

ENABLE CONVERTER POS/NEG - Factory set to the ordered configuration.

SVA/PHA - Jumper plug selects PHA or SVA; factory set to PHA.

COIN/ANTI - Jumper plug selects coincidence or anti-coincidence gating for PHA mode; factory set to coincidence.

Four jumper plugs selects the polarity of the MCA transfer commands:

DT POS/NEG - Factory set to the ordered configuration.

READY POS/NEG - Factory set to negative true.

DATA ACCEPTED POS/NEG - Factory set to negative true.

ENABLE DATA POS/NEG - Factory set to negative true.

A.2.5 Indicators

%DT - Ten-segment LED indicator displays the average dead time of the converter.

A.2.6 Performance

INTEGRAL NON-LINEARITY - <±0.025% of full scale over the top 99.5% of range including effects from tilt.

DIFFERENTIAL NON-LINEARITY - <±0.7% over the top 99.5% of range.

DRIFT, GAIN - <±0.009% of full scale/°C, after a 60 minute warm-up.

DRIFT, ZERO - <±0.0025% of full scale/°C, after a 60 minute warm-up.

DRIFT, LONG TERM - <±0.005% of full scale per 24 hours at a constant temperature.

PEAK SHIFT - <±0.025% of full scale at rates up to 50 kHz.

ADC DEAD TIME - Linear Gate Time + Conversion Time + Memory Cycle Time.

CONVERSION TIME - 1.5 µs + 0.01 (N + X) µs where N = Address Count, and X = effective digital offset.

CHANNEL PROFILE - Typically flat over 90% of channel width.

A.3 High Voltage Bias Supply

A.3.1 Inputs

HVPS INH - Logic low inhibits and gates off the output high voltage; maximum logic low ≤0.7 V at ≤1.3 mA: Open circuit or logic high ≥6 V resumes normal operation; sourcing: 12 V through 10 kΩ; maximum input + 12 V; rear panel BNC.

A.3.2 Outputs

HVPS OUT - Dual range, 30 V dc to 5000 V dc at 300 µA or 15 V dc to 2000 V dc at 1 mA, rear panel PROGRAM module selectable, continuously variable; one rear panel SHV connector.

A.3.3 Controls

ON/OFF - Front panel 2-position toggle switch enables or disables output.

OUTPUT VOLTAGE - Front panel 10-turn direct readout dial permits continuous adjustment of the output voltage.

POLARITY - Positive or negative, rear panel PROGRAM module selectable.

A.3.4 Indicators

OUTPUT VOLTAGE - Ten-segment LED indicator displays voltage in increments of 600 V.

POLARITY - LEDs indicate polarity selected and operate with high voltage ON or OFF providing a polarity preview when the 1510 is energized.

INH (INHIBIT) - LED provides visual indication of the INHIBIT status.

A.3.5 Performance

RIPPLE AND NOISE - ≤5 mV peak to peak.

OUTPUT STABILITY - Long term drift of output voltage is ≤0.01%/hr. and ≤0.02%/8 hr. at constant input line voltage, load, and ambient temperature after a 60 minute warm up.

TEMPERATURE COEFFICIENT - ≤±50 ppm/°C after 30 minute warm up, operating range 0 to 33 °C.

REGULATION - ≤0.001% variation in output voltages for line and load changes within the operating range at constant ambient temperature.

OVERLOAD PROTECTION - Power supply will withstand any overload, including a short circuit for an indefinite period, and will resume normal operation when the excessive load is removed.

OUTPUT LOAD CAPACITY - 0 to 300 µA on 5 kV range and 0 to 1 mA on 2 kV range.

DIAL ACCURACY - <±1% of full scale (5 kV).

CURRENT LIMIT - 5 kV range: ±450 µA; 2 kV range: ±1.3 mA.

A.4 System Rear Panel Connectors

With the exception of the ADC data, preamp power and high voltage connectors, all signal connectors are BNC type.

DATA - 25-pin D-type female.

PREAMP POWER - 9-pin D-type female.

HVPS OUT - SHV (Isolated from chassis ground by 470 Ω).

A.5 Standard Accessories

C123-5 - SHV to SHV; RG 59/U, 75 Ω, 1.5 m (5 ft) cable; one included with 1510.

C120-5 - BNC to BNC; RG 62/U, 93 Ω, 1.5 m (5 ft) cable; two included with 1510.

C120-.5 - BNC to BNC; RG 62/U, 93 Ω, 15 cm (0.5 ft) cable; one included with 1510.

A22540 - Rack mount hardware, included with 1510.

A22541 - Preamp power extension; 9-pin D-type connectors; 1.5 m (5 ft) cable, included with 1510.

CA141 - BNC female/female barrel connector; included with the 1510.

45112512 - SHV male/male barrel connector; included with the 1510.

A.6 Interface Cables

One of the following 1510/MCA interface cables is provided with the 1510 model ordered.

C1547-4 - Ribbon cable; mates the 1510-01 with the Series 35, Series 35 Plus, Series 40, Series 80, Series 85, Series 88, Series 90, Series 95 and System 100 MCAs; 25-pin D-type connectors; 1.2 m (4.0 ft) cable.

C1554 - Ribbon cable; mates the 1510-03 with the 556 AIM; 25-pin D-type connector on the 1510 end and a 34-pin D-type connector on the AIM end; 1.2 m (4.0 ft).

C1556 - Ribbon cable; mates the 1510-02 with the AccuSpec/B and AccuSpec/MC; 25-pin D-type connector on the 1510 end and a 37-pin D-type connector on the AccuSpec end; 1.2 m (4.0 ft).

A.7 Optional Cable

C1545A - Shielded ADC/MCA interface ribbon cable, 3.0 m (10 ft). Used in place of the supplied C1547-4 ribbon cable.

A.8 Physical

SIZE - 4.45 X 42.5 X 39.1 cm high, wide, deep (1.75 X 16.75 X 15.38 in.)

WEIGHT - 5.0 kg (11 lb).

SHIPPING WEIGHT - 7.3 kg (16 lb).

AC POWER - 90 to 110 V, 105 to 125 V, 195 to 235 V, and 210 to 250 V. Rear panel jumper plug selectable; 50 to 60 Hz, approximately 40 W.

PREAMP POWER - Provides ±24 V, ±12 V (±2%) and ground for standard preamplifiers; 50 mA current on each line; rear panel 9-pin D-type connector.

OPERATING TEMPERATURE - 0 to 33 °C.

HUMIDITY - 0 to 80%, non-condensing.

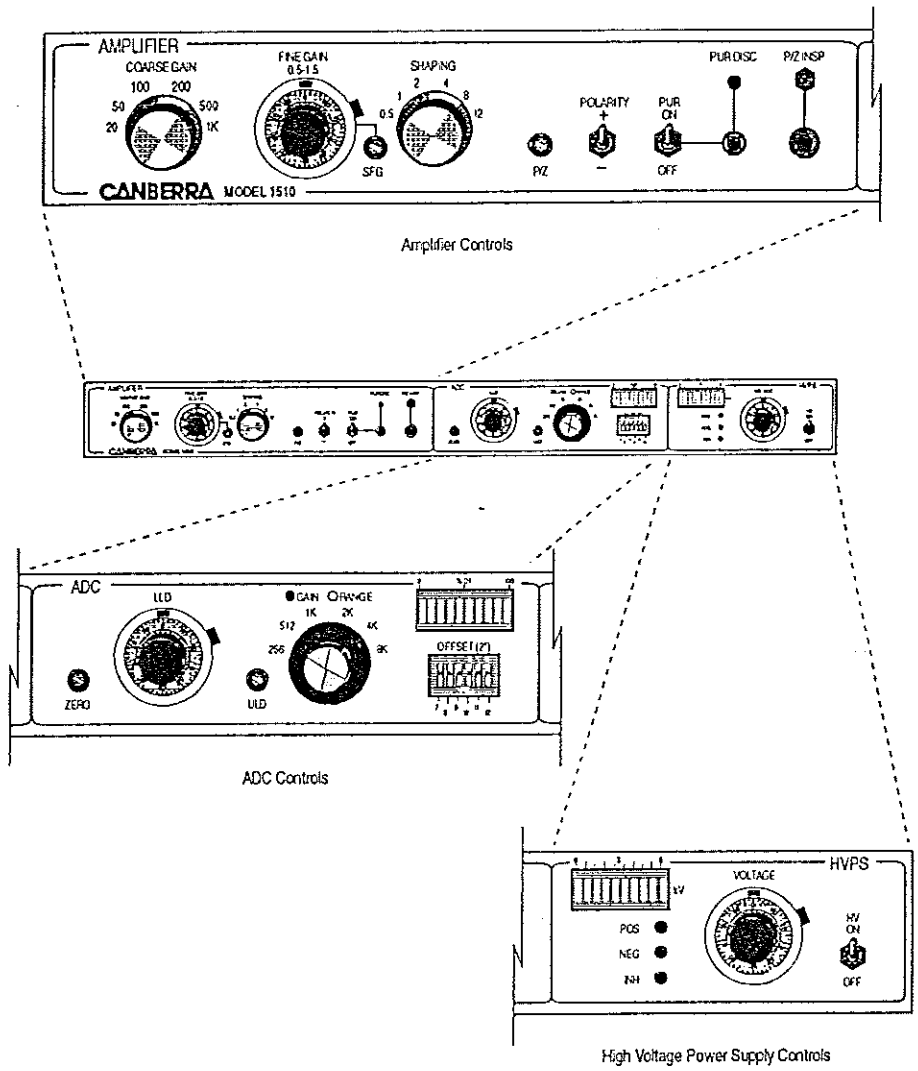

Figure A.1 Front Panel Controls
(see Sections A.1, A.2 and A.3)

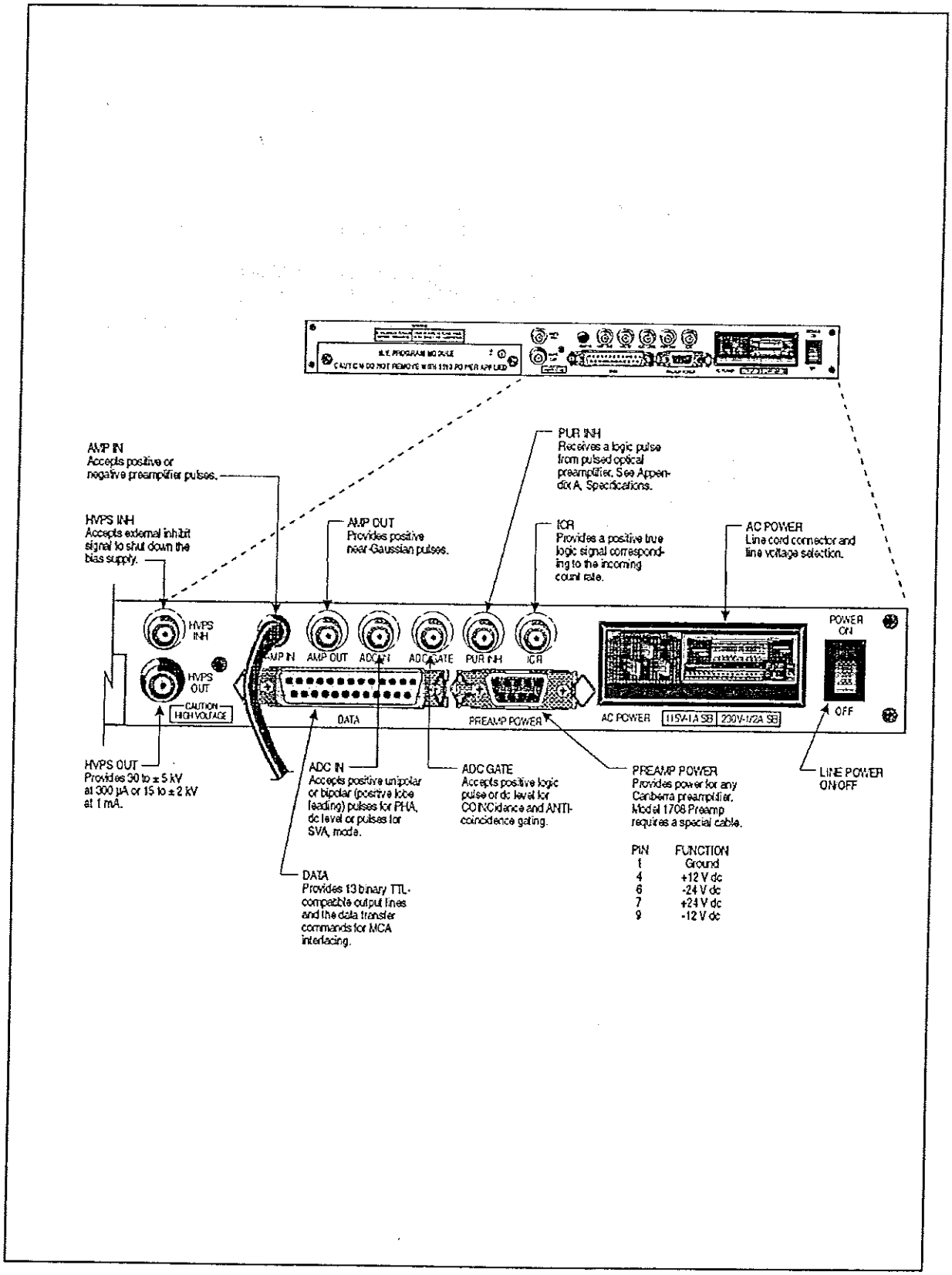

Figure A.2 Rear Panel Connectors

B. High Voltage Polarity/Range Module

WARNING **This unit produces hazardous voltages. Turn the 1510's ac power and High Voltage *off* before changing the programming module.**

To change the Polarity or the Voltage Range, loosen the screws at each end of the programming module on the 1510's rear panel and remove the module from the unit.

Note Handle the module's PC board only by the edges. Touching the board's surfaces may contaminate them with skin oil and dirt, causing performance degradation. If you suspect the PC board is contaminated, swab it with denatured alcohol.

B.1 Polarity

To check the HVPS polarity, look at the HVPS module plate. The selected polarity ("+" or "–") is visible through the observation hole in one corner of the plate (Figure B.1). The 1510 is factory set for "+" polarity.

To change the polarity, remove the programming module, turn it around and reinstall it. The "–" polarity sign should now be visible in the observation hole.

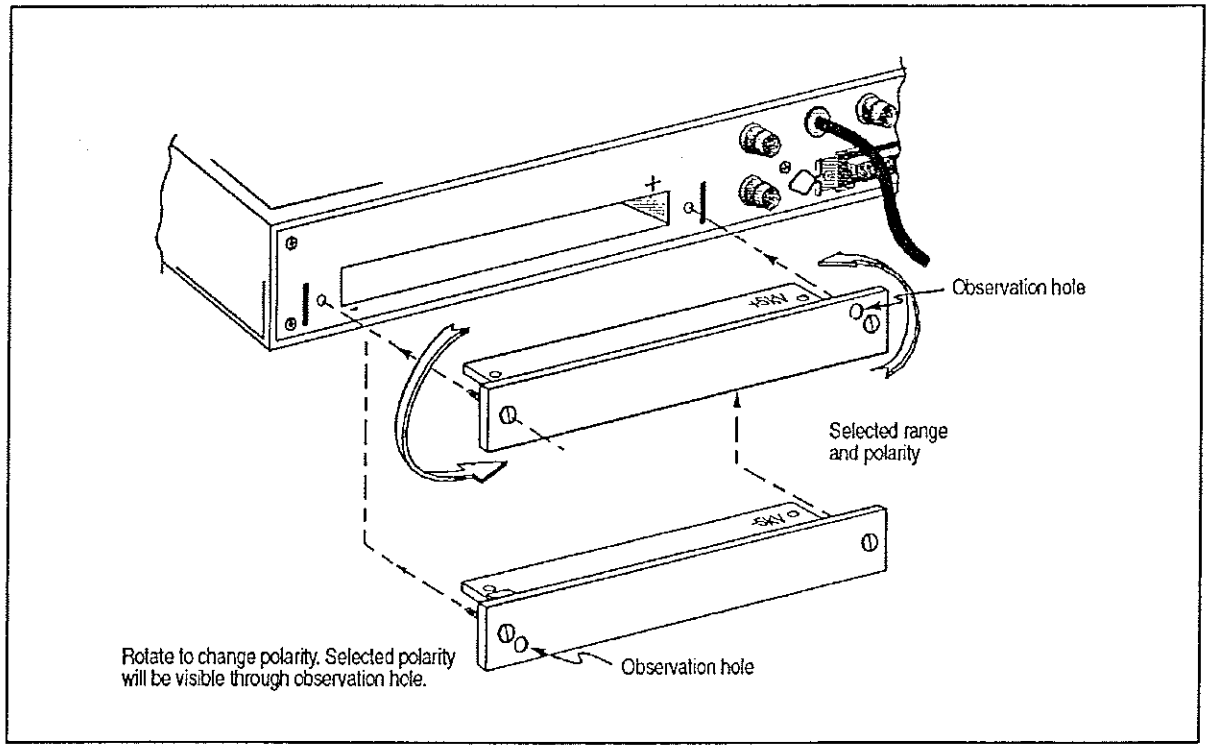

Figure B.1 HVPS Programming Module Removal and Installation

B.2 Voltage Range

The 1510 is set for the 5 kV range. To change the output to the 2 kV range for sodium iodide detectors, remove the programming module from the 1510 (see Figure B.1). Remove the two nylon screws securing the PC board to the bracket, reverse the board, replace the screws and reinstall the reassembled programming module.

Note: The PC board must be installed on the bracket center line, otherwise mounting screw alignment is not possible. This was done intentionally as a safeguard to insure proper installation.

When attached to the bracket, the selected range will be indicated on the upper right edge of the PC board when positioned for installation in the 1510 (see Figures B.1 and B.2).

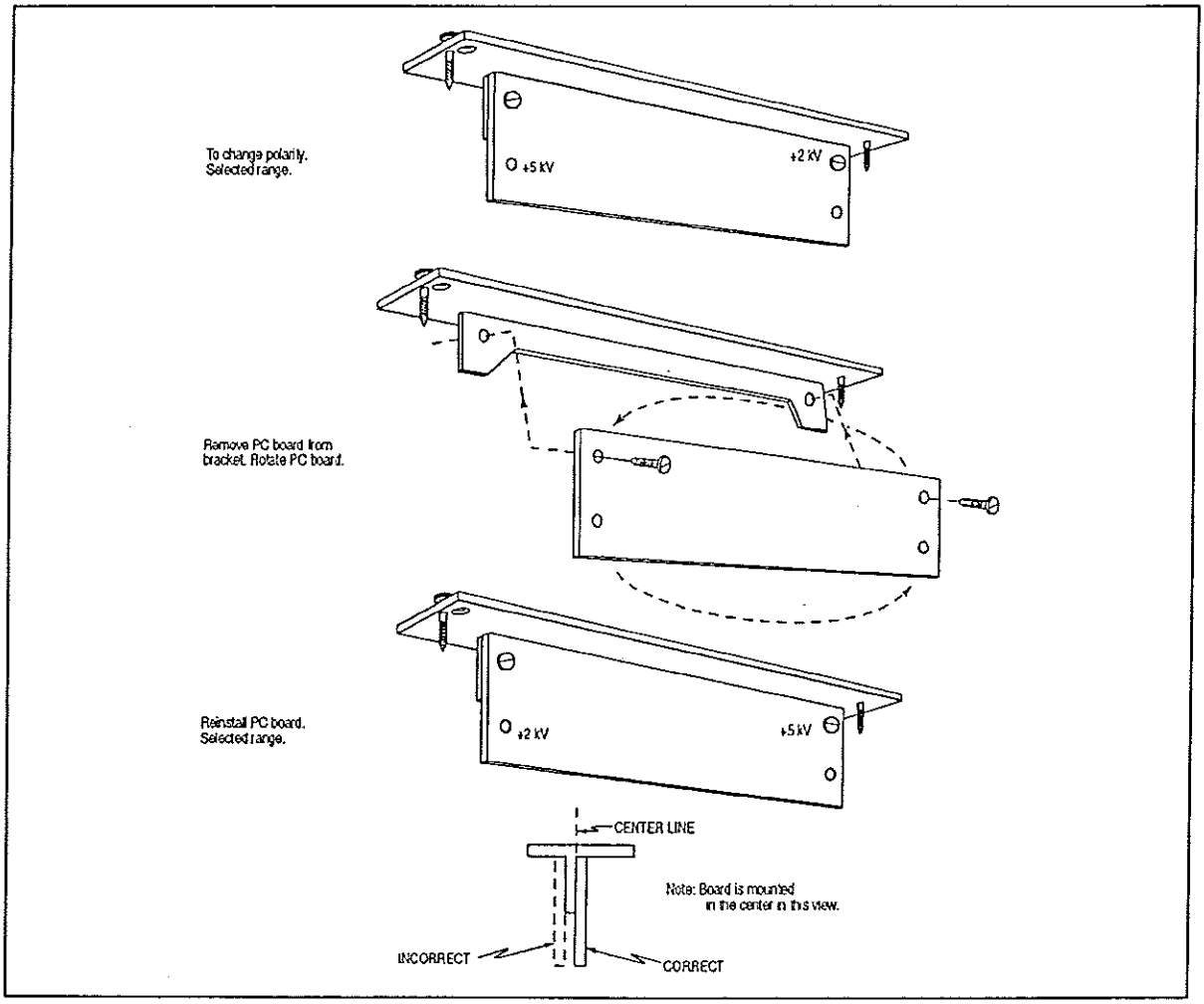

Figure B.2 Board Orientation

C. Internal Controls and Connectors

WARNING **Hazardous voltages are present inside the 1510. Turn off the unit and remove the line cord before servicing the unit.**

C.1 Operating Voltage Selection

To change the operating voltage of the 1510, move the plastic fuse shield, next to the ac line cord socket, to one side. The voltage selection board is located just below the fuse. The operating voltage that the 1510 is set for will be visible on the card.

To change between 120 and 240 V or to change to low-line voltage (100 or 220 V), pull the selector card out of its socket and replace it so that the desired voltage is visible beneath the fuse, as shown in Figure C.1. A pair of needle-nose pliers will be useful here.

Be sure to change the fuse when changing the operating voltage. Use a 1 A slow blow fuse for 95-125 V. Use a ¼ A slow blow fuse for 195-250 V.

C.2 Case Removal

To change jumpers, you'll have to remove the 1510 from its case.

1. Before attempting to remove the case, turn off the ac power and remove the ac line cord from the rear of the 1510.

2. Remove the following knobs:

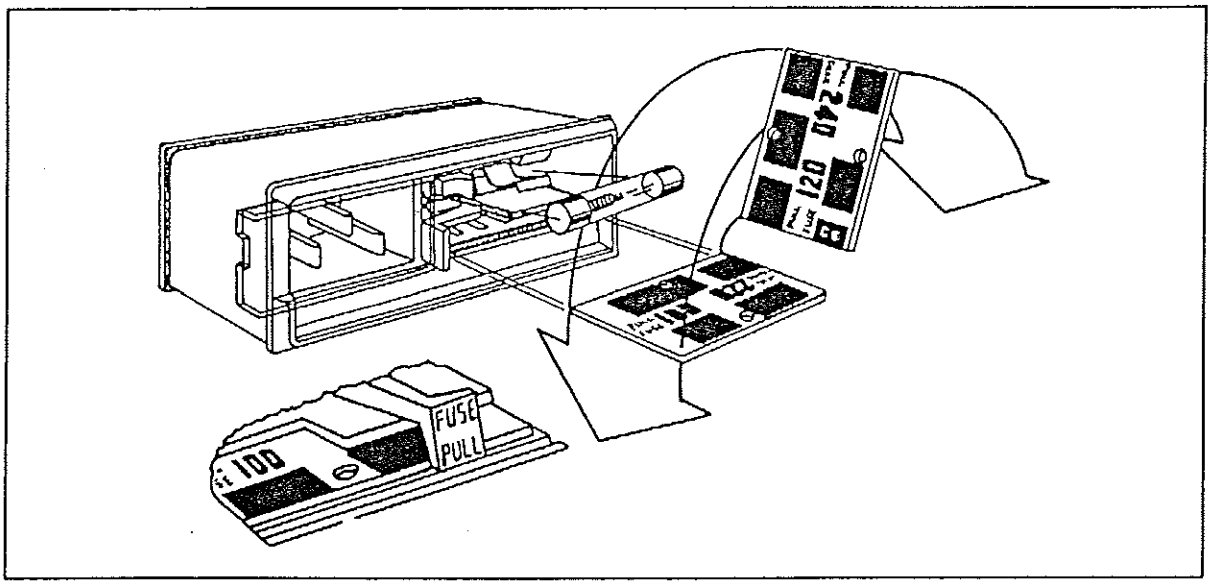

Figure C.1 Voltage Selection

Amplifier Coarse Gain
Amplifier Shaping
ADC Gain/Range knob set

3. Remove the two case securing screws located at the top of the case (see Figure C.2).
4. On the 1510 front panel, align the duo-dial locking tabs with the corresponding cut-outs or slots in the front panel.
5. Begin pushing the 1510 out of the case, to the rear, by pressing firmly on the knobs. The knobs may need to be jiggled slightly.
6. With the 1510 slightly out, grasp the rear panel and heat sink and gently pull the 1510 from its case.
7. To reassemble, perform the steps in the reverse order.

   Note: Align the front panel duo-dial locking tabs with the corresponding slots or cutouts provided in the front panel.

   With the knobs part way through the front panel, the knobs may need to be jiggled slightly to achieve complete insertion. The two bar-graph displays should protrude slightly through the front panel with proper reassembly.

8. Reinstall the two case securing screws (see Figure C.2).

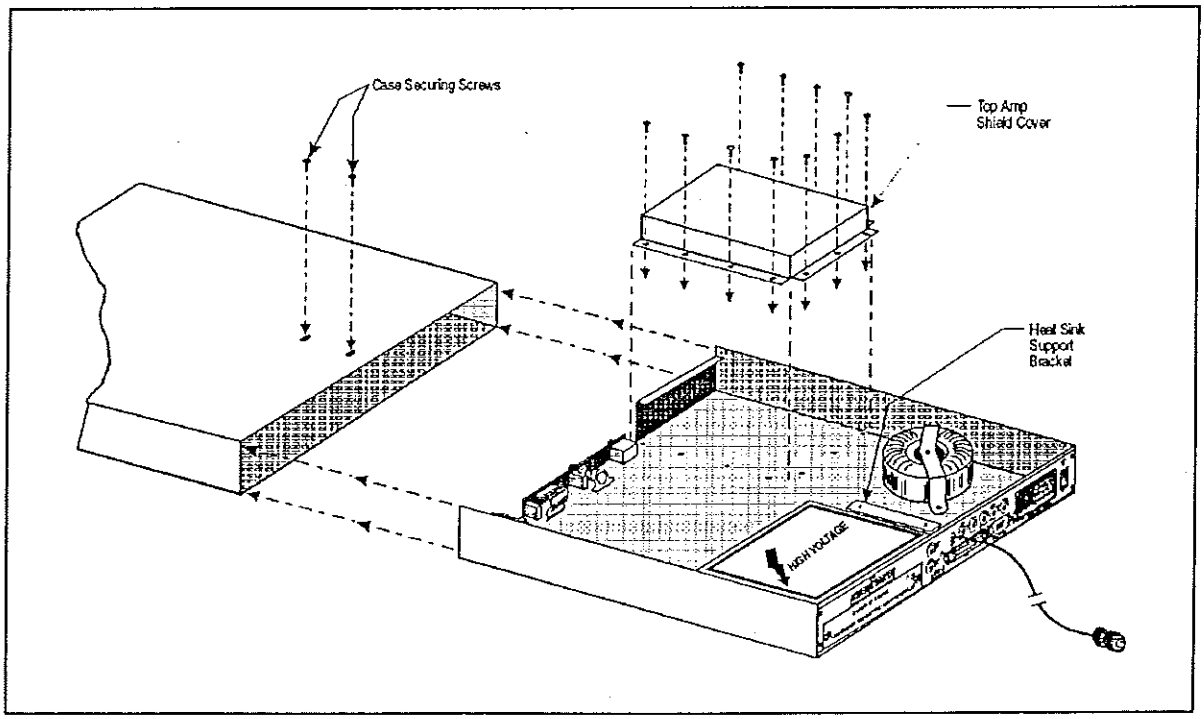

Figure C.2 Top Shield Cover Removal

C.3 Amplifier Top Shield Removal

1. Remove the 1510 from the case as outlined in Appendix C.2.
2. Remove the 14 screws and lock washers securing the amplifier top shield (see Figure C.2). Leave the bottom cover in place.
3. To reassemble, perform the steps in the reverse order.

Note: The bottom cover and top cover form an integral RF/EMI shield when assembled. It is important that *all* the securing screws be replaced and uniformly tightened.

C.4 Amplifier Internal Jumpers

Internal jumpers have been provided allowing for performance optimization for a specific application. The jumper plugs have been factory set for optimal performance for general applications (see Figure C.3).

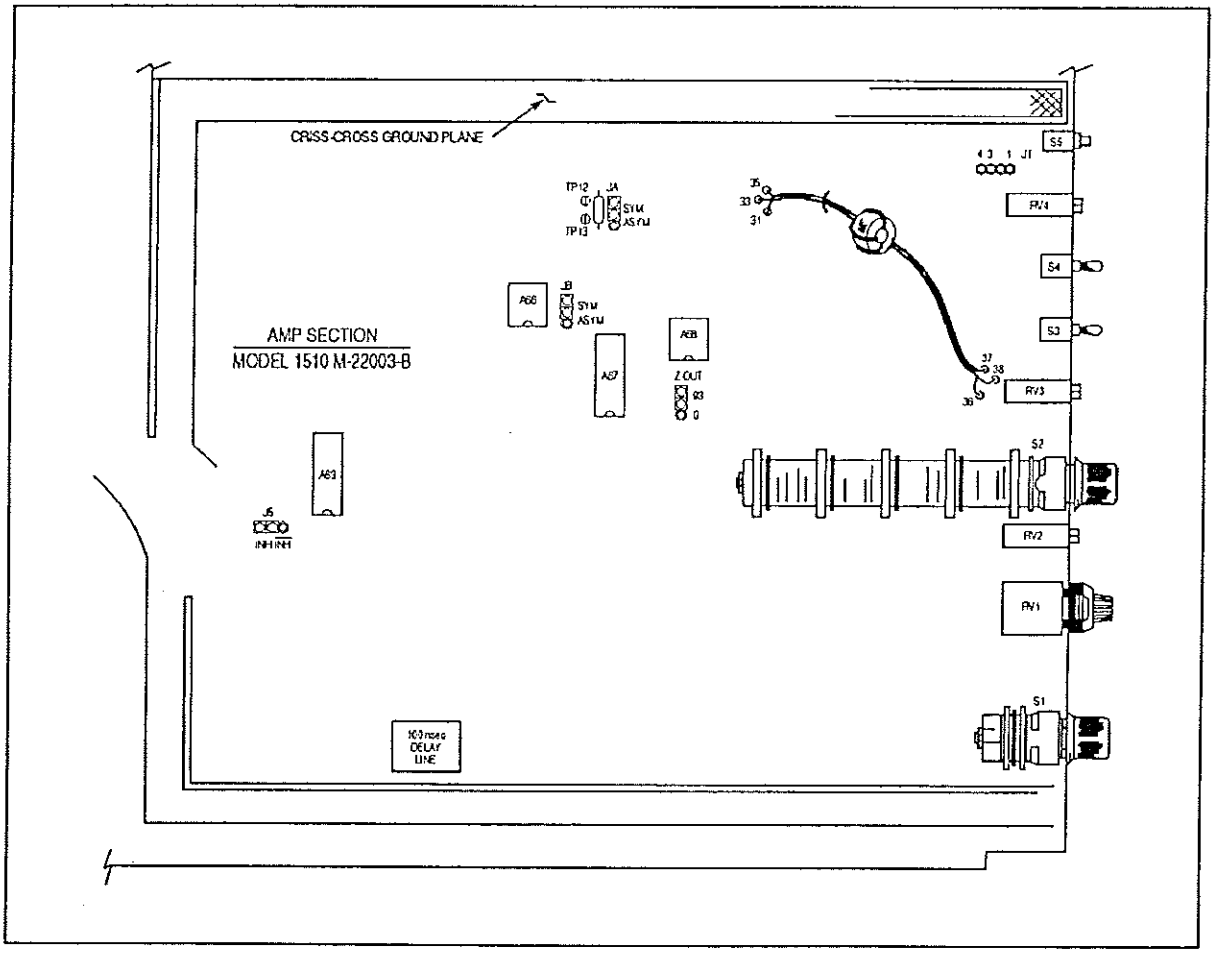

Figure C.3 Amplifier Internal Jumpers

C.4.1 Z-out

The output impedance of the 1510's AMP OUT connector can be changed from the factory setting of ≤ 1 ohm to approximately 93 ohms.

When using the 1510 Amp and ADC as an integral system, they are normally connected using a short length of RG-62 coax cable. However, if the AMP OUT signal drives a long coax cable, perhaps to an external ADC or an oscilloscope, oscillation could develop.

With the Z_{out} jumper plug set for 93 ohms, up to a few hundred feet of coax cable may be safely used. If oscillation is still present, the cable length should be terminated at the receiving end with 93 ohms. Note, however, that the 93 ohm output impedance is in series with the termination impedance and a decrease in the total signal range will occur. For example, the signal amplitude will be reduced by 50% if both Z_{out} and the load terminations equal to 93 ohms.

C.4.2 JA, JB, SYM-ASYM

The baseline restorer in the 1510 amplifier is flexible in that both Symmetrical and Asymmetrical Modes are offered. For the Symmetrical Mode, the restoration currents are identical above and below the baseline. With Asymmetrical Mode selected, the restoration current above the baseline (referenced to a positive output signal) is much less than that below the baseline.

For general purpose applications, the 1510 is shipped set for the Symmetrical Mode, which is much more tolerant of detector systems exhibiting baseline discontinuities resulting from excessive noise, high voltage effects, microphonics and secondary time constants. For an exceptional detector and good laboratory environment, you may want to consider using the Asymmetrical Mode for slightly better resolution performance.

Note: Whichever baseline restorer mode you choose, jumper plugs JA and JB must *both* be set the same!

C.4.3 J5, INH-INH/

Jumper plug J5 is used to change the sense of the pileup rejector INHibit signal. With INH selected, a logic "1" initiates an inhibit and with INH/ selected a logic "0" initiates the inhibit. Factory set to INH (positive true). For more details, please refer to Appendix A.1.1, Amplifier Input Specifications.

C.5 ADC Internal Jumpers

The ADC jumper plugs have been factory preset, allowing compatibility with all Canberra MCAs. For other MCAs and special applications, please consult the user manual for the intended instrument's requirements. See Figure C.4 for jumper plug locations.

C.5.1 J2, Dead Time Polarity

Sets the polarity of the dead time MCA transfer signal, pin 21 of the ADC Data Connector. Shipped in the POSitive position for the 1510-01 and the negative position for the 1510-02 and 1510-03.

C.5.2 J8, Enable Data

Sets the polarity of the ENABLE DATA signal on pin 22 of the ADC Data Connector. Shipped in the NEGative true (enable) position.

C.5.3 J9, Data Buffer

Enables (B) or disables (B/) the ADC Data Buffer. Shipped in the enabled (B) position. For details, please refer to Appendix F, ADC Interfacing and Data Transfer.

C.5.4 J10, Data Accepted

Sets the polarity of the DATA ACCEPTED signal on pin 17 of the ADC Data Connector. Shipped in the NEGative true (enable) position.

C.5.5 J11, Data Ready

Sets the polarity of the DATA READY signal on pin 14 of the ADC Data Connector. Shipped in the NEGative true (enable) position.

C.5.6 J12, PHA/SVA

Sets the ADC's conversion mode for either Pulse Height Analysis (PHA) or Sampled Voltage Analysis (SVA). Shipped in the PHA mode.

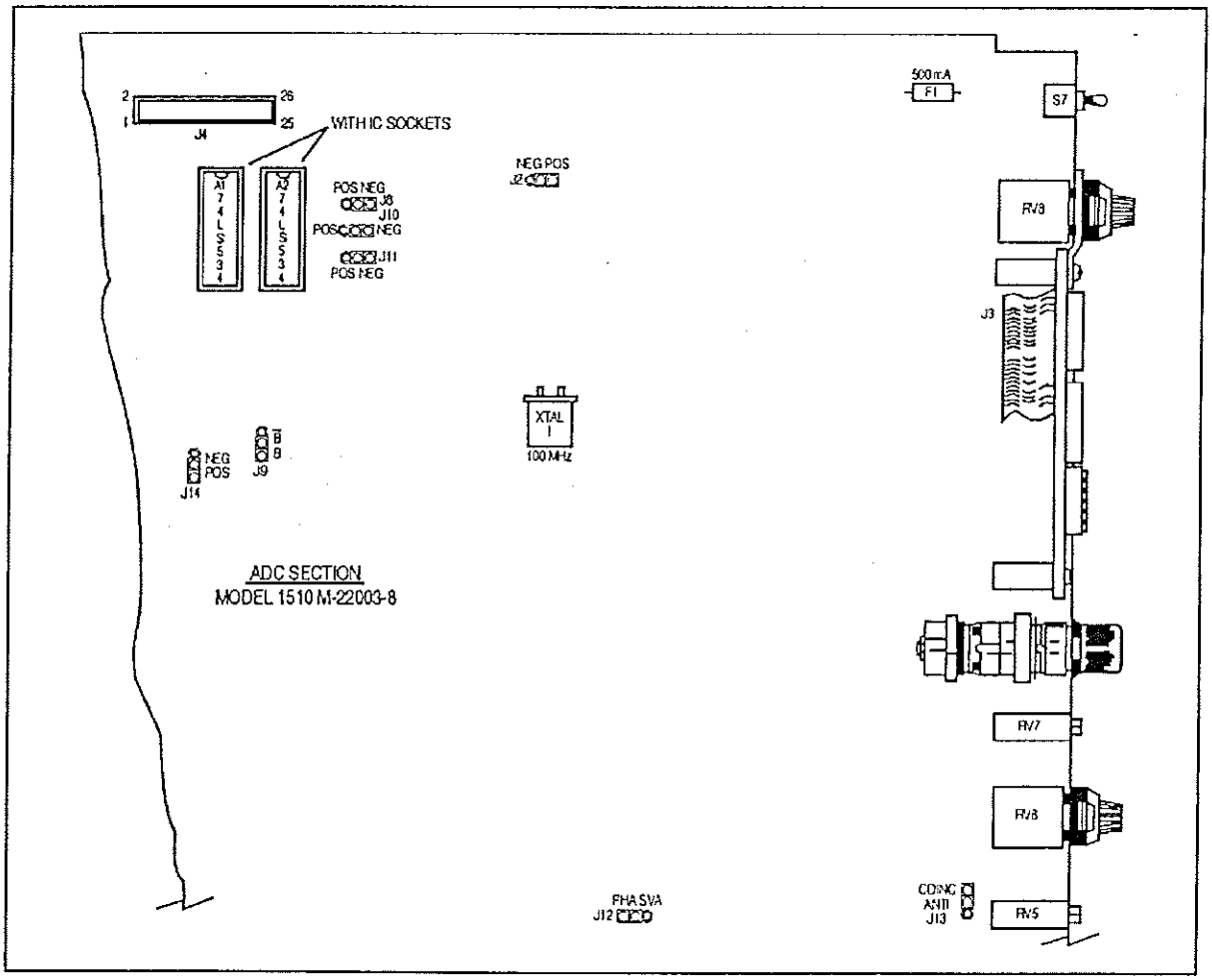

Figure C.4 ADC Internal Jumpers

C.5.7 J13, Coinc/Anti

Sets the ADC's Gate Input mode for COINCidence or ANTIcoincidence. Shipped in the COINC mode.

C.5.8 J14, Enable Converter

Set the Enable Converter signal's polarity (on pin 18 of the ADC Data Connector). Shipped in the POSitive true position for the 1510-01 and the NEGative true position for the 1510-02 and 1510-03. For more details, please refer to Appendix F, ADC Interfacing and Data Transfer.

C.6 ADC Setup Diagrams

Block Diagrams C.5, C.6, and C.7 illustrate the ADC setup and ADC/MCA interfaces for the different 1510 model options. Your Model 1510 will have been configured at the factory for proper operation, it will not be necessary to change the jumper settings unless your needs were not anticipated by the standard setup.

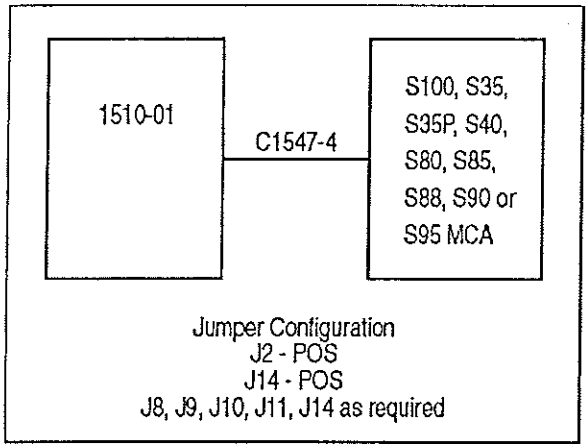

Figure C.5 Model 1510-01 and Various MCAs

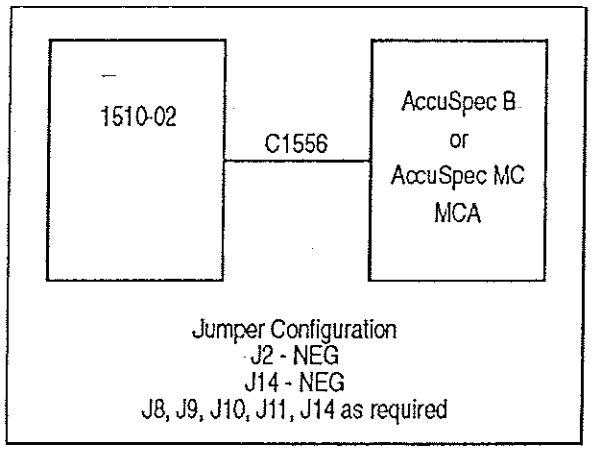

Figure C.6 Model 1510-02 and AccuSpec/B or AccuSpec/MC

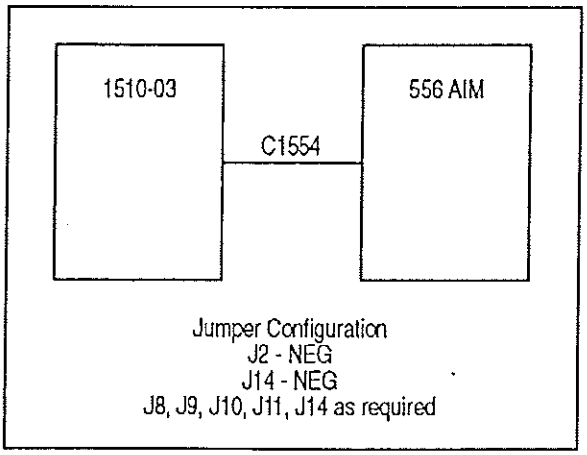

Figure C.7 Model 1510-03 and Model 556 AIM

D. Performance Adjustments

D.1 Amplifier Pole/Zero (P/Z)

At high count rates, the P/Z adjustment is extremely critical for maintaining good resolution and low peak shift. For a precise and optimum setting of the P/Z, a scope vertical sensitivity of 50 mV/div should be used.

However, most scopes will overload for a 10 V input signal when the vertical sensitivity is set for 50 mV/div. Overloading the scope input will distort the signals' recovery to the baseline. Thus, the P/Z will be incorrectly adjusted resulting in a loss of resolution at high count rates.

To prevent scope overloading, the clamping circuit provided in the 1510 should be used. Monitor the AMP OUT signal at the 1510's front panel P/Z INSP test point using an oscilloscope and suitable scope probe. Ground the scope probe to the nearby PUR or POLARITY switch body.

When performing the following P/Z adjustments, set the scope vertical sensitivity to 50 mV/div and hold down the P/Z INSP switch. The AMP OUT signal will now be clamped, eliminating potential scope overload allowing precise P/Z adjustment.

Pole/Zero Using a Ge Detector and a ^{60}Co Source

Adjust the radiation source count rate between 2 kcps and 25 kcps. While observing the AMP OUT signal at the P/Z INSP test point, adjust the P/Z so that the trailing edge of the unipolar pulse returns to the baseline with no overshoots or undershoots.

Figure D.1 shows the correct setting of the P/Z control. Figures D.2 and D.3 show under- and over-compensation for the preamplifier decay time constant. As illustrated in Figure D.1, the UNIPOLAR output signal should have a clean return to the baseline with no bumps, overshoots or undershoots.

Note: Some amplifier shapings may exhibit small undershoots. These arise primarily from amplifier shaping component tolerance and secondary time constants associated with the detector/preamp system. If an undershoot is present and is less than 20 mV, its impact on performance is insignificant. However, if small shaping undershoots are present, they should not be confused with P/Z misadjustment undershoots which exhibit a much longer time constant and have a larger performance impact.

At high count rates, P/Z misadjustment will affect spectral peak shape and resolution:

With correct P/Z, spectral peaks will appear symmetrical.

Undercompensated P/Z will produce low energy tailing.

Overcompensated P/Z will produce high energy tailing.

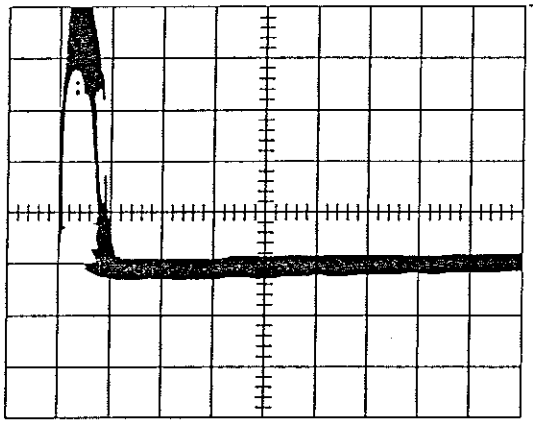

Figure D.1 Correct Pole/Zero Compensation (Source)

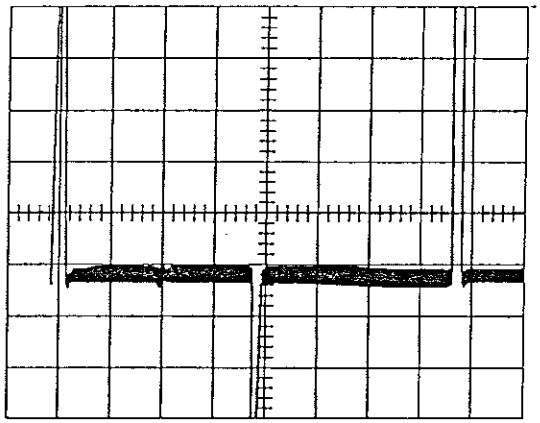

Figure D.4 Correct Pole/Zero Compensation (Square Wave)

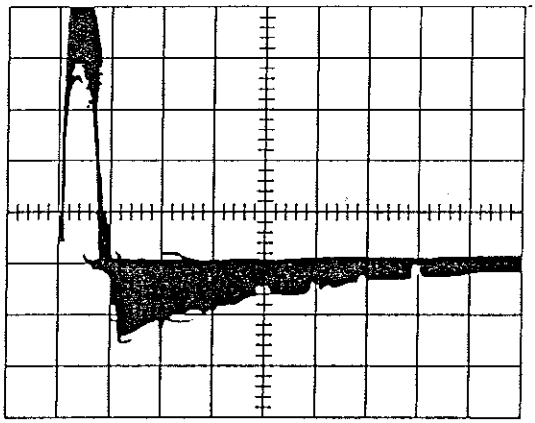

Figure D.2 Undercompensated Pole/Zero (Source)

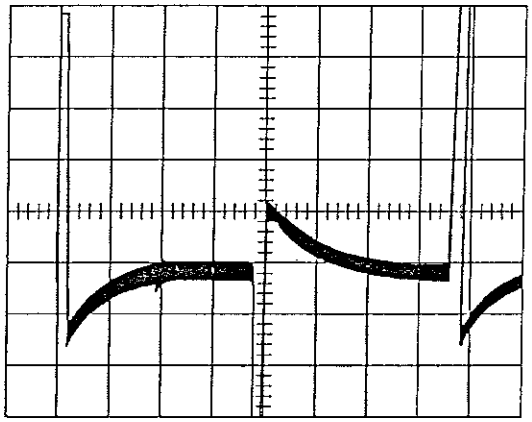

Figure D.5 Overcompensated Pole/Zero (Square Wave)

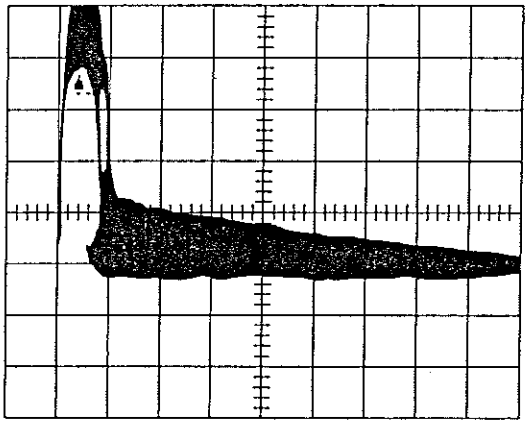

Figure D.3 Overcompensated Pole/Zero (Source)

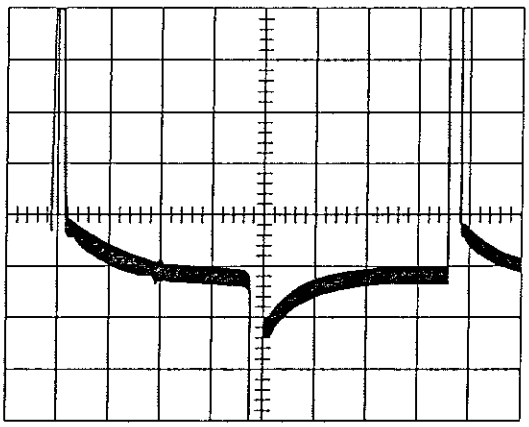

Figure D.6 Undercompensated Pole/Zero (Square Wave)

Oscilloscope:
Vert: 50 mV/div
Horiz: 10 µs/div

Source ^{60}Co
1.33 MeV peak; 7 V amplitude
Count Rate: ≈2 kcps
Shaping: 2 µs

Pole/Zero Adjustment Using a Square Wave Generator

The 1 kHz calibration square wave generated by most oscilloscopes can be used to drive the preamp test input with a square wave for a more precise Pole/Zero adjustment. Connect the scope CALIBRATION Output through an attenuator to the preamp test input and perform the following steps.

1. The amplifier's COARSE GAIN, SHAPING, and INPUT POLARITY controls should be set for the intended application.
2. Adjust the square wave generator for a frequency of approximately 1 kHz.
3. Connect the square wave generator's output to the preamp's TEST INPUT.
4. Remove all radioactive sources from the vicinity of the detector.
5. Set the scope's Channel 1 vertical sensitivity to 5V/div, and adjust the main time base to 0.2 ms/div.
6. Monitor the 1510 AMP OUT signal at the P/Z INSP test point. Do not press the P/Z INSP switch at this time. Adjust the square wave generator's amplitude control (attenuator) for an AMP OUT signal of ± 8 V.

   Note: Both positive and negative unipolar pulses will be observed at the output.

7. Reduce the scope sensitivity to 50 mV/div. To prevent scope overload, clamp the AMP OUT signal by pressing the P/Z INSP switch. With the AMP OUT signal clamped, adjust the P/Z as illustrated in Figure D.6.

Figure D.4 shows the correct setting of the P/Z control. Figures D.5 and D.6 show under- and over-compensation for the preamplifier decay time constant. As illustrated in Figure D.4, the UNIPOLAR output signal should have a clean return to the baseline with no bumps, overshoots or undershoots.

D.2 Amplifier Shaping Selection

Shaping time constant selection generally is a compromise between optimizing throughput and resolution.

For germanium detectors, 4 µs provides better performance over a wider range of count rates and at high count rates.

For high resolution detectors, longer shaping time constants offer better signal to noise (s/n) ratio and reduced sensitivity to the effects of detector ballistic deficit. However, as the system count rate increases, resolution will degrade rapidly as a result of the amplifier's long processing time and the effects of pulse pileup.

The optimum shaping-time constant depends on the detector characteristics (such as size and noise characteristics), preamplifier and incoming count rate. The following table lists shaping-time constant ranges for other detectors.

Detector	Shaping Time in µs
Scintillation Photomultiplier [NaI(Tl)]	0.5 through 1
Planar Implanted Passive Silicon (PIPS)	0.5 through 2
Gas Proportional Counter	0.5 through 2
Lithium Drifted Silicon [Si(Li)]	8 through 12
Lithium Drifted Germanium [Ge(Li)]	2 through 4
Planar Germanium	4 through 12
Silicon Surface-Barrier (SSB)	0.5

Refer to the specific Detector Operator's Manual for the recommended shaping time. This will be a good starting point. Further refinements may be realized through experimentation. Collect spectra using shaping times above and below the recommended to find the one that provides optimal resolution performance for your particular detector and application.

Note: The P/Z must be recalibrated each time the shaping is changed.

D.3 ADC Zero

The ZERO control varies the zero intercept of the ADC conversion function so that zero energy is stored in channel zero of the memory. The Model 1510 ADC is shipped with the ZERO set for a GAIN of 8192. For other ADC GAINs, a slight adjustment of the control may be necessary for precise energy calibration, but is not critical.

For accurate setting of the ZERO control, a Model 8210 Precision Pulser, or equivalent, should be used:

1. Connect the Pulser's SIGNAL OUT to the ADC INput.
2. Set the Pulser to HI, 0°, +, and 0.5 µs Rise Time.
3. Set the ADC's GAIN control as desired.
4. Set all binary switches on the Model 8210 to the *on* (right-hand) position, turn the RELAY *on*, and adjust the COARSE and FINE AMPLITUDE controls for maximum conversion. That is, so that counts are collected in the highest channel of memory.
5. If the memory size is smaller than the GAIN selected, the appropriate OFFSET will have to be switched in on the ADC. For instance, if the memory is 4096 channels and the GAIN is set for 8192, an OFFSET of 4096 must be added so that conversion can take place in the highest channel of the memory.
6. Turn all binary switches on the Model 8210 OFF, except the 1/64 switch, which should be left *on*.
7. Set all OFFSET switches on the ADC to the *off* position.
8. Adjust the ZERO control so that counts are being collected in the proper channel, as shown in the following table.

ADC Gain	Channel
8192	128
4096	64
2048	32
1024	16
512	8
256	4

9. Repeat steps 4 through 8 until no further adjustments are necessary.

10. Note that the ZERO adjustment is made only for the one ADC GAIN setting being used. The ZERO need not be adjusted again unless another ADC GAIN is selected for use.

E. System Considerations with High Resolution Detectors

This section describes some commonly encountered questions about achieving high resolution spectra and some recommendations on how to attain the best performance.

E.1 System Design Considerations

High resolution spectroscopy systems require several connections involving the preamp, bias supply, and spectroscopy amplifier. Under normal operating conditions, this does not present a problem, and optimal performance is achieved.

However, in some applications these connections are unusual in terms of environment, length, or routing. Under such conditions, systems are susceptible to oscillations or noise due to ground loops or to electromagnetic interference (EMI) from sources such as raster displays, power supplies or computers. This interference will degrade the performance of most high resolution detector systems.

The 1510 includes features to minimize these ground loop and EMI problems. However, an awareness of potential problems and care regarding equipment setup, cable routing, and placement can completely solve these problems in most cases.

Amplifier Shaping

The shaping time constant sets the amplifier's frequency response, pulse shape and processing time. The proper choice is usually a compromise between count rate and detector noise bandwidth. For example, a Ge detector usually realizes best results with 4 µs shaping, but at very high count rates the pile-up effects can be reduced with a shorter shaping.

Incorrect shaping can result in resolution degradation due to excessive noise, pile-up at high count rates and detector ballistic deficit. See Appendix D.2.

Amplifier Noise

Amplifier noise is random in nature and is summed in quadrature (RSS) with the noise from the detector and the preamplifier. The amplifier's gain is selected so that the energy range of interest matches the ADC's full scale range. Noise associated with the 1510's amplifier should not be a significant factor.

Baseline Restorer

For best signal to noise performance, a direct coupled amplifier with unipolar shaping would be the best theoretical solution, but is not practical because of offset voltages in the preamplifier and amplifier. Therefore, an ac coupled amplifier is required for dc stability. However, count rate changes can cause shifts in the baseline unless a bipolar pulse shaping or a baseline restorer (for unipolar shaping) is used.

A Baseline Restorer removes the fluctuations in a unipolar amplifier by monitoring the baseline and providing drift correction to maintain a level baseline.

An Auto Threshold circuit in the 1510 amplifier tracks the peak of the random noise and gates the restorer off when the input being processed exceeds the threshold, thus eliminating energy pulse degradation.

ADC Conversion Gain

To calculate the location of a spectrum peak and its Full Width at Half Maximum (FWHM) at least 20 channels are required in the peak. If the peak has fewer channels, the uncertainty in the calculation will increase the computed FWHM.

The ADC Conversion Gain determines the number of channels that the input signal is divided into which affects resolution. For a scintillation detector, a Conversion Gain of 256 or 512 is sufficient to resolve expected peaks; a higher ADC Gain can be used if the Amplifier Gain is not adequate to cover the ADC's input range.

For a Ge detector with the 1.33 MeV ^{60}Co peak at about 90% of ADC full scale, an ADC Gain of 8192 is required to adequately determine the FWHM. With a 4096 ADC Gain, the FWHM calculation can be degraded by about 100 eV because of the granularity of the data points. This can be reduced if a sophisticated peak fitting routine is used.

E.2 System Setup Considerations

The previous factors can be analyzed before assembling the system and are important considerations for system design. The following are some practical points that permit a system to perform to its potential.

Pole/Zeroing

The P/Z (pole/zero) adjustment matches the amplifier to the preamplifier's output pulse fall time and is extremely critical for good high count rate performance. This adjustment compensates for the exponential decay time constant of the preamplifier pulse. The P/Z must be adjusted if the Amplifier Shaping is changed, but need not be adjusted for a change in the Amplifier Gain.

For precise and optimum setting of the P/Z, an oscilloscope vertical sensitivity of 50 mV/cm should be used. However, most scopes will overload for a 10 V input signal when the vertical sensitivity is set for 50 mV/cm, distorting the signal's recovery to the baseline. Thus, the P/Z will be incorrectly adjusted, resulting in a loss of resolution at high count rates. To prevent scope overload and resultant signal distortion, monitor the amplifier output signal at the P/Z INSP test point and hold down the P/Z INSP button to clamp the output signal. See Appendix D.1.

Amplifier Oscillations

If the cable connecting the output of the amplifier to the ADC exceeds 3 m (10 ft.) in length, oscillations can occur. This is caused by the cable capacitance loading the high bandwidth output amplifier.

This should not be a problem since the 1510 amplifier is intended to drive the internal ADC and not require an interconnecting cable longer than 15 cm (0.5 ft).

However, if it becomes necessary for the 1510 amplifier to drive long coax cables, an internal jumper plug (Z_{out}) is provided to place a 93 ohm resistor in series with the output to eliminate potential oscillations. See Appendix C.4.1.

Vibration and Noise

Vibration transmitted to the detector and cryostat can be through the floor or mounting, as well as direct audio coupling through the air. Vibration isolators in the mounting and sound absorbing covers around the detector can reduce this problem. Decreasing the amplifier shaping time constant may improve spectrometer performance in a noisy environment.

Radio Frequency Interference (RFI)

A nearby radio station can sometimes be picked up by a detector. Grounding the preamplifier or cryostat may help, but this can cause ground loops, resulting in 50 or 60 Hz noise.

Analyzer Interference

If the detector is located within a few feet of the MCA, it can receive electromagnetic interference (EMI). In older analyzers this can be from the ferrite cores that were used as memory elements. On the more recent MCAs the display uses a TV type display; these have yoke and flyback transformers that generate large magnetic fields.

The cables connected to the detector must be kept away from the display. **Do not** run the cables in front of the display. See Section 4.3 and Figure 4.2.

Grounding

Grounding problems often cause poor performance from a detector. Generally the best performance is obtained when the 1510, MCA and other associated equipment share a single-point house ground. The detector preamp should be powered from the 1510's rear panel Preamp Power connector, not from a separate power source.

F. ADC Interfacing and Data Transfer

This section will provide information that will be helpful when interfacing the ADC to an MCA.

F.1 ADC Data Transfer

A typical conversion and data transfer sequence is illustrated below:

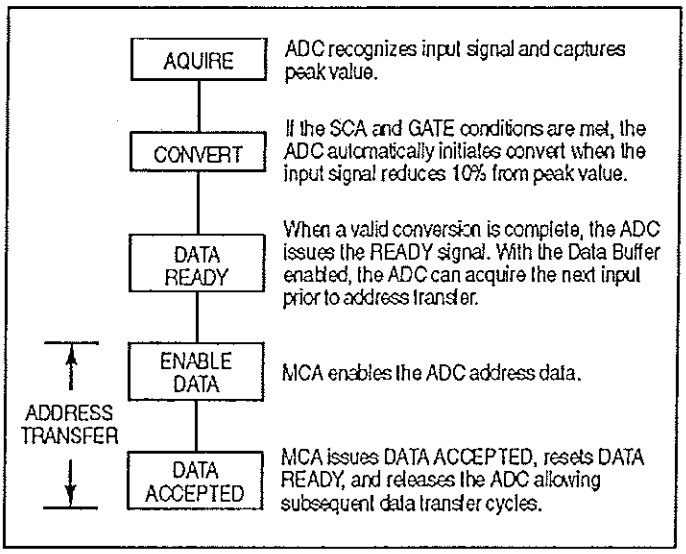

Figure F.1 Typical Conversion and Transfer Sequence

The result of the ADC Conversion is a 13-bit binary coded number or address. At the conclusion of the conversion, the address data is transferred into holding register and the data transfer signal DATA READY is set true. The address data is now valid and can be accessed and used by the MCA or CPU.

If the Buffer is selected (Section C.5.3), the ADC can begin the next conversion even though data transfer to the memory unit is still in process. The 1510 is shipped with the Buffer Option enabled.

Note: If the Data Buffer feature is disabled, the ADC is not allowed to begin the next conversion until the data transfer sequence ends.

The address lines are driven by tri-state drivers activated by ENABLE DATA, which is initiated by the data memory device.

When transfer is complete, the memory device sets DATA ACCEPTED true, releasing the ADC to begin the next pending transfer sequence.

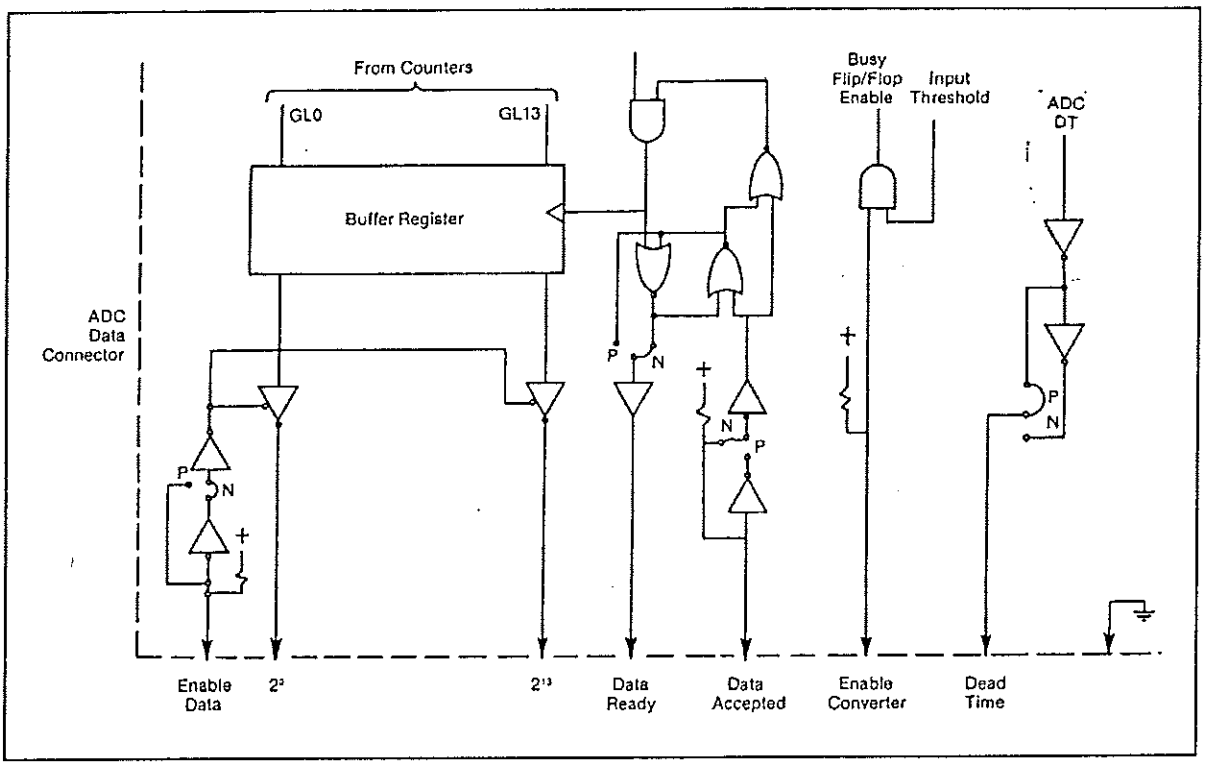

Figure F.2 Representative Interfacing Logic
(See Schematic B-22017 for Details)

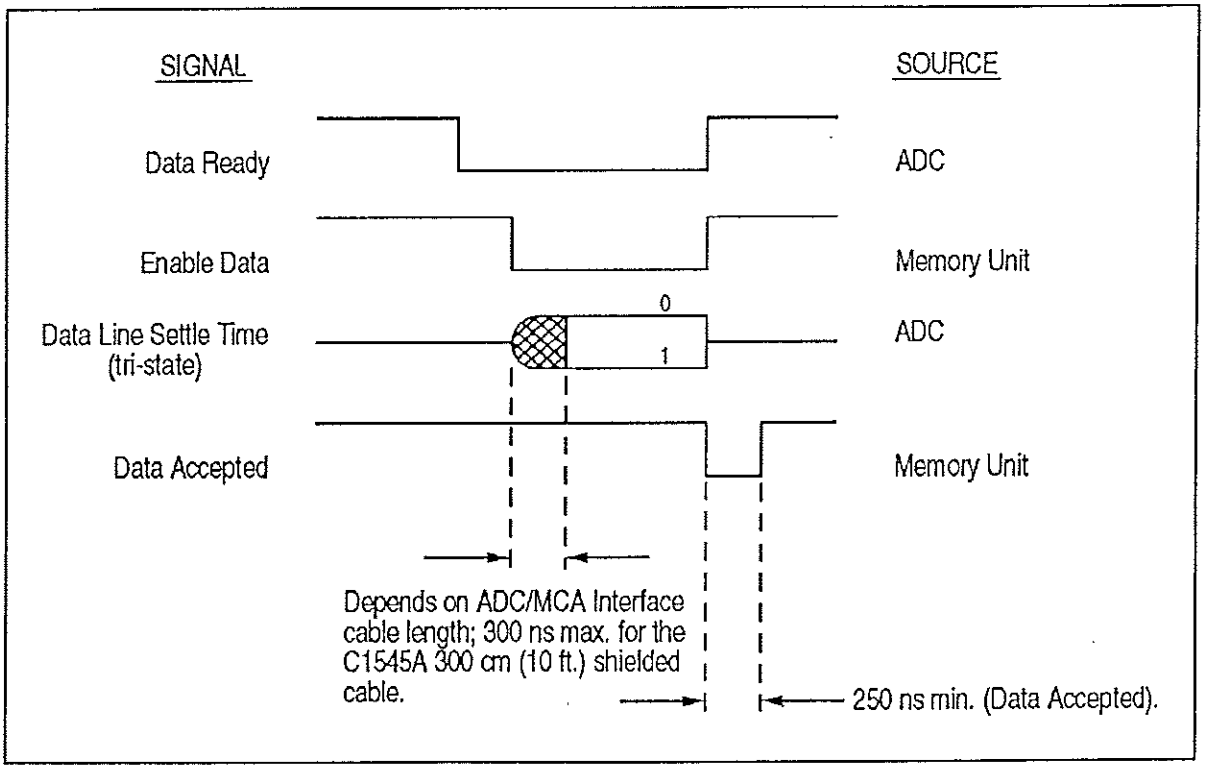

Figure F.3 Data Transfer Timing Diagram

F.2 Dependent ADC Applications

There are two dependent ADC applications, Data Buffer Hold Time and Multi-Parameter Applications to consider.

Data Buffer Hold Time

The ADC data buffer has a maximum hold time of 1 ms. Normally this does not present a problem, since MCA data transfer times are 1 to 20 µs. However, for the longer ADC service times that could be experienced with computer-based data acquisition systems, incorrect conversion values can result.

Multi Parameter Applications

In multiparameter applications involving multiple ADCs, coincident events are acquired for PHA and List Storage.

The data buffer in these applications could let the ADCs get out of synchronization, allowing data transfer for non-coincident events.

To insure proper coincident data collection, synchronization, and applications involving long ADC service times, Canberra recommends disabling the ADC Data Buffer (Appendix C.5.3).

F.3 The Invalid Flag

It may sometimes be necessary to record all inputs whether valid or not. Appendix F.3.1 describes the conditions which will set the INVALID flag output (signal INV at DATA connector pin 20). Because of the ADC buffer operation, the ADC can begin a second conversion even though the first event was not yet accepted by the memory storage device. If a second conversion is completed and is invalid prior to the transfer of the first conversion, there is no way to determine which event, the first or the second, is invalid. Thus, without using the GATE or ENABLE CONVERTER inputs, there is no INVALID/DATA synchronization.

F.3.1 Invalid Flag Conditions

For a conversion to be accepted, it must meet *all* of the following criteria. When any criterion is violated, the INVALID flag (DATA connector pin 20) will be set. Note that the "90% point" mentioned in the following paragraphs is the same as the end of Linear Gate signal.

SCA Window – Pulses not falling within the SCA's window will be rejected, initiating a dump cycle. An LLD or a ULD violation will generate the INVALID flag. Both states are interrogated at the 90% point.

Baseline – Input pulses exceeding the LLD but not the ADC ZERO baseline will be rejected, initiating a dump cycle. The condition is interrogated at the 90% point, setting the INVALID flag when violated.

Digital Underflow – Input pulses resulting in a numeric conversion less than the counter back-bias or less than the digital offset, or both, will be rejected by inhibiting ADC READY. The INVALID flag will be set at EOC (end of conversion).

Digital Overflow – Input pulses resulting in a numeric conversion greater than the ADC RANGE will be rejected by inhibiting ADC READY. The INVALID flag will be set at EOC (end of conversion).

Late Coincidence/Anticoincidence – The GATE pulse width must be at least 250 ns wide and be true (high or open circuit for coincidence, low for anticoincidence) for at least 100 ns before the 90% point. Otherwise the conversion is aborted by initiating a dump cycle. The INVALID flag will be set at the 90% point.

F.4 Dead Time

If PUR/LTC is selected, the Dead Time output is the sum of the ADC conversion time and amplifier dead time. The ADC dead time component begins when an input signal crosses the input threshold, 20 mV to 100 mV controlled by the LLD, and ends at the conclusion of conversion. If PUR/LTC is not selected, the Dead Time is representative of the ADC acquisition and conversion times.

F.5 Enable Converter

The ENABLE CONVERTER input (DATA connector pin 18) can be used to inhibit a later conversion, allowing synchronization of multiple ADCs. If a conversion is in process when the signal is received, it will be allowed to finish its data transfer.

F.6 J102 Data Connector Signals

Pin	Signal	In/Out	Description
1	2^0	Output	
2	2^1	Output	
3	2^2	Output	
4	2^3	Output	
5	2^4	Output	
6	2^5	Output	
7	2^6	Output	Gated binary address data, negative true (0 V) as standard: TTL tri-state outputs; outputs enabled by setting ENABLE DATA to a logic 0, $V_o > 3$ V at 20 mA (high), $V_o < 0.9$ V at 20 mA (low).
8	2^7	Output	
9	2^8	Output	
10	2^9	Output	
11	2^{10}	Output	
12	2^{11}	Output	
13	2^{12}	Output	
14	DATA READY	Output	Signals external memory storage unit that a conversion is complete; positive true or negative true logic, set by internal jumper J8; shipped in negative true position.
17	DATA ACCEPTED	Input	Feedback signal from the memory storage unit which acknowledges data acceptance. This pulse resets the ADC and clears the INValid flag, if set. Positive true or negative true logic set by internal jumper J7; shipped in negative true position. TTL hysteresis input with a 4.7 kΩ pull-up resistor to 5 V.
18	ENABLE CONVERTER	Input	Used to gate the ADC on or off. Pulses in progress before this signal starts will be allows to finish the output sequence; further inputs will be ignored. Postive true logic. TTL hysteresis input with a 4.7 kΩ pull-up resistor to 5 V.
20	INV/	Output	Invalid; set by digital under or overflow (OVF) if the ADC input is not within the SCA window or does not exceed the ZERO intercept setting. Invalid may also be set if the linear input with a COINC Gate signal is not large enough to cause conversion. The INV/ signal is reset by the DATA ACCEPTED signal. Negative true logic. TTL output with a 4.7 kΩ pull-up resistor to 5 V.
21	DEAD TIME	Output	Used to Enable the live time circuit to control storage periods. Positive true or negative true logic; set by internal jumper J10; shipped in positive true position. TTL hysteresis input with a 4.7 kΩ pull-up resistor to 5 V.
22	ENABLE DATA	Input	Used to gate the 13-bit data onto the output lines. Positive true or negative true logic, set by internal jumper J6; shipped in negative true position. TTL hysteresis input with a 4.7 kΩ pull-up resistor to 5 V.
24	GND	.	Ground.

G. Rack Mount Hardware

Rack mount brackets and hardware are included in the 1510 accessory package. Using the #10-32 x 1/4 pan head screws, attach the left and right brackets as shown in Figure G.1.

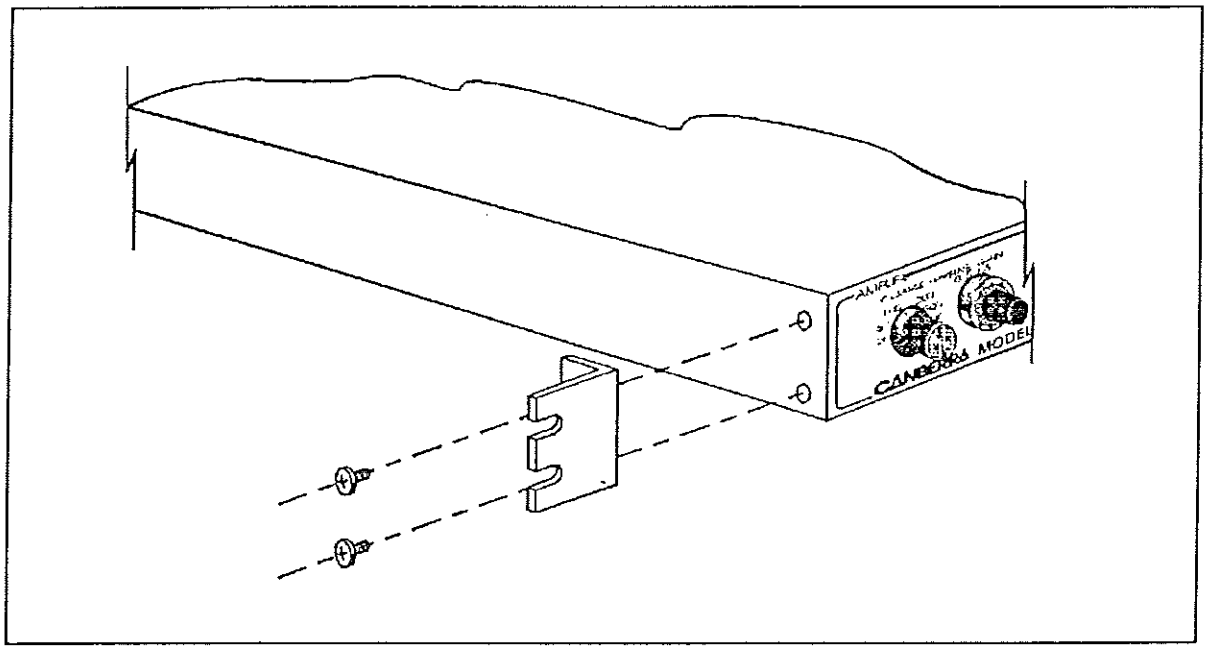

Figure G.1 Installation of Rack Mount Hardware

H. ADC/MCA Interface Cables

This section provides information regarding the available ADC/MCA interface cable options and connector-retaining hardware installations. One of these cables is shipped with your 1510, depending on the particular model of the 1510 you ordered.

H.1 Hardware Installation

The MCA end of the ADC/MCA interface cable does not have the retaining hardware installed. A small bag containing the hardware is included as part of the 1510 accessory package.

Two connector retaining methods commonly employed are screws (jacking screw) and catch set (spring clips).

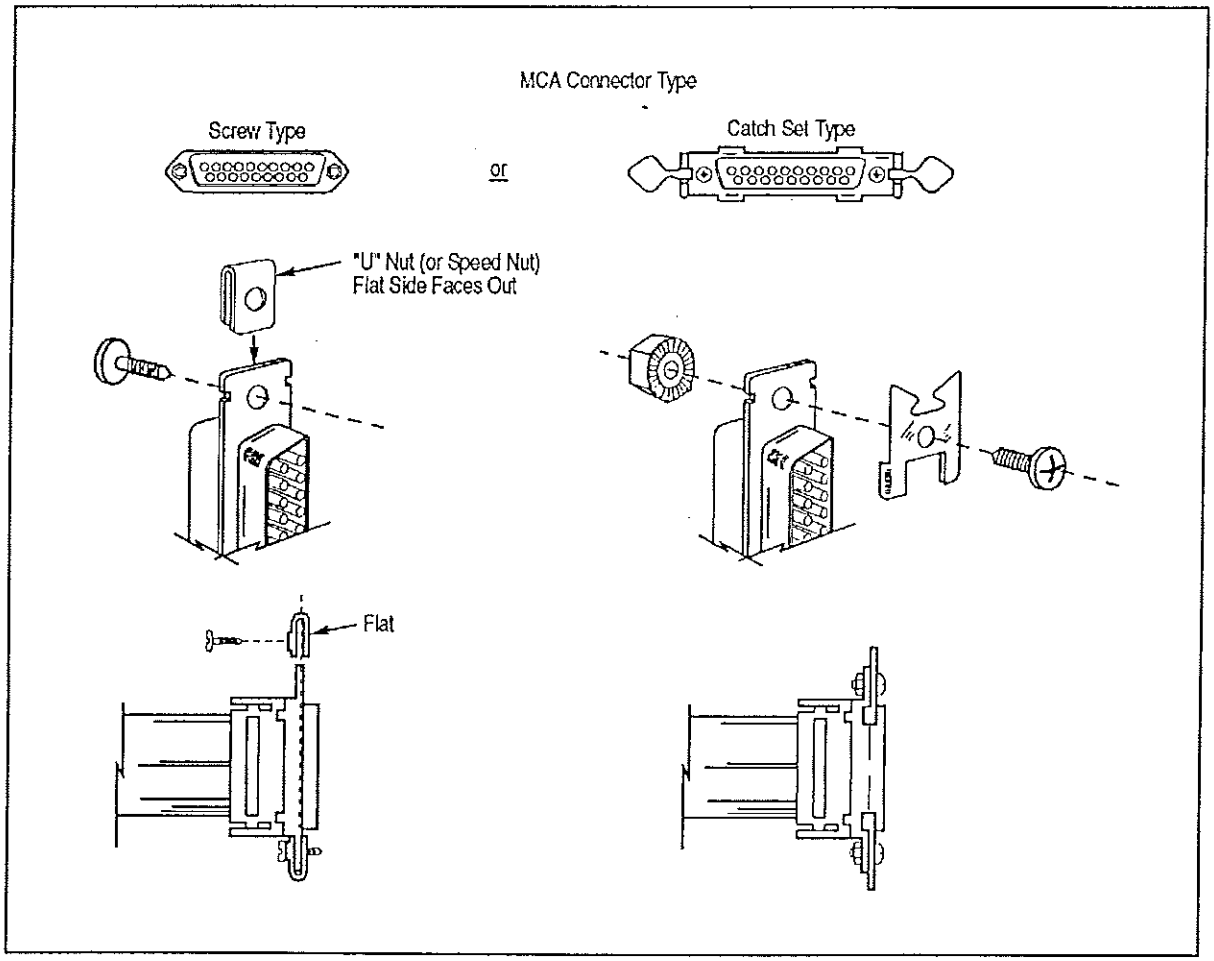

Figure H.1 Connector Hardware Assembly

Determine which method is to be used on the intended MCA and assemble the appropriate hardware as shown in Figure H.1.

H.2 C1547-4 ADC/MCA Interface Cable

The 1.2 m (4 ft) C1547-4 ribbon cable, shipped with the Model 1510-01, connects the 1510-01 to the Series 35, Series 35 Plus, Series 40, Series 80, Series 85, Series 88, Series 90, Series 95 and System 100 MCAs.

The 25-pin D-style connector with a plastic housing connects to J102 on the 1510-01. The 25-pin D-style connector with a metal housing connects to one of the MCAs listed above. This cable has a one-to-one signal translation.

H.3 C1545A ADC/MCA Interface Cable

The 3 m (10 ft) optional C1545A cable is a special shielded cable for connecting the 1510-01 to the Series 35, Series 35 Plus, Series 40, Series 80, Series 85, Series 88, Series 90, Series 95 and System 100 MCAs. This cable is available at extra cost; please consult the factory.

H.4 C1556 ADC/MCA Interface Cable

The 1.2 m (4 ft) C1556 cable, shipped with the Model 1510-02, connects the 1510-02 to the Accuspec B or Accuspec MC MCAs. The 25-pin D-style end of the cable connects to J102 on the 1510-02. The 37-pin D-style end of the cable plugs directly into the connector on the Accuspec B or Accuspec MC board. The short ribbon adaptor provided with the MCA is not needed; it should be kept for possible use with other system configurations.

ADC (25-pin D-Male)		MCA (37-pin D_Male)	
Signal	Pin	Pin	Signal
2^0/	1	26	(ADC 0*)
2^1/	2	27	(ADC 1*)
2^2/	3	28	(ADC 2*)
2^3/	4	29	(ADC 3*)
2^4/	5	30	(ADC 4*)
2^5/	6	31	(ADC 5*)
2^6/	7	32	(ADC 6*)
2^7/	8	8	(ADC 7*)
2^8/	9	9	(ADC 8*)
2^9/	10	10	(ADC 9*)
2^{10}/	11	11	(ADC 10*)
2^{11}/	12	12	(ADC 11*)
2^{12}/	13	13	(ADC 12*)
DATA RDY/	14	24	(READY*)
2^{13}/	15	7	Not used
INHAD/†	16	25	(INH*)
DATA ACCEPT/	17	20	(CLADC*)
ENABLE CONVERT/	18	23	(ACQ*)
DEAD TIME/	21	22	(ADCB*)
ENDATA/	22	21	(ATR*)
GND	24	1,2,3,4,5,6	GND

† Internal controls: The C1556 cable's internal jumpers are set to: 1 to 2, 4 to 5, and 7 to 10.

H.5 C1554 ADC/AIM Interface Cable

The 1.2 m (4 ft) C1554 cable, shipped with the Model 1510-03, connects the 1510-03 to the Model 556 AIM Module.

The 25-pin D-style end of the cable connects to J102 on the 1510-03. The 34-pin keyed ribbon cable connector plugs directly into the connector on the Model 556.

ADC (25-pin D-Male)		MCA (34-pin Ribbon Conector	
Signal	Pin	Pin	Signal
2^0/	1	14	(ADC 0*)
2^1/	2	16	(ADC 1*)
2^2/	3	18	(ADC 2*)
2^3/	4	20	(ADC 3*)
2^4/	5	22	(ADC 4*)
2^5/	6	24	(ADC 5*)
2^6/	7	26	(ADC 6*)
2^7/	8	15	(ADC 7*)
2^8/	9	17	(ADC 8*)
2^9/	10	19	(ADC 9*)
2^{10}/	11	21	(ADC 10*)
2^{11}/	12	23	(ADC 11*)
2^{12}/	13	25	(ADC 12*)
DATA RDY/	14	10	(READY*)
2^{13}/	15	34	Not used
INHAD/†	16	12	(INH*)
DATA ACCEPT/	17	2	(CLADC*)
ENABLE CONVERT/	18	8	(ACQ*)
DEAD TIME/	21	6	(ADCB*)
ENDATA/	22	4	(ATR*)
GND	24	1,3,5,7,9,11	GND

† Internal controls: The C1554 cable's internal jumpers are set to: 1 to 2, 4 to 5, and 7 to 10.

WARRANTY

This warranty covers Canberra hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Equipment manufactured by Canberra's Instruments Division, Detector Products Division, and Nuclear Systems Division is warranted against defects in materials and workmanship for one year from the date of shipment.

Canberra warrants proper operation of its software only when used with software and hardware supplied by Canberra and warrants software media to be free from defects for 90 days from the date of shipment.

If defects are discovered within 30 days of the time you receive your order, Canberra will pay transportation costs both ways. After the first 30 days, you will have to pay the transportation costs.

This is the only warranty provided by Canberra; there are no other warranties, expressed or implied. All warranties of merchantability and fitness for an intended purpose are excluded. Canberra shall have no liability for any special, indirect or consequential damages caused by failure of any equipment manufactured by Canberra.

EXCLUSIONS

This warranty does not cover equipment which has been modified without Canberra's written permission or which has been subjected to unusual physical or electrical stress as determined by Canberra's Service Personnel.

Canberra is under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than Canberra personnel without the prior approval of Canberra.

This warranty does not cover detector damage caused by abuse, neutrons, or heavy charged particles.

SHIPPING DAMAGE

Examine shipments carefully when you receive them for evidence of damage caused in transit. If damage is found, notify Canberra and the carrier immediately. Keep all packages, materials and documents, including your freight bill, invoice and packing list. Although Canberra is not responsible for damage sustained in transit, we will be glad to help you in processing your claim.

OUT OF WARRANTY REPAIRS

Any Canberra equipment which is no longer covered by warranty may be returned to Canberra freight prepaid for repair. After the equipment is repaired, it will pass through our normal pre-shipment checkout procedure.

RETURNING EQUIPMENT

Before returning equipment for repair you must contact your Regional Service Center or one of our factories for instructions. For detector repair, contact the Canberra Detector Division in our Meriden, Connecticut, factory for instructions. If you are going to return the equipment to the factory, you must call first to get an Authorized Return Number (ARN).

When you call us, we will be glad to suggest the best way for you to ship the equipment and will expedite the shipment in case it is delayed or lost in transit. Giving you shipping advice does not make us responsible for the equipment while it is in transit.

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