LINEAR GATE
and
STRETCHER
Model 1454

Instruction Manual

December, 1972

CANBERRA INDUSTRIES, INC.
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Meriden, Connecticut 06450

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WARRANTY

Canberra-Manufactured Equipment

Equipment manufactured by Canberra Industries, Inc. is warranted against defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in the instruction manuals. Repairs or replacement, at Canberra's option, will be made without charge at the Canberra factory during this warranty period. Except for the case of defects discovered upon initial operation, shipping expense to Canberra is to be paid by the customer; shipping expense to return the repaired equipment will be paid by Canberra.

The customer must obtain shipping instructions, including an *Authorized Return Number* (ARN), before returning any equipment to the Canberra factory. Compliance with this provision by the customer shall be a condition of this warranty. In giving shipping instructions, Canberra shall not, therefore, assume any liability in connection with the shipment. If, upon receipt of the equipment, Canberra determines that such equipment is not defective within the terms of this warranty, the customer shall pay to Canberra upon invoice, the cost of all transportation and cost of repairs at the then prevailing Canberra repair rate.

This warranty shall not apply to equipment that has been modified or serviced by other than Canberra service personnel, or to failures caused by defective equipment not supplied by Canberra.

This warranty applies only to equipment manufactured by Canberra. On other equipment supplied by Canberra, the full warranty, and only that warranty offered by the original manufacturer, will be passed on to the customer.

WARRANTY ON EQUIPMENT NOT MANUFACTURED BY CANBERRA

Canberra's basic one-year warranty applies only to equipment manufactured by Canberra. Although Canberra may frequently supply, as part of systems, equipment manufactured by other companies, the only warranty that shall apply to such non-Canberra equipment is that warranty offered by the original manufacturer.

Canberra will, upon request, state what warranties are offered by the original manufacturers of such items as computers, teletype machines, printers, plotters, and other non-Canberra equipment which may be supplied as part of a Canberra system. In no case, however, will Canberra assume any liability for such equipment other than to pass on to its customer whatever warranty is supplied by the original manufacturer.

WARRANTY ON SOFTWARE

Canberra will warrant system operation with *Canberra Laboratory Automated Software Systems* (CLASS) only. If the customer decides to use software other than CLASS, Canberra assumes *no* responsibility. Engineering assistance, however, for non-CLASS software is available to the user and should be contracted separately if desired.

ON-SITE WARRANTY OPTION

The basic Canberra warranty applies only to equipment manufactured by Canberra which is *returned to the factory.* If equipment must be repaired at the customer's site, the actual repair labor and parts will be provided at no charge during the warranty period. However, travel expenses to and from the customer's site, and living expenses while on site, shall be paid by the customer unless an on-site warranty option has been purchased. This option may only be purchased prior to shipment of the equipment to the customer.

The on-site warranty option provides for free on-site warranty work (Canberra pays all travel and living expenses) within the first 60 days after delivery of equipment to the customer. If installation is ordered from Canberra, the 60 day period commences upon completion of the initial installation. After the 60 day period, labor and materials used on site will still be covered by the basic warranty, but the customer shall pay for all travel and living expenses incurred for any on-site service.

The price of this 60 day on-site warranty option is $300.00 or two percent (2%) of the entire system list price, whichever is greater.

The on-site warranty option is available only within the contiguous forty-eight (48) United States and Canada.

After the 60 day on-site warranty period, or after initial installation of the equipment, a maintenance contract may be purchased. This is to be contracted through Canberra's Customer Engineering Department. Contact the factory for details concerning maintenance contracts.

INSTALLATION

Installation of equipment purchased from Canberra shall be the sole responsibility of the customer unless it is specifically contracted for at the prevailing Canberra field service rates. To insure timely installation after receipt of equipment, it is recommended that installation be contracted for at the time the equipment is ordered.

REPAIRS

Any Canberra-manufactured instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. When returning instruments for repair, contact the factory for shipping instructions and an *Authorized Return Number* (ARN).

All correspondence concerning repairs should include Model Number and a description of the problem observed.

Once repaired, all equipment passes through our normal pre-shipment checkout procedure, and will meet or surpass its original specifications when returned. Return shipping expense on out-of-warranty repairs will be charged to the customer.

For instruments out of warranty, the customer must supply a purchase order number for the repair before the item will be returned.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, immediately notify Canberra and the carrier making delivery, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in damage claims.

LINEAR GATE and STRETCHER

Model 1454

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and
STRETCHER

Model 1454

Section 1
INTRODUCTION

The Canberra Model 1454 Linear Gate and Stretcher provides a standardized optimum shaped output for fuller utilization of the capabilities of a multichannel analyzer in high-rate/high-resolution nuclear spectroscopy. An extremely flexible module, the Model 1454 includes a pulse stretcher, DC coupled linear gate, DC restorer, and pulse pileup rejector.

The integral pulse stretcher portion of the Model 1454 compensates for the incompatibility of multichannel analyzers which have stringent requirements for input pulse shapes. All main amplifier pulses are converted to a standardized linear output pulse shape, variable in width (1-5μsec) and delay time (0.5 to 5μsec) via front panel controls. Rectangular in appearance, the linear stretched output is essentially flat topped with very little droop (< 0.3mV/μsec). Thus, linearity of the succeeding MCA is improved where sharply peaked pulse shaping has been used in the main linear amplifier.

Total DC coupling, fast circuitry, baseline restoration, and pileup rejection all contribute to preserve spectral resolution at high count rates. The integral DC restorer permits the use of existing amplification systems in high rate experiments and increases the count rate capabilities of the Model 1454. Sophisticated pulse pileup rejection circuitry enhances high rate performance; after the input pulse has reached its peak, subsequent pulses are automatically inhibited until both the output pulse has terminated and the input recovered to the baseline.

A choice of externally gating or strobing the Model 1454 output is available, with Coincidence/Anticoincidence gated mode of operation. Therefore, analyzer overload may be minimized without requiring additional gating modules.

DC operation of the multichannel analyzer is essential for optimum count rate performance when using the Model 1454. A rear panel Period Output supplies the necessary logic information to enable DC operation of certain MCA's. Selectable output polarity and full scale output voltage range of 3, 5, or 10 volts ensures maximum MCA compatibility.

Section 2

SPECIFICATIONS

2.1 INPUTS

SIGNAL INPUT	Polarity: positive 0.1 to 10V unipolar or bipolar linear pulses Rise time: ⩾ 100 nanoseconds Width: ⩾ 300 nanoseconds Input impedance: approximately 250 ohms for 0.1V signal; ⩾ 20K ohms over 1V; DC or DC restorer coupled
GATE INPUT	Polarity: positive logic pulse or DC level, ⩾ 3.5V (± 20V max) Width: ⩾ 100 nanoseconds Input impedance: approximately 2K ohms, DC coupled

2.2 OUTPUTS

SIGNAL OUTPUT	Polarity: positive or negative 0.1 to 10V essentially flat topped rectangular pulse Rise time: approximately 0.5 microsecond; duration and delay as selected by front panel controls; DC offset variable from -2V to +2V Output impedance: ⩽ 0.1 ohm, DC coupled
PERIOD OUT	Polarity: +5V logic pulse, leading edge in time coincidence with Signal Output Duration: essentially equal to Signal Output Output impedance: 50 ohms, series-connected, DC coupled

2.3 PERFORMANCE

INTEGRAL NONLINEARITY	< ± 0.05% from 0.1 to 10V output for inputs with rise time ⩾ 200 nanoseconds
STRETCHER DROOP	< 0.3mV/microsecond
GATE FEEDTHROUGH	< 0.05% of signal amplitude with gate closed
GATE PEDESTAL	essentially zero pedestal, factory calibrated
NOISE CONTRIBUTION	< 20 microvolts rms, referred to input
PILEUP REJECTION	after the input pulse has reached its peak, subsequent pulses are atuomatically inhibited until both the output pulse has terminated and the input recovered to the baseline

TEMPERATURE OPERATING RANGE	0 to 50°C
TEMPERATURE STABILITY	Output DC level: ≤ 0.1 mv/°C Gain: $\leq 0.0075\%$/°C
COUNT RATE STABILITY	$< 0.1\%$ pulser peak shift at 80% of full scale when modulated by 0-80kHz of random Cs^{137} with photopeak at 70% of full scale, using Model 1413 amplifier with active filter time constant of 1 microsecond unipolar

2.4 CONNECTORS

SIGNAL INPUT, SIGNAL OUTPUT, GATE INPUT	front panel, BNC UG-1094/U
PERIOD OUT	rear panel, BNC, UG-1094/U

2.5 POWER

+24V	–	35mA
- 24V	–	60mA
+12V	–	140mA
- 12V	–	75mA

2.6 PHYSICAL

SIZE	single-width NIM module (1.35 x 8.714 inches) per TID-20893 (Rev.)
WEIGHT	2.0 lb (3.5 lb. shipping weight) .90 kg (1.58 kg shipping weight)

Section 3

OPERATING INSTRUCTIONS

3.1 GENERAL

The purpose of this section is to familiarize the user with the controls of the Model 1454 Linear Gate and Stretcher and to be sure that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following processes are carried out, the user will gain sufficient familiarity with the instrument to permit its proper use in the system at hand.

3.2 SET UP

1. Insert the module in an AEC compatible base unit/power supply such as the Canberra Model 1400 and interconnect with other modules as shown in Figure 3-1. Turn on the Power switch.

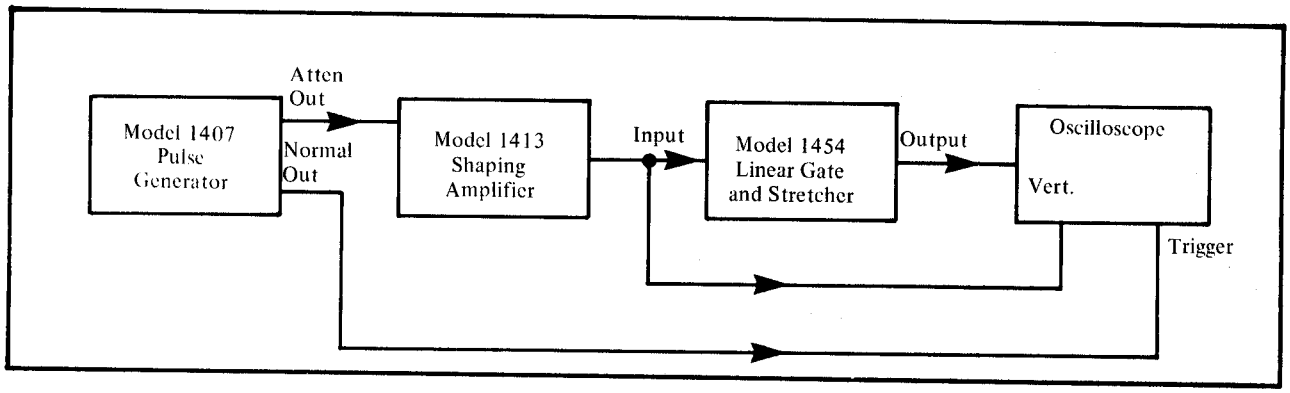


Figure 3-1. Test System Connections.

2. Set the controls of the Model 1454 as follows:

Restorer:	LO
Gate Mode:	ANTI
Delay & Width:	min. (fully CCW)
DC Level:	Leave at factory adjustment
Range:	10V
Polarity:	POS

3. Connect the Output of the Model 1454 to the B input of an oscilloscope.

3.3 INITIAL CHECKOUT

1. Connect an oscilloscope probe (A input) to the test point at the input. Set the amplifier for 1 μsec shaping and gain sufficient to give a 1 volt output. Observing the amplifier output, set the oscilloscope for 0.1V sensitivity and 50 μsec/cm sweep. Adjust the Pole/Zero compensation of the shaping amplifier for correct compensation. Change the scope sensitivity to .5V/cm and the sweep speed to 1 μsec. Now observe the Model 1454 input (A input) and Output (B input) at the same time on the scope. The waveshapes should be similar to those shown in Figure 3-2.

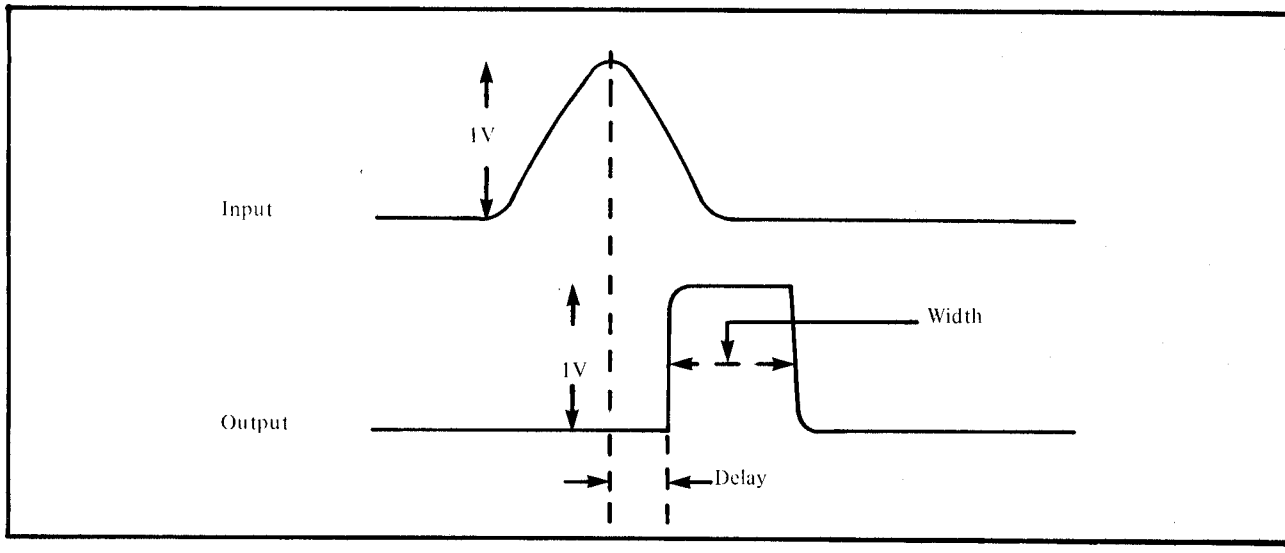


Figure 3-2. Input-Output Waveforms.

2. Now by varying the Delay control, the output pulse can be delayed up to 5μsec. This 5μsec can be increased up to 25μsec by replacing the removable delay timing capacitor on the P.C. board with a .0047 nfd cap. This is shown in the Internal Adjustment diagram located in the control section. Return the control to min. delay.

3. Vary the Width control. The output pulse width should vary from 1μsec to at least 5μsec. Return to min.

4. Change the Range switch from 10 to 5 and then to 3. The output should go from 1 volt to .5 volts to .33 volts. Return to 10 and change the Polarity switch to Negative. Notice the output is now a negative 1 volt pulse. Return to Positive and increase the input to yield a 10 volt output (input 10 volts).

3.4 ADVANCED FAMILIARIZATION

3.4.1 PILE UP REJECTION

1. Replace the Model 1407 Pulse Generator with a Model 1407P Pulse Pair Generator (or equivalent). Set the pulse generator to approximately 5kHz pulse rate, Mode to Pulse Pair, and Delay to 7μsec. (variable to 10). Adjust oscilloscope sweep speed and observe both input pulses. Now adjust the Model 1407P amplitude and the gain of the shaping amplifier so that both pulses are 3 volts.

2. With the Width and Delay control set at min (fully CCW), observe the output of the Model 1454. Both pulses should appear with an amplitude of 3 volts. Decrease delay of second pulse from the Model 1407P, observing that the output of the Linear Gate and Stretcher is inhibited for the second pulse if the pulse pair separation is closer than 3μsec. (Pulse pair separation is defined as the time interval between the finish of the first pulse and the start of the second pulse).

3. Increase the Delay control on the Model 1454, notice the second pulse is inhibited sooner. The pulse pair separation now becomes 3 μsec plus the delay time. Return delay to min.

4. Now observe the Model 1454 Input and Output on a dual trace oscilloscope. Gradually reduce the pulse pair separation until the two input pulses begin to overlap; observe that the output is still that of the first input signal until the inflection point of the input is less than 50 millivolts when the output amplitude becomes the sum of the two peaks.

The Model 1454 rejects tail pile up pulses. Now change the Model 1407P to Dual Pulse so only one pulse appears at Input and Output of the Model 1454. Also increase the Delay and Width controls on the Model 1454 to max. (fully CW).

3.4.2 GATED MODE

1. With the Gate Mode switch in Anti (as originally shipped), the output of the Model 1454 is enabled as long as there is no positive voltage greater than 3.5 volts applied to the Gate Input BNC. If this voltage is applied, the output will be disabled for the duration of the positive voltage. If, however, the Gate Mode is changed to Coinc., the Gate Input will have just the opposite effect.

2. To obtain a suitable Gate Input signal, use a Canberra Model 1455A Logic and Delay unit (or equivalent). Set the amplitude of the Positive Routing Output to 5 volts and the baseline at approximately 0 (baseline adjust is internal). Trigger the Model 1455A from the Trigger output of the Pulse Generator. Adjust the Delay for min. and the width to about 1μsec. Now connect the Positive Routing Output of the Model 1455A to the Gate Input of the Model 1454.

3. With the Model 1454 Gate Mode in the Coinc. position, observe that the output is enabled. Now adjust the Delay of the Model 1455A so that the Gate Pulse begins after the delay time of the Model 1454 (delay time ends at the beginning of the output pulse).

Observe the Output now is disabled. Change the Gate Mode to Anti and observe the output enabled again. Now if the leading edge of the gate is returned to its original position, the output is disabled. Therefore, in the Anti mode, the output is disabled, if the gate is positive from when the input signal exceeds 100mV until the end of the delay time of the Model 1454 (delay time starts at the peak of the input and finishes at the start of the Output and is adjustable). In the Coinc. Mode, the Output is enabled if the gate is positive during the same time period. It should be noted that the min. width needed to trigger the gate circuit is 100 nanoseconds.

3.4.3 STROBED MODE

With the Model 1455A set for maximum delay and a 1μsec wide pulse, change the internal Strobe Mode switch to the Strobe position. Now gradually increase the delay of the Model 1455A until an output appears. Notice now that the Output begins when the gate pulse goes positive, if after the peak of the input signal, and that the delay of the Model 1454 does not effect the point at which it starts. However, in this mode, the gate can only enable the output if it goes positive during the delay time of the Model 1454. To increase delay time of the Model 1455A to 25μsec, refer to Figure 4.2.

3.5 OPERATION WITH A LIVE SOURCE

1. Replace the pulse generator with a live detector and source at a low counting rate. Also remove the Model 1455A. On the Model 1454, place Gate Mode to ANTI, and the Strobe Mode switch to Gated.

2. Observe the input pulses containing the energy of peaks of interest.

3. Observe the Output pulses containing the energy of peaks of interest. This can now be adjusted for optimum condition of the MCA.

3.6 INPUT/OUTPUT REQUIREMENTS

1. DC restored input should be selected if the preceding linear amplifier has AC coupling. The LO rate position is used for duty cycles less than 20%, the HI position for duty cycles above 20%.

If the preceding amplifier is DC restored, use the DC position of the Restorer. Before connecting the Amplifier/Restorer, measure the DC level at the input test point of the Model 1454, then adjust the DC level output of the Amplifier/Restorer to the same input voltage of the Model 1454.

2. The Output DC level of the Model 1454 is adjustable from ±2V to - 2V to provide matching the input requirements of the following instrumentation (typically a multichannel analyzer). To get the full performance from the Model 1454, the input of the MCA must be DC coupled.

3. The Period Output pulse provides the necessary logic signal to open the Multichannel Analyzer linear gate when the linear output is present, thus enabling DC operation of the MCA ADC without the necessity of supplying a non-delayed signal to operate the MCA discriminators.

The relatively fast rise time of the Model 1454 Output signal will cause spectrum broadening of the line width with some MCA's of other manufacturers. By using the Period Output logic pulse as a coincidence input signal to control the MCA linear gate, the high resolution capabilities of the Model 1454 may be realized.

Figure 3-3 shows a typical connection to an MCA.

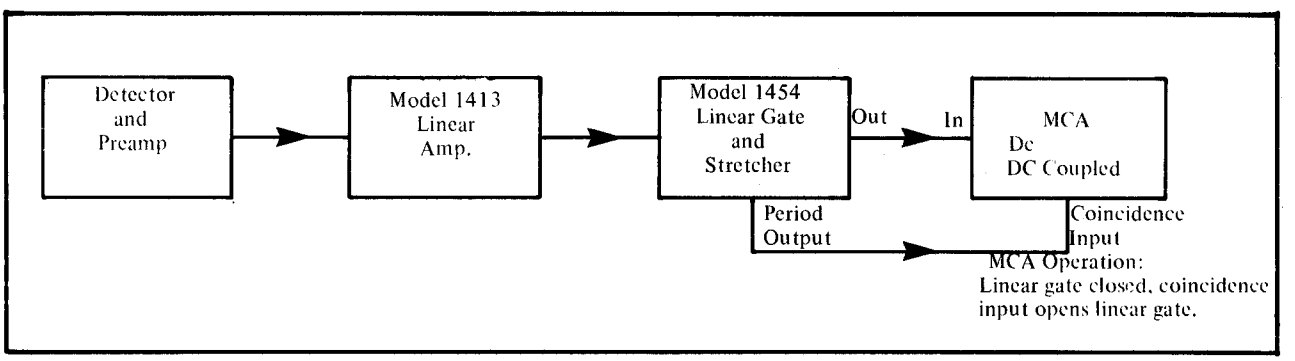
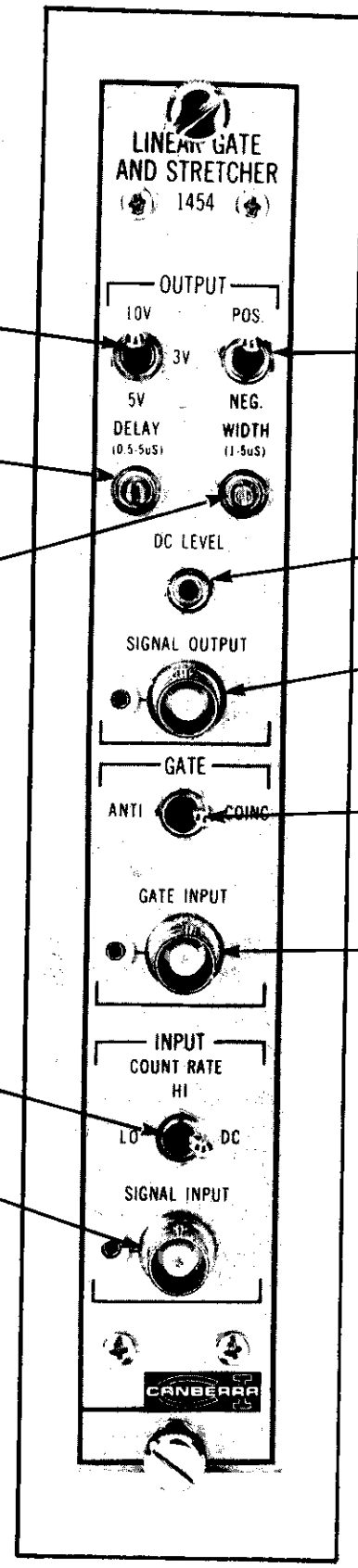


Figure 3-3. Typical Connection to MCA.

Section 4

CONTROLS AND CONNECTORS

4.1 FRONT PANEL CONTROLS



OUTPUT RANGE
Selects Full Scale Output signal range .03 to 3V, .05 to 5V and .1 to 10V, with respect to 0-10V input.

DELAY
Determines time of Output after peak of input. 0.5 to 5 microsecond range.

WIDTH
Determines width of output pulse 1 to 5 microsecond range.

POLARITY OF OUTPUT SIGNAL
Either positive or negative.

DC LEVEL
Varies zero level of output from - 2V to +2V. Factory set to 0 ± 25mV.

OUTPUT
Essentially flat top pulse, maximum 10V into 100 ohms. Rise time 500 nanoseconds.

GATE MODE
ANTI - Outputs occur unless gate signal is received.
COINC. - No output until gate signal is received.

GATE INPUT
Gate In requires +3V signal.

RESTORER
Setup for HI and LO count rates. DC coupled to use external DC restorer.

INPUT SIGNAL (0.1-10V)
Input from shaping amplifiers, Unipolar or Bipolar, Positive signal first.

Figure 4-1. Front Panel, Model 1454.

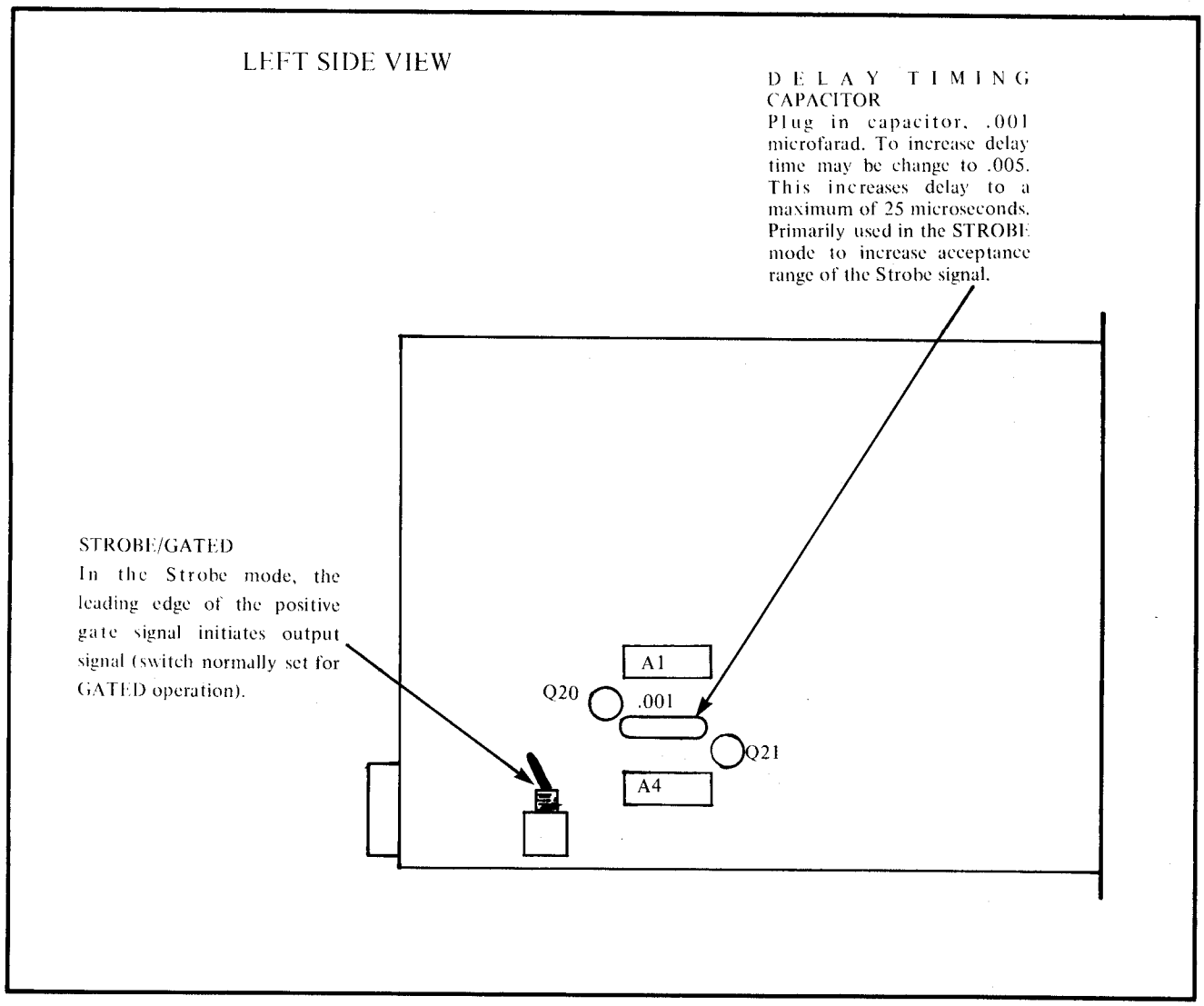


Figure 4-2. Internal Controls and Connectors, Model 1454.

4.3 REAR PANEL CONNECTOR

PERIOD OUTPUT
A positive 5 volt logic pulse occurring in coincidence with the Signal Output.

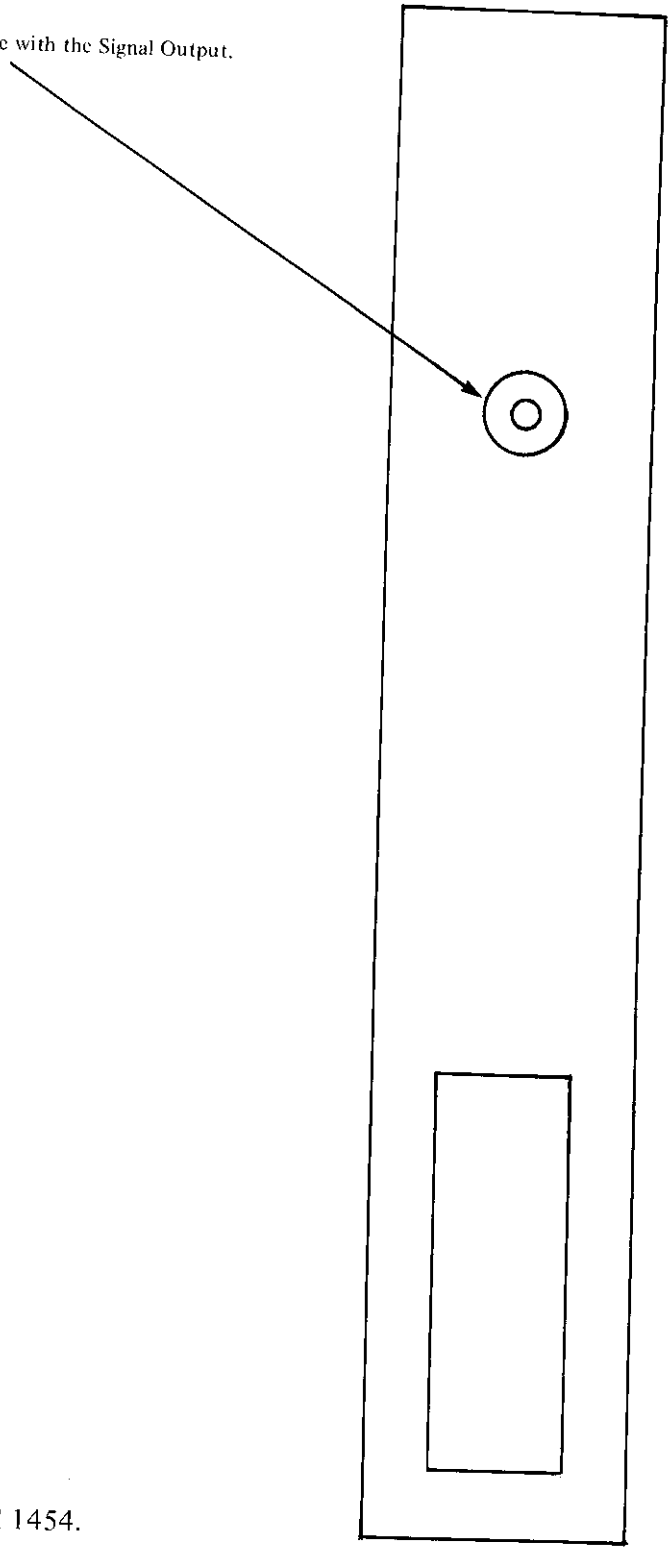


Figure 4-3. Rear Panel, Model 1454.

Section 5

CIRCUIT DESCRIPTION

5.1 GENERAL

The Model 1454 Linear Gate and Stretcher is described in detail by the following sub-sections:

DC Restorer and Input Buffer
Stretcher
Output Amplifier
Controlling Logic

Reference to the Block Diagram (Figure 5-1) and Timing Sequences (Figures 5-2 and 5-3) will be helpful in the following discussion of the various circuits.

5.2 DC RESTORER AND INPUT BUFFER

The Input Signal is applied to the Restorer Q1, Q2, then to the Buffer, non-inverting Amplifier.

The Restorer switch provides three modes of operation by differentiating the input signal at different rates. DC provides direct coupling to the input, LO provides differentiating at a slow rate, and HI provides differentiating at a faster rate. The signal is then referenced to a DC zero by the constant current sources Q1 and Q2 feeding two diodes. These diodes, by virtue of the constant current through them, will exhibit a constant voltage drop and thereby establish a DC zero to the input of the amplifier. The input buffer amplifier is a basic closed loop, non-inverting amplifier with unity gain. The input differential dual transistor (Q4) has equal collector currents and voltages for maximum temperature stability. Q7 is a constant current source located in the emitter of Q4. This provides a constant current through Q4 and also is reflected as a high input impedance at the input of the amplifier. Q3 is a constant current source for a high impedance load for the signal current driving the complementary output FET's Q5 and Q6.

5.3 STRETCHER

The stretcher is a basic amplifier which expands the input signal over a period of time determined by the controlling logic and the RC time of the stretcher. The input differential dual transistor (Q9) is matched for maximum temperature stability. The output of Q9 feeds an emitter follower (Q15) for impedance matching. This feeds a voltage gain stage (Q14) which drives the stretch capacitor (200 pf). This capacitor then follows the rise of the input signal through Q14 and the diode in series with it. Once the peak is reached, the diode doesn't allow the capacitor to discharge through Q14. Instead it sees the high impedance of a FET (Q11) and a 68 megohm resistor, which allows the capacitor to discharge very slowly. Due to the fact that the RC time of the network is approximately 1000 times greater than the desired stretcher pulse width used, the output (TP2) remains at the input amplitude. After the output pulse, the stretcher pulse is discharged very quickly by Q13, controlled by the logic circuit. Q11, a source follower, presents the voltage across the stretcher capacitor to the output, while Q16 is a current source which supplies Q11 with a fixed current. The output of Q11 is fed through an emitter follower (Q12) to the output amplifier.

5.4 OUTPUT AMPLIFIER

This section is a basic closed loop amplifier. A differential dual transistor (Q31) is located at the input for maximum temperature stability. Located in the emitter of Q31 is a current source (Q33) used to provide a constant current and a high input impedance. The output of Q31 is then fed to a voltage gain stage (Q28, Q32) which in turn feeds a source follower (Q29). This then feeds a pair of

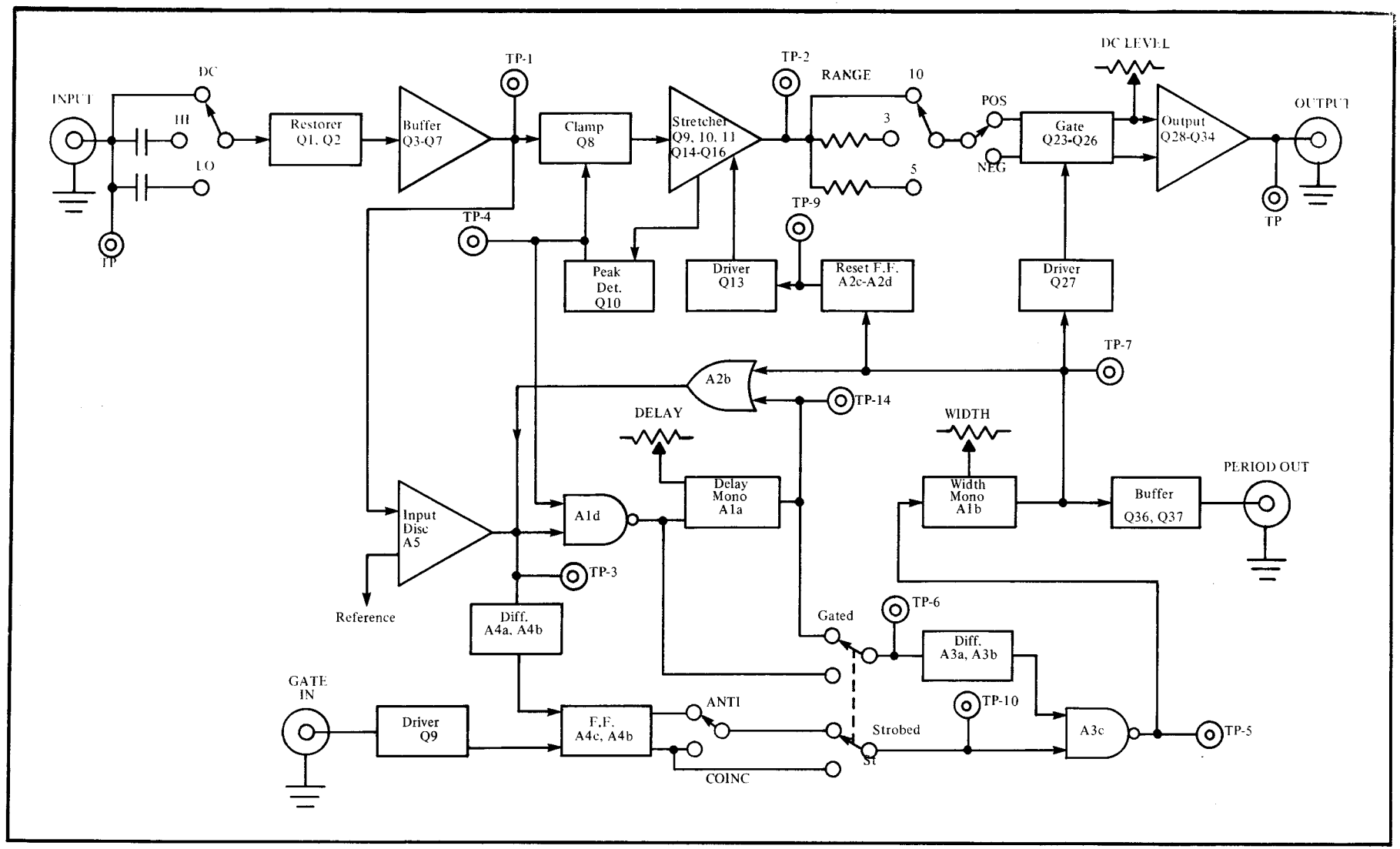


Figure 5-1. Block Diagram, Model 1454.

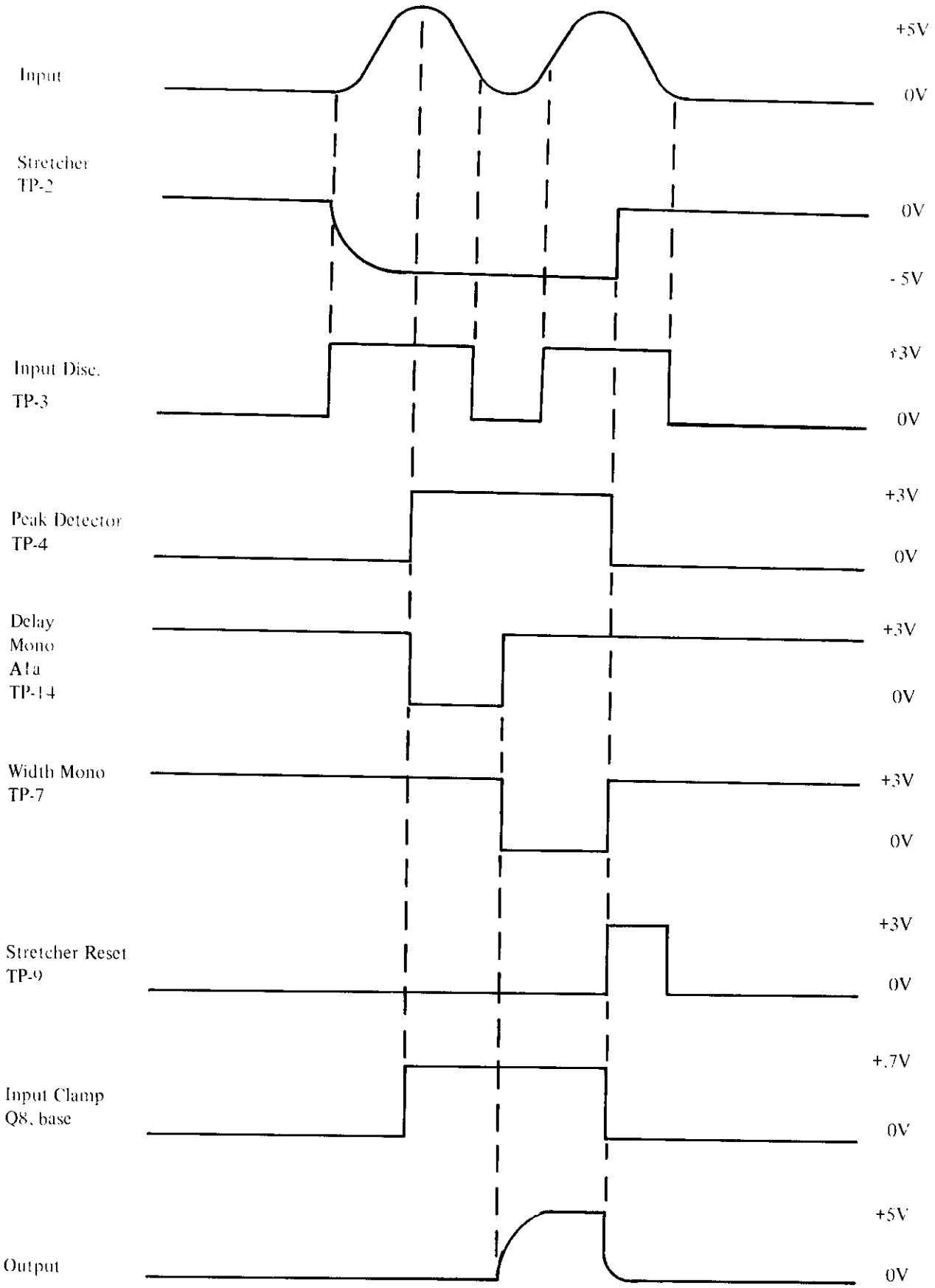


Figure 5-2. Waveforms for Piled-up Pulses.

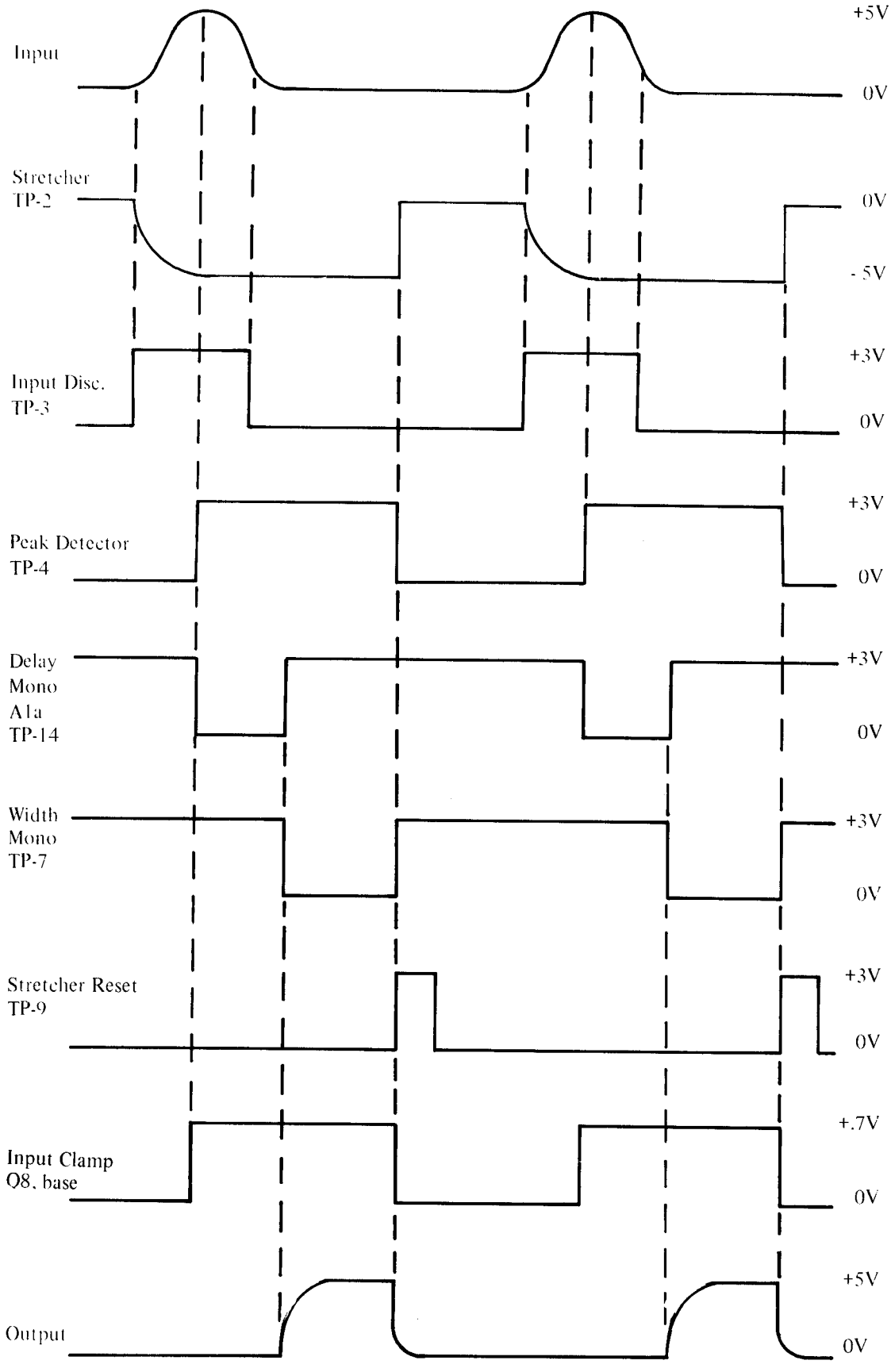


Figure 5-3. Waveforms for Two Valid Pulses.

complementary transistors (Q30, Q34) which provides fast switching and a low impedance for the output. The output is then fed back to the input through a resistor to provide a fixed gain. At the input to the amplifier, however, is located a three position Range switch, a Polarity switch, a DC level offset control, and a linear gate.

The Range switch does nothing more than change the input resistance to the amplifier, thereby changing the overall gain of the amplifier. This switch provides three output ranges of 10, 5, and 3 volts.

The Polarity switch takes the output of the stretcher and feeds it either to the inverting or non-inverting input. Thus a negative or positive signal can be obtained at the Output depending on the polarity selected. The DC Level control provides a DC voltage to the input which is fed to the output through the amplifier. This provides a DC offset voltage from - 2 Volts to +2 Volts at the output, depending on the setting of the DC Level control.

The Linear Gate is used to select a portion of the stretcher signal and present it to the output. This portion selected is controlled by the Logic control circuit. The gating transistors Q23 through Q26 are held in saturation with a negative voltage on the base. When in saturation, the signal to the amplifier is attenuated by approximately 2000 to 1 by transistor's saturation resistance, therefore, no output appears. When the transistors are turned off with a positive voltage, no attenuation takes place because of the high off resistance of the transistors. RV5 is used to balance the two input gates. Therefore it can be seen that the input to the Linear gate will control the time and the width of the output pulse while the stretcher controls the amplitude.

5.5 CONTROLLING LOGIC

The Controlling Logic can be broken into several sections. These are the discriminators, peak detector, and the gating circuit. All of these circuits combine to prevent random pulse interference, control the output pulse width, and also determine the time that the output appears. The input discriminator (A5, A1-c) provides a positive pulse (TP3) when the input signal exceeds the threshold voltage (100mVolt) determined by RV3. When the input signal passes its peak, it is detected by Q10 to give a positive pulse (TP4). These signals are combined in AND gate A1-d, triggering the Delay Monostable (A1a, Q20).

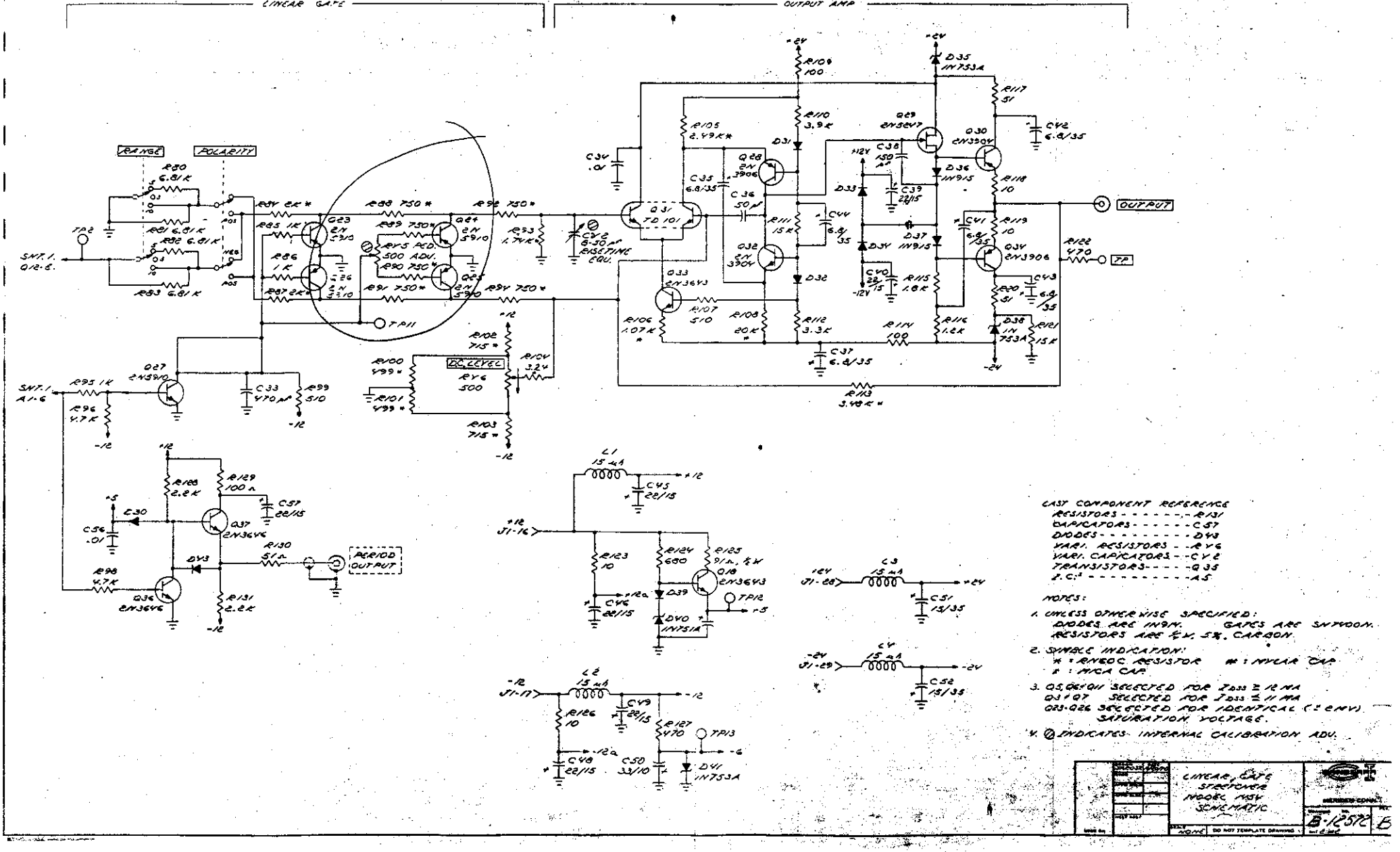
The discriminator pulse, differentiated in A4c, A4d, sets the Bistable A4a, A4b, (TP10). The output of the Bistable and the Delay Monostable are combined in AND gate A3c to provide the trigger pulse (TP5) to fire the Width Monostable (A1b, Q21). The Width (TP7) and Delay Monostables are ORed in A2b to clamp the input linear signal, during the stretcher time, by Q8 in the Stretcher amplifier. Also this signal holds AND gate A1d positive to prevent retriggering of the Delay Monostable by linear input signals occurring during the stretched time period.

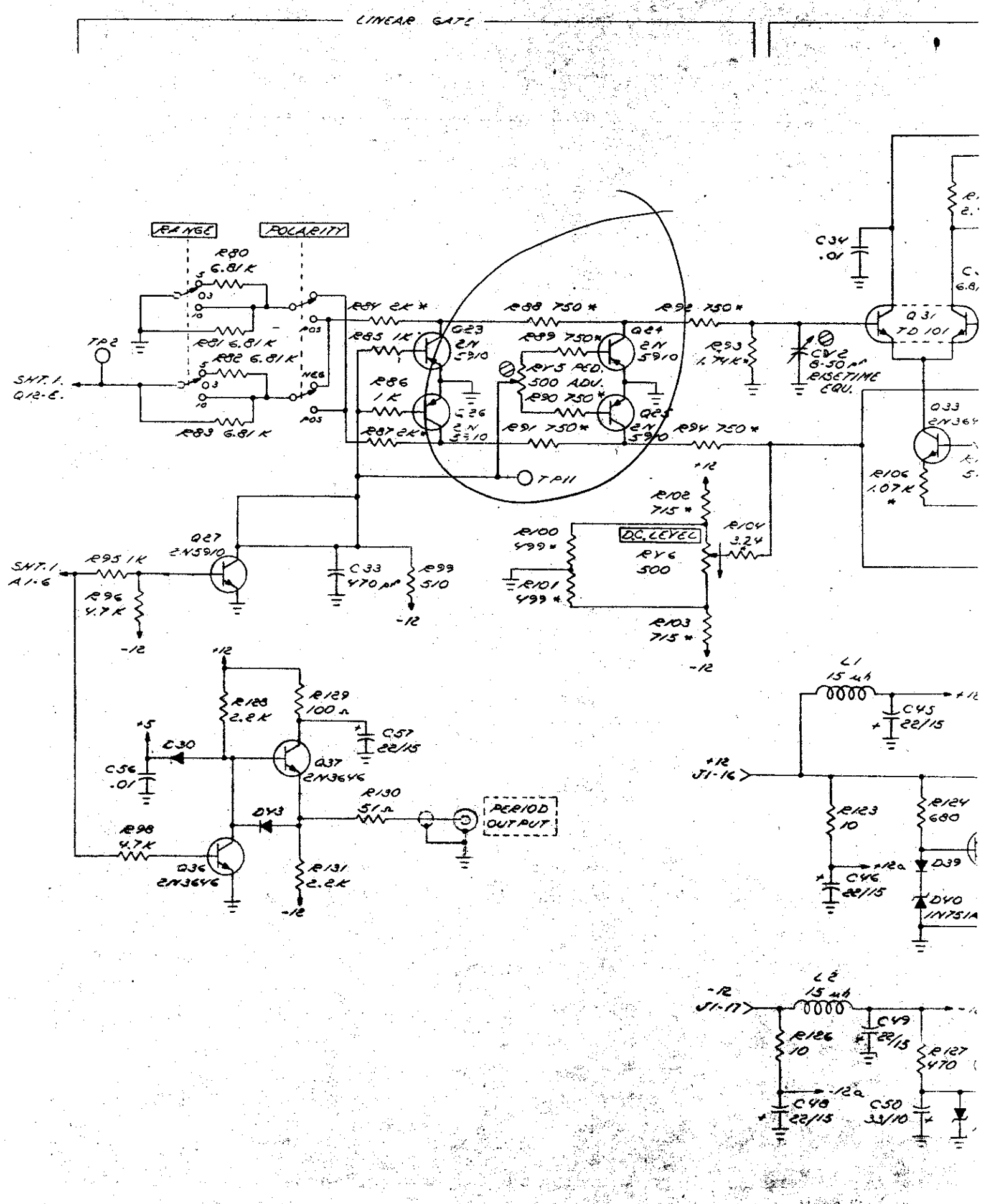
At the end of the Width Monostable, the Reset Monostable (A2a, Q22) is triggered resetting the Stretcher Amplifier to zero through A2c and Q13. If the input discriminator is still ON at the time of the Reset pulse, the Reset period is lengthened by A2d and A2c, so that the Stretcher amplifier follows the input signal to ground, preventing further outputs until the linear input signal recrosses the input discriminator. Small input signals, which do not trigger the input signal, are quickly returned to zero voltage by the reset current from the peak detector Q10, through R43 and Q13. During a valid input signal, this reset current is shunted to ground by Q17, which is driven from the output of A2b. If a gate signal occurs during the delay period, the output of Q19 resets the Bistable (A4a, A4b), preventing the trigger pulse to appear at TP5, and inhibiting the Width Monostable.

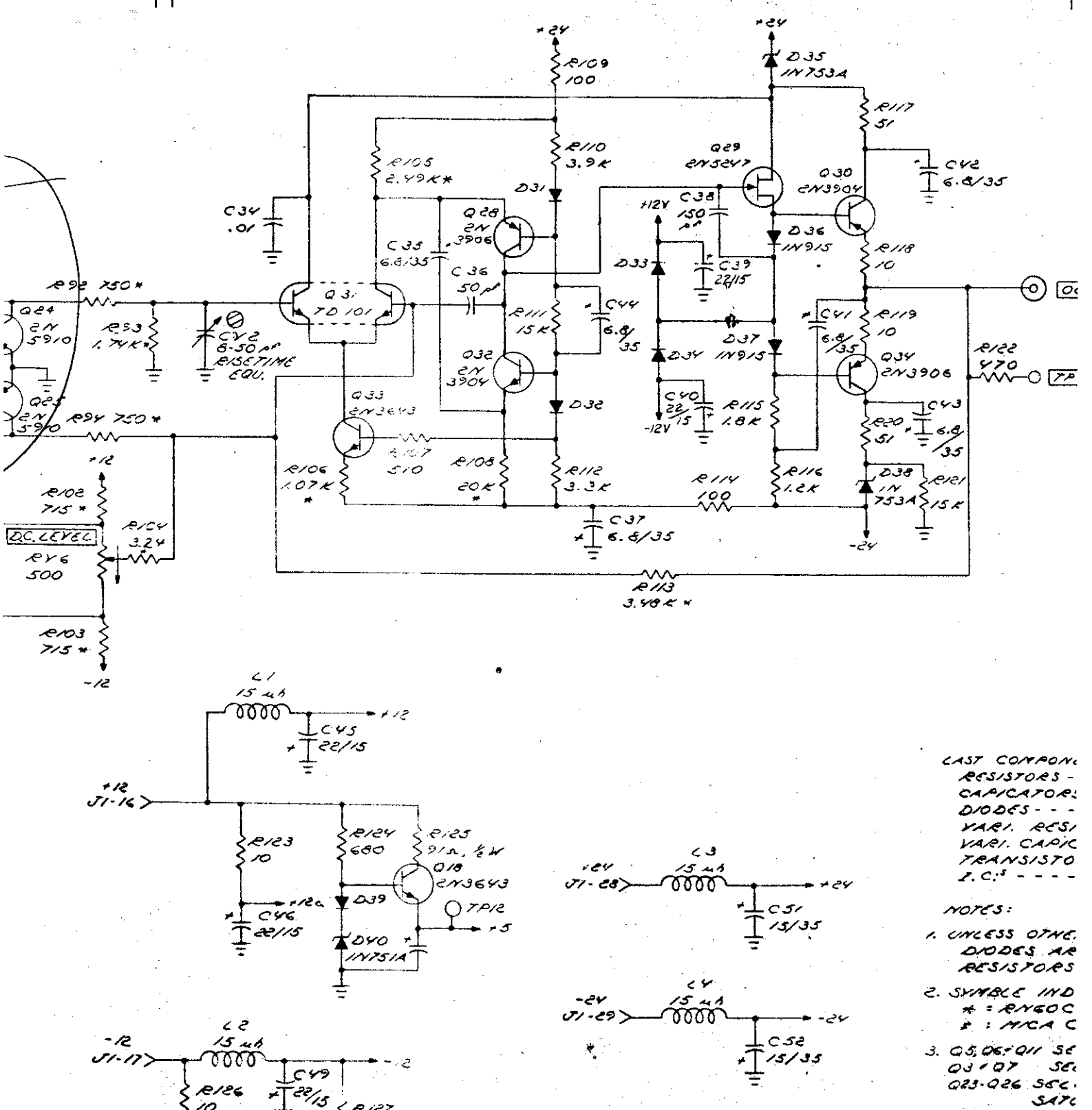
With the Gate Mode switch at COINC, the negative output of the Bistable is applied to the AND gate A3c, thus the Width Monostable is inhibited until a gate signal is received.

The Width Monostable opens the output gate, through Q27.

REV	CHANGE	ECN	BY	DATE	APPD
	INITIAL RELEASE	742	[illegible]	[illegible]	[illegible]
A	SEE ECN	762	[illegible]	[illegible]	[illegible]
B	SEE ECN	914	[illegible]	[illegible]	[illegible]




LINEAR GATE
RANGE
POLARITY
R80 6.81K
R81 6.81K
R82 6.81K
R83 6.81K
TP2
SHT. 1. Q12-E.
R84 2K *
R85 1K
R86 1K
R87 2K *
Q23 2N 5910
Q26 2N 5910
R88 750 *
R89 750 *
R90 750 *
R91 750 *
R92 750 *
R93 1.74K *
Q24 2N 5910
Q25 2N 5910
R95 FCD. 500 ADJ.
CV2 8-50 µµf RISETIME EQU.
Q31 TO 101
C34 .01
Q33 2N3640
R106 1.07K *
TP11
+12
R102 715 *
R100 499 *
R101 499 *
D.C. LEVEL
RV6 500
R104 3.24 K
R103 715 *
-12
Q27 2N5910
SHT. 1 A1-6
R95 1K
R96 4.7K
C33 470 µµf
R99 510
R128 2.8K
R129 100 Ω
C57 22/15
+5
C30
C56 .01
Q37 2N3646
R130 51 Ω
D43
PERIOD OUTPUT
R98 4.7K
Q36 2N3646
R131 2.2K
L1 15 µh
C45 22/15
J1-16
R123 10
R124 680
D39
C46 22/15
+12a
D40 IN751A
L2 15 µh
J1-17
C49 22/15
R126 10
R127 470
C48 22/15
-12a
C50 33/10

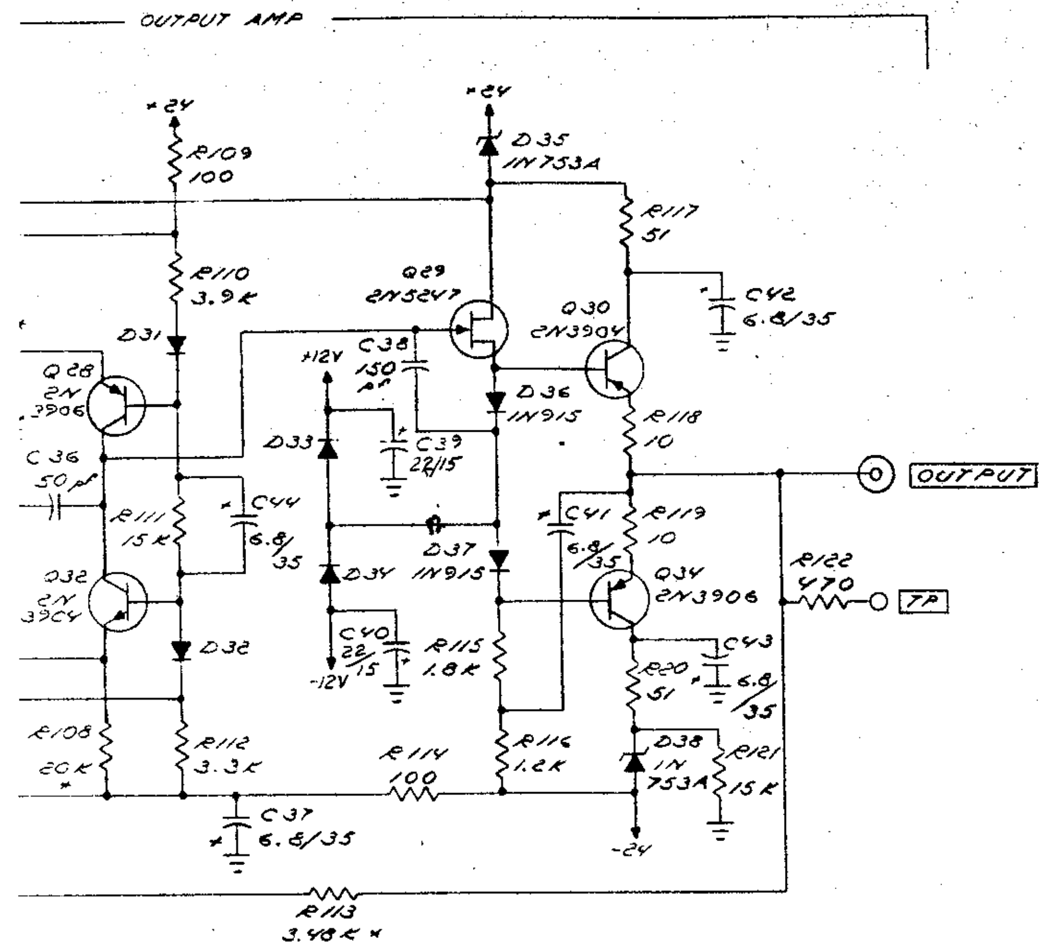


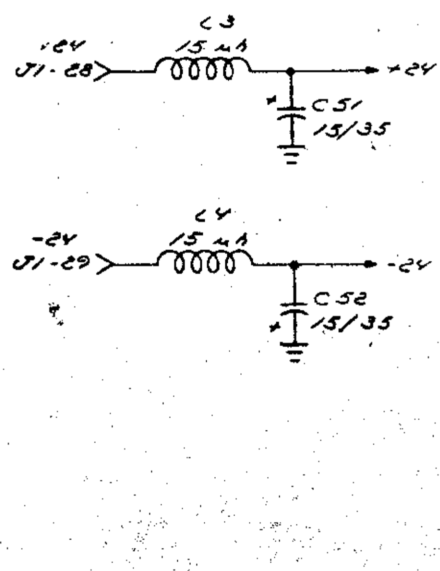
CAST COMPONE
RESISTORS -
CAPACATORS
DIODES - - -
VARI. RESI
VARI. CAPAC
TRANSISTO
I.C.'S - - - -

NOTES:

1. UNLESS OTHE
DIODES AR
RESISTORS
2. SYMBOLE IND
* = RN60C
# : MICA C
3. Q5, Q6; Q11 SE
Q3-Q7 SE
Q23-Q26 SEC
SAT
4. ⊘ INDICATES

REV	CHANGE	ECN	BY	DATE	APPD
	INITIAL RELEASE	742			
A	SEE ECN	762	J.C.N.		
B	SEE ECN	914	J.C.		



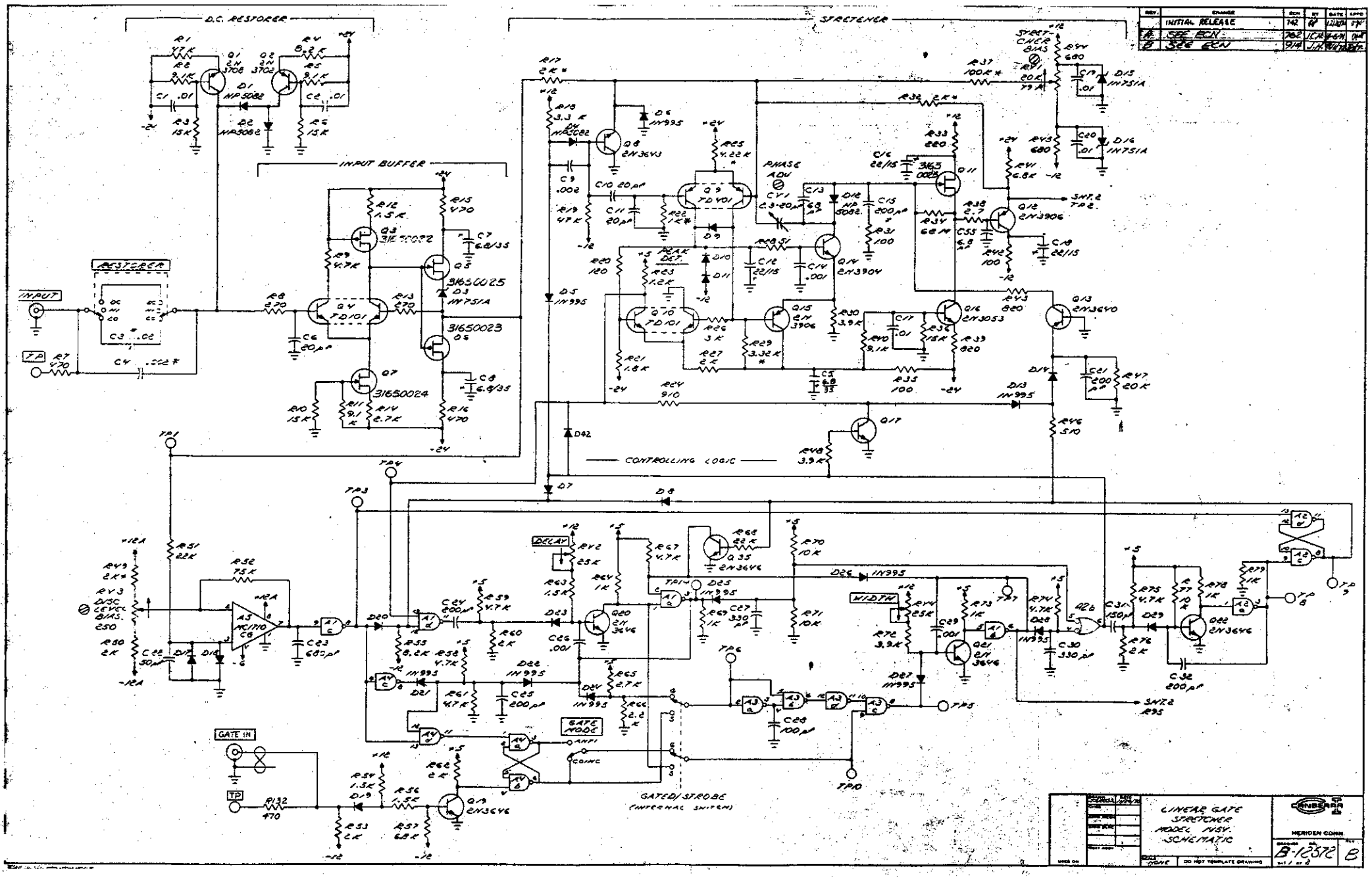


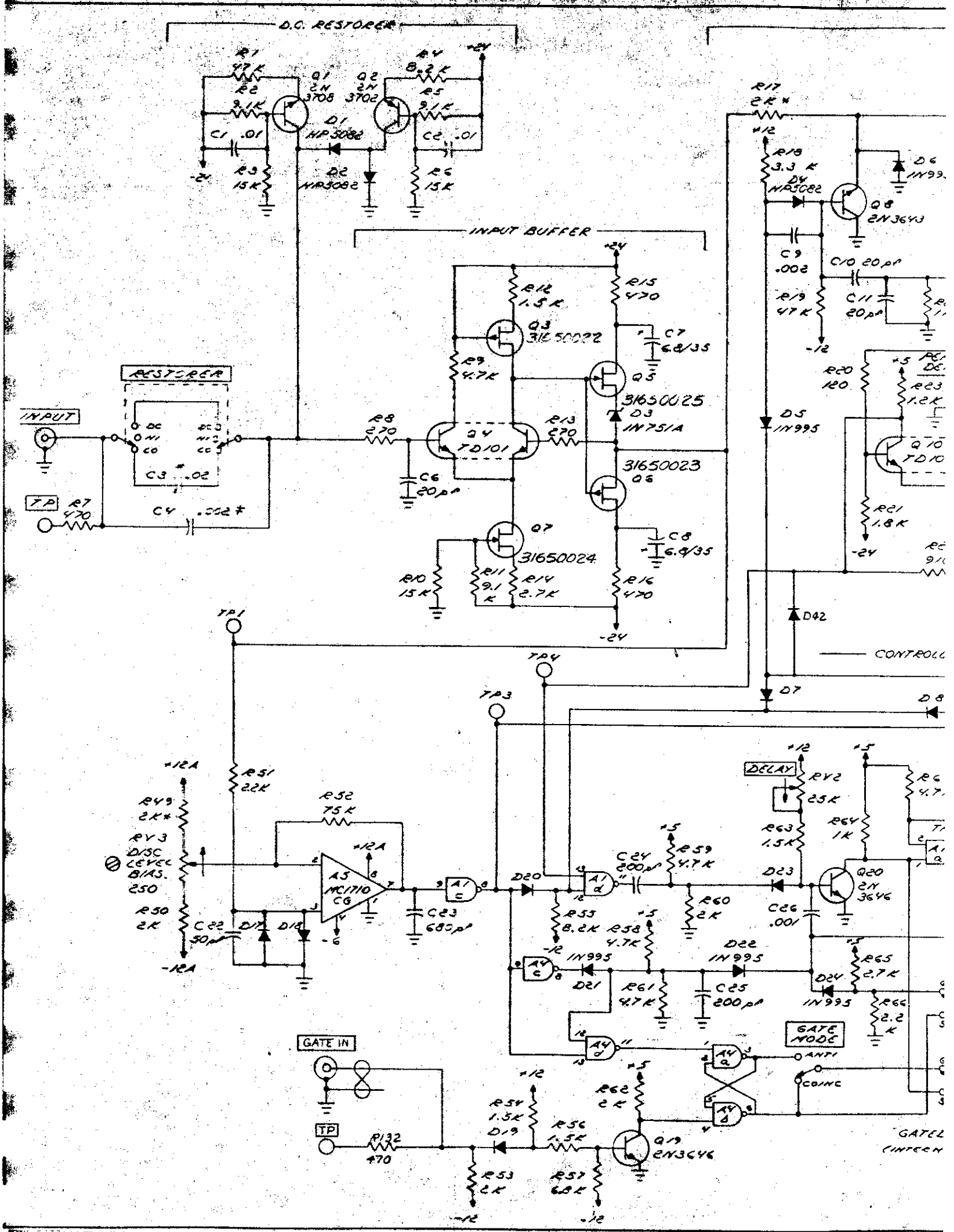
LAST COMPONENT REFERENCE
- RESISTORS - - - - - - - - R131
- CAPICATORS - - - - - - C57
- DIODES - - - - - - - - - D43
- VARI. RESISTORS - - RV6
- VARI. CAPICATORS - - CV2
- TRANSISTORS - - - - Q35
- I.C.'s - - - - - - - - - - A5

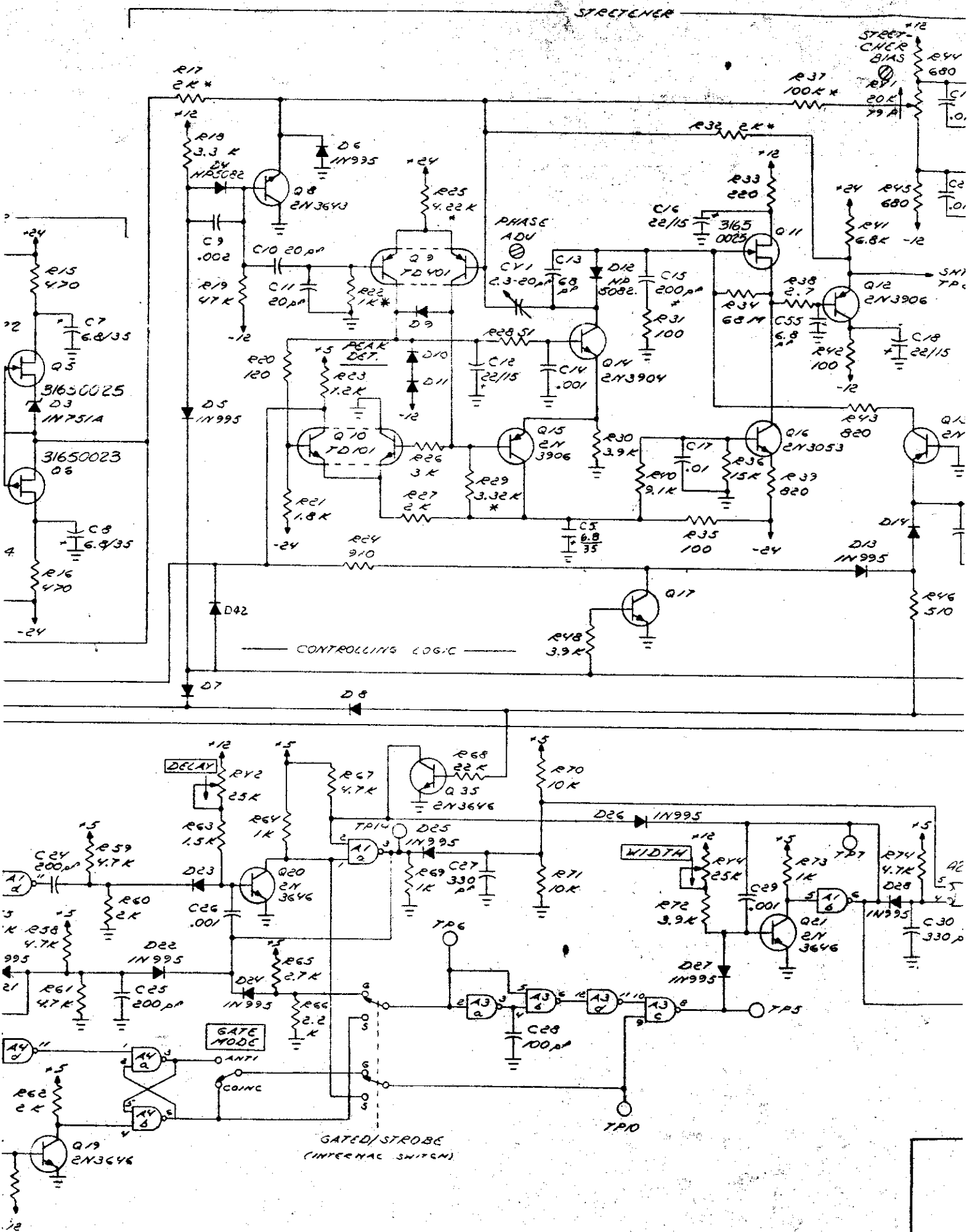
NOTES:

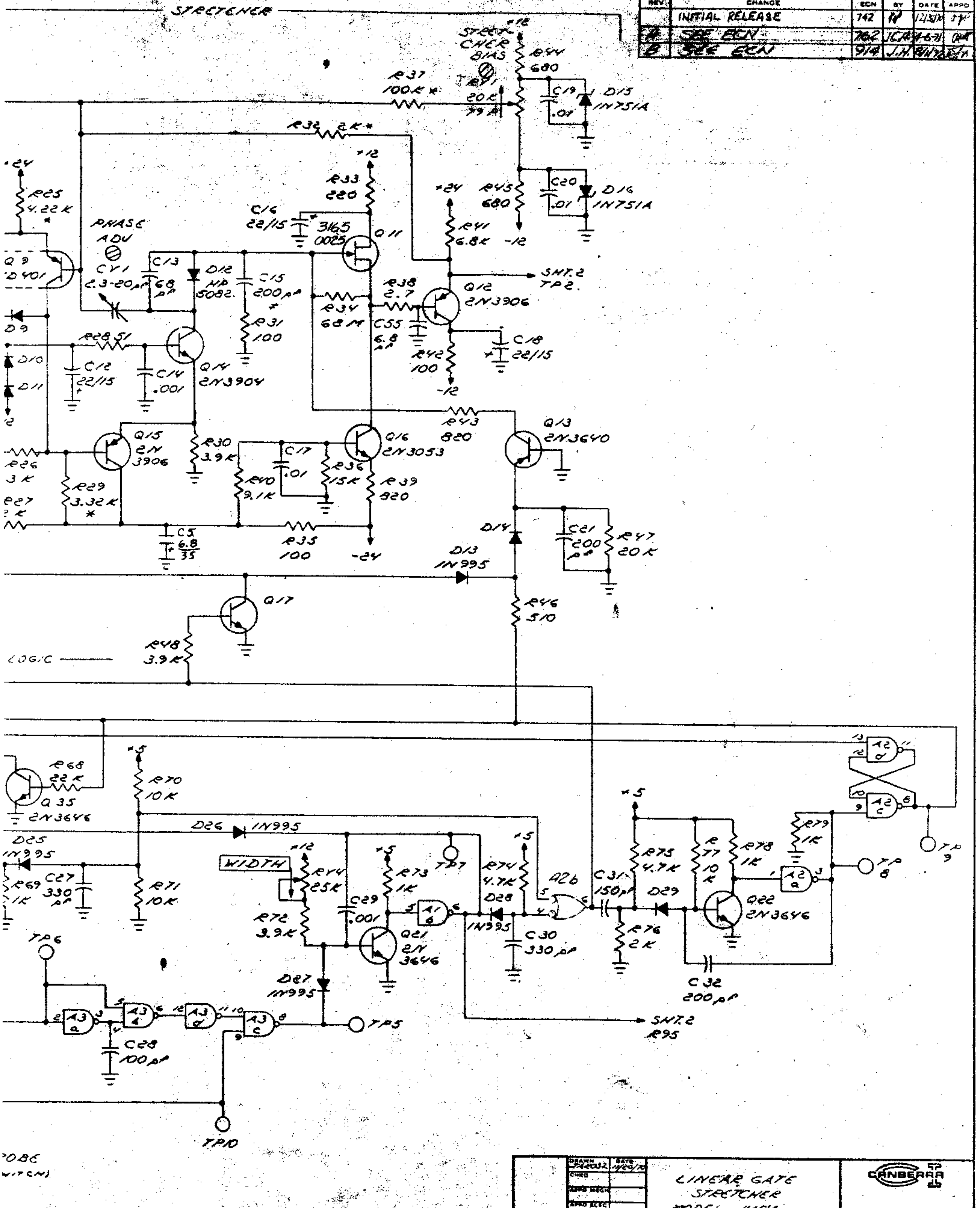
1. UNLESS OTHERWISE SPECIFIED:
   DIODES ARE 1N914. GATES ARE SN7400N.
   RESISTORS ARE ¼W, 5%, CARBON.
2. SYMBLE INDICATION:
   * : RN60C RESISTOR # : MYLAR CAP
   ≠ : MICA CAP
3. Q5, Q6 & Q11 SELECTED FOR IDSS ≥ 12 MA
   Q3 & Q7 SELECTED FOR IDSS ≤ 11 MA
   Q23-Q26 SELECTED FOR IDENTICAL (±2MV) SATURATION VOLTAGE.
4. ⊘ INDICATES INTERNAL CALIBRATION ADJ.

LINEAR, GATE STRETCHER MODEL 1454 SCHEMATIC	CANBERRA MERIDEN CONN.
SCALE NONE	DO NOT TEMPLATE DRAWING
DRAWING NO. B-12572	REV. B


D.C. RESTORER
STRETCHER
INPUT BUFFER
REGISTERS
INPUT
CONTROLLING LOGIC
PHASE ADV
PEAK DET.
DELAY
WIDTH
GATE IN
GATE MODE
ANTI
COINC
GATED/STROBE
(INTERNAL SWITCH)
LINEAR GATE STRETCHER MODEL 1454 SCHEMATIC
CANBERRA
MERIDEN CONN.
B-10572
B


D.C. RESTORER
INPUT BUFFER
RESTORER
INPUT
TP
GATE IN
DELAY
GATE MODE
ANTI
COINC
CONTROLL
GATEL
CINTECH


STRETCHER
STRETCHER BIAS
R17 2K *
R37 100K *
R32 2K *
R44 680
R19 3.3 K
D6 IN995
Q8 2N3643
D4 HP5082
R25 4.22K *
PHASE ADV
CV1 2.3-20pf
C16 22/15
3165 0025
Q11
R33 220
R45 680
R41 6.8K
-12
+24
+12
C9 .002
C10 20pf
C11 20pf
R19 47K
R22 1K *
Q9 TD401
C13 68pf
D12 ND 5082
C15 200pf *
R31 100
R38 2.7
Q12 2N3906
R34 68K
C55 6.8pf
R42 100
C18 22/15
R15 470
C7 6.8/35
Q5 31650025
D3 IN751A
Q4 31650023
C8 6.8/35
R16 470
-24
+5
PEAK DET.
R23 1.2K
D10
D11
R28 5K
C12 22/15
C14 .001
Q14 2N3904
R20 120
R21 1.8K
D5 IN995
Q10 TD101
R26 3K
Q15 2N3906
R29 3.32K *
R30 3.9K
C17 .01
Q16 2N3053
R36 15K
R33 820
R43 820
R40 9.1K
R27 2K
C5 6.8/35
R35 100
R24 910
D13 IN995
D14
R46 510
Q17
R48 3.9K
D42
CONTROLLING LOGIC
D7
D8
DELAY
RV2 25K
R67 4.7K
R68 22K
Q35 2N3646
R70 10K
D26 IN995
TP14
D25 IN995
R63 1.5K
R64 1K
C24 200pf
R59 4.7K
D23
Q20 2N3646
R60 2K
C26 .001
R69 1K
C27 330pf
R71 10K
WIDTH
RV4 25K
R73 1K
TP7
R74 4.7K
D28 IN995
C30 330pf
R72 3.9K
C29 .001
Q21 2N3646
D27 IN995
R58 4.7K
D22 IN995
R61 4.7K
C25 200pf
D24 IN995
R65 2.7K
R66 2.2K
TP6
TP5
C28 100pf
GATE MODE
ANTI
COINC
R62 2K
Q19 2N3646
TP10
GATED/STROBE (INTERNAL SWITCH)



REV	CHANGE	ECN	BY	DATE	APPD
	INITIAL RELEASE	742			
A	SEE ECN	762	JCA	4-6-71	
B	SEE ECN	914	J.N.		

LINEAR GATE STRETCHER MODEL 1454 SCHEMATIC

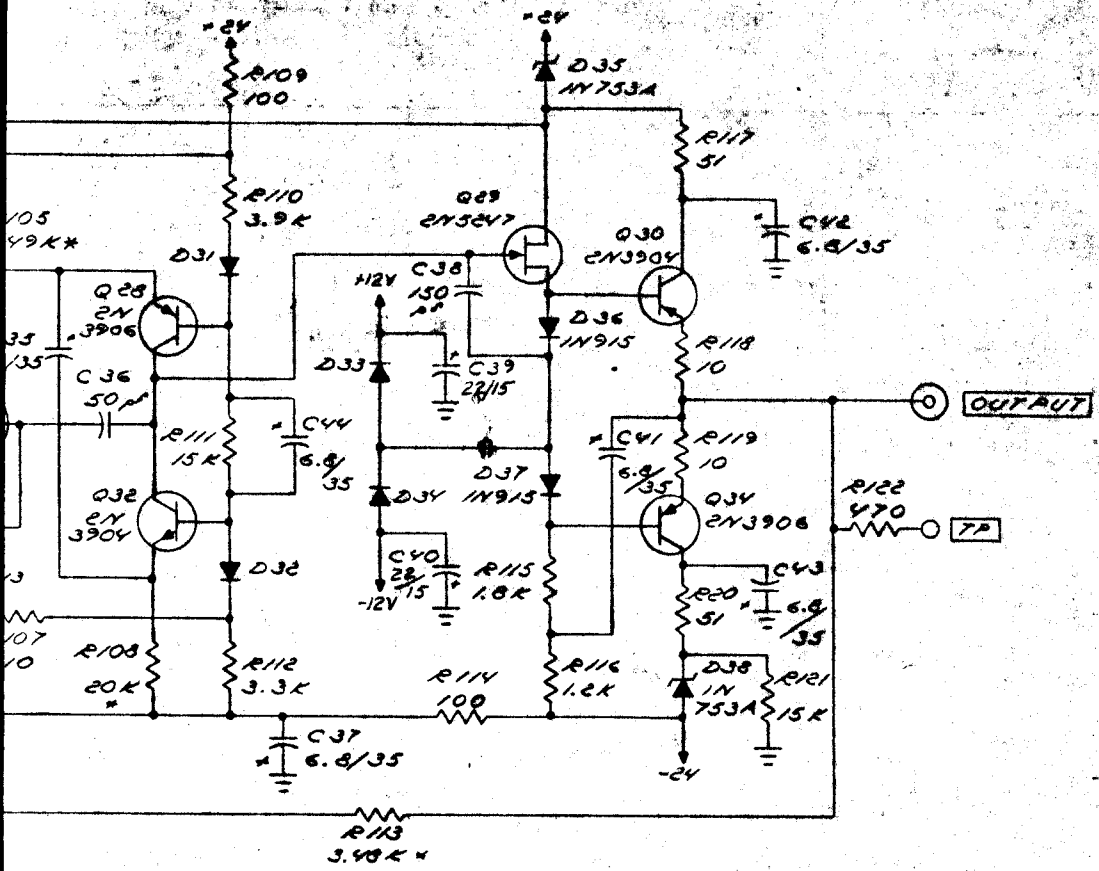
CANBERRA MERIDEN CONN.

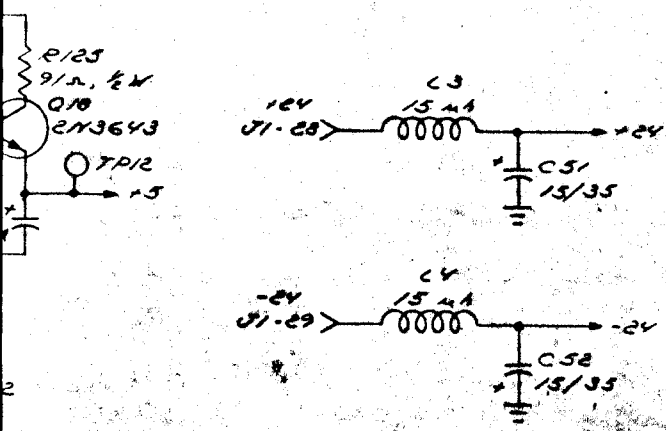
DRAWING NO. B-12572 REV B SHT 1 OF 2

SCALE NONE DO NOT TEMPLATE DRAWING

REV	CHANGE	ECN	BY	DATE	APPD
	INITIAL RELEASE	742	[illegible]	[illegible]	[illegible]

OUTPUT AMP





CAST COMPONENT REFERENCE

RESISTORS	R1XX
CAPACITORS	C5X
DIODES	D3X
VARI. RESISTORS	RV6
VARI. CAPACITORS	CV2
TRANSISTORS	Q3X
I.C.'S	A5

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   DIODES ARE IN914. GATES ARE SN7400N.
   RESISTORS ARE 1/4W, 5%, CARBON.
2. SYMBOL INDICATION:
   * = RNC60C RESISTOR ** = NYLAR CAP.
   # = MICA CAP.
3. Q5, Q6 - Q11 SELECTED FOR $I_{DSS} \geq 12$ MA
   Q3 - Q7 SELECTED FOR $I_{DSS} \geq 4$ MA
   Q23 - Q26 SELECTED FOR IDENTICAL (±2 mV) SATURATION VOLTAGE.
4. ⊘ INDICATES INTERNAL CALIBRATION ADJ.

	LINEAR, GATE SPECTROSCOPY AMPLIFIER SCHEMATIC		
DRAWN	DO NOT TEMPLATE DRAWING	1572	B

LINEAR GATE AND STRETCHER

Model 1454

CANBERRA INDUSTRIES, INC.
45 Gracey Avenue
Meriden, Connecticut 06450

Telephone: 203-238-2351

WARRANTY

canberra nuclear instruments

This equipment is warranteed by Canberra to be free from defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in this instruction manual. Repairs or replacement, at Canberra's option, will be made without charge at the Canberra plant during this warranty period. Except for the case of defects discovered upon initial operation, shipping expense to Canberra is to be paid by the customer; shipping expense to return the repaired equipment will be paid by Canberra.

Canberra reserves the right to modify its products without incurring the responsibility for modifying previously manufactured products.

Canberra does not assume any liability for the results of particular installations, as these circumstances are not in our control.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, notify Canberra and the carrier making delivery immediately, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in damage claims.

REPAIRS

Any Canberra instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. All such work will be done at the least possible expense to the customer. All equipment thus repaired or realigned will pass through our normal preshipment checkout procedure and will meet or surpass its original specifications when returned. Return shipping expense will, in this case, also be charged to the customer.

CANBERRA

CANBERRA INDUSTRIES, INC.
45 Gracey Avenue
Meriden, Connecticut 06450
Tel: 203-238-2351

At the time of this shipment a final manual was not available. Your name has been placed on our back-order list and a manual will be shipped to you shortly.

Thankyou

CANBERRA INDUSTRIES
45 Gracey Avenue
Meriden. Connecticut 06450

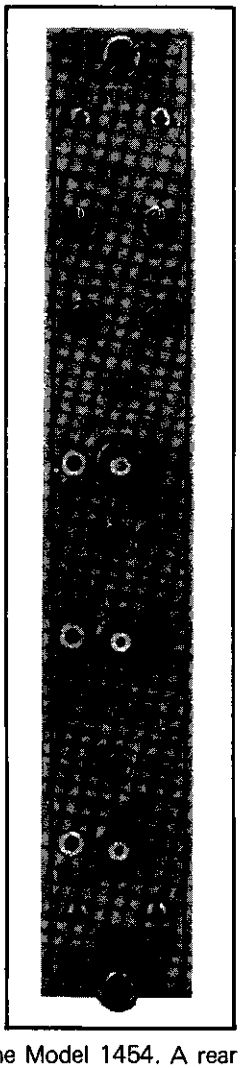
LINEAR GATE AND STRETCHER model 1454

CANBERRA

NUCLEAR ELECTRONICS

Features

- Linear Gate
- Pulse Stretcher
- Baseline Restorer
- Pileup Rejector
- Variable Linear Delay
- Variable Output Width



Description

The Canberra Model 1454 Linear Gate and Stretcher provides a standardized optimum shaped output for fuller utilization of the capabilities of a multichannel analyzer in high rate/high resolution nuclear spectroscopy. An extremely flexible module, the Model 1454 includes a pulse stretcher, DC coupled linear gate, DC restorer, and pulse pileup rejector.

The integral pulse stretcher portion of the Model 1454 compensates for the incompatibility of multichannel analyzers which have stringent requirements for input pulse shapes. All main amplifier pulses are converted to a standardized linear output pulse shape, variable in width (1-5μsec) and delay time (0.5μsec) via front panel controls. Rectangular in appearance, the linear stretched output is essentially flat topped with very little droop ($<$0.3mV/μsec). Thus, linearity of the succeeding MCA is improved where sharply peaked pulse shaping has been used in the main linear amplifier.

Total DC coupling, fast circuitry, baseline restoration, and pileup rejection all contribute to preserve spectral resolution at high count rates. The integral DC restorer permits the use of existing amplification systems in high rate experiments and increases the count rate capabilities of the Model 1454. Sophisticated pulse pileup rejection circuitry enhances high rate performance; after the input pulse has reached its peak, subsequent pulses are automatically inhibited until both the output pulse has terminated and the input recovered to the baseline.

A choice of externally gating or strobing the Model 1454 output is available, with Coincidence/Anticoincidence gated mode of operation. Therefore, analyzer overload may be minimized without requiring additional gating modules.

DC operation of the multichannel analyzer is essential for optimum count rate performance when using the Model 1454. A rear panel Period Output supplies the necessary logic information to enable DC operation of certain MCA's. Selectable output polarity and full scale output voltage range of 3, 5, or 10 volts ensures maximum MCA compatibility.

Specifications

INPUTS

SIGNAL INPUT - positive 0.1 to 10V unipolar or bipolar linear pulses; rise time $\geq$100 nanoseconds; width $\geq$300 nanoseconds; $Z_{in} \approx 250\ \Omega$ for 0.1V signal, $\geq$20K Ω over 1V; DC or DC restorer coupled

GATE INPUT - positive logic pulse or DC level, $\geq$3.5V ($\pm$20V max); width $\geq$100 nanoseconds; $Z_{in} \approx 2K\ \Omega$, DC coupled

OUTPUTS

SIGNAL OUTPUT - positive or negative 0.1 to 10V essentially flat topped rectangular pulse; rise time $\approx$0.5μsec; duration and delay as selected by front panel controls; DC offset variable from -2V to +2V; $Z_o \leq 0.1\ \Omega$, DC coupled

PERIOD OUT - +5V logic pulse, leading edge in time coincidence with Signal Output; duration essentially equal to Signal Output; Z_o=50 Ω, series-connected, DC coupled

Specifications (continued)

CONTROLS

POLARITY - front panel toggle switch to select either positive or negative output polarity, with respect to positive input

RANGE - front panel three position toggle switch to select either 3V, 5V, or 10V full scale output for +10V input signal

DELAY - front panel single-turn screwdriver adjust potentiometer to adjust Signal Output delay time from peak of input signal in GATED mode of control; 0.5 to $\geqslant$5 μsec range; acts as automatic reset in STROBE mode

WIDTH - front panel single-turn screwdriver adjust potentiometer to vary Signal Output pulse width; 1 to $\geqslant$5 μsec range

DC LEVEL - front panel 22-turn screwdriver adjust potentiometer to set the Signal Output baseline between $\pm$2V, in order to match the input DC offset level of the following DC coupled instrument

GATE MODE - front panel two position toggle switch to select COINCidence or ANTIcoincidence gated mode of operation; output is enabled (COINC) or inhibited (ANTI) upon receipt of a positive Gate Input signal (pulse or DC level) anytime between the beginning of the linear input signal and the start of the stretched output signal

COUNT RATE - front panel three position toggle switch to select DC or DC restorer coupling, HI and LO positions

GATED/STROBE - internal two position toggle switch to select GATED or STROBE mode of control; in GATED mode, a Gate Input signal controls output according to GATE MODE switch; in STROBE mode, output is inhibited until positive Strobe signal (only pulse inputs accepted) appears at the Gate Input connector; leading edge of Strobe pulse causes output in time coincidence; Strobe pulse must occur after peak of linear input signal; automatic reset in absence of Strobe pulse, variable 1 to 25μsec maximum

PERFORMANCE

INTEGRAL NONLINEARITY - $<\pm$0.05%, from 0.1 to 10V output for inputs with rise time $\geqslant$200 nanoseconds

STRETCHER DROOP - $<$0.3mV/ μsec

GATE FEEDTHROUGH - $<$0.05% of signal amplitude with gate closed

GATE PEDESTAL - essentially zero pedestal, factory calibrated

NOISE CONTRIBUTION - $<$20μV rms, referred to input

PILEUP REJECTION - after the input pulse has reached its peak, subsequent pulses are automatically inhibited until both the output pulse has terminated and the input recovered to the baseline

TEMPERATURE OPERATING RANGE - 0 to 50^{o}C

TEMPERATURE STABILITY - (1.) Output DC Level - $\leqslant$0.1mV/^{o}C; (2.) Gain $\leqslant$0.0075%/^{o}C

COUNT RATE STABILITY - $<$0.1% pulser peak shift at 80% of full scale when modulated by 0-80KHz of random Cs ^{137} with photopeak at 70% of full scale, using Model 1416 or 1417 amplifier with active filter time constant of 1 μsec unipolar

CONNECTORS

SIGNAL INPUT, SIGNAL OUTPUT, GATE INPUT - front panel, BNC, UG-1094/U

PERIOD OUT - rear panel, BNC, UG-1094/U

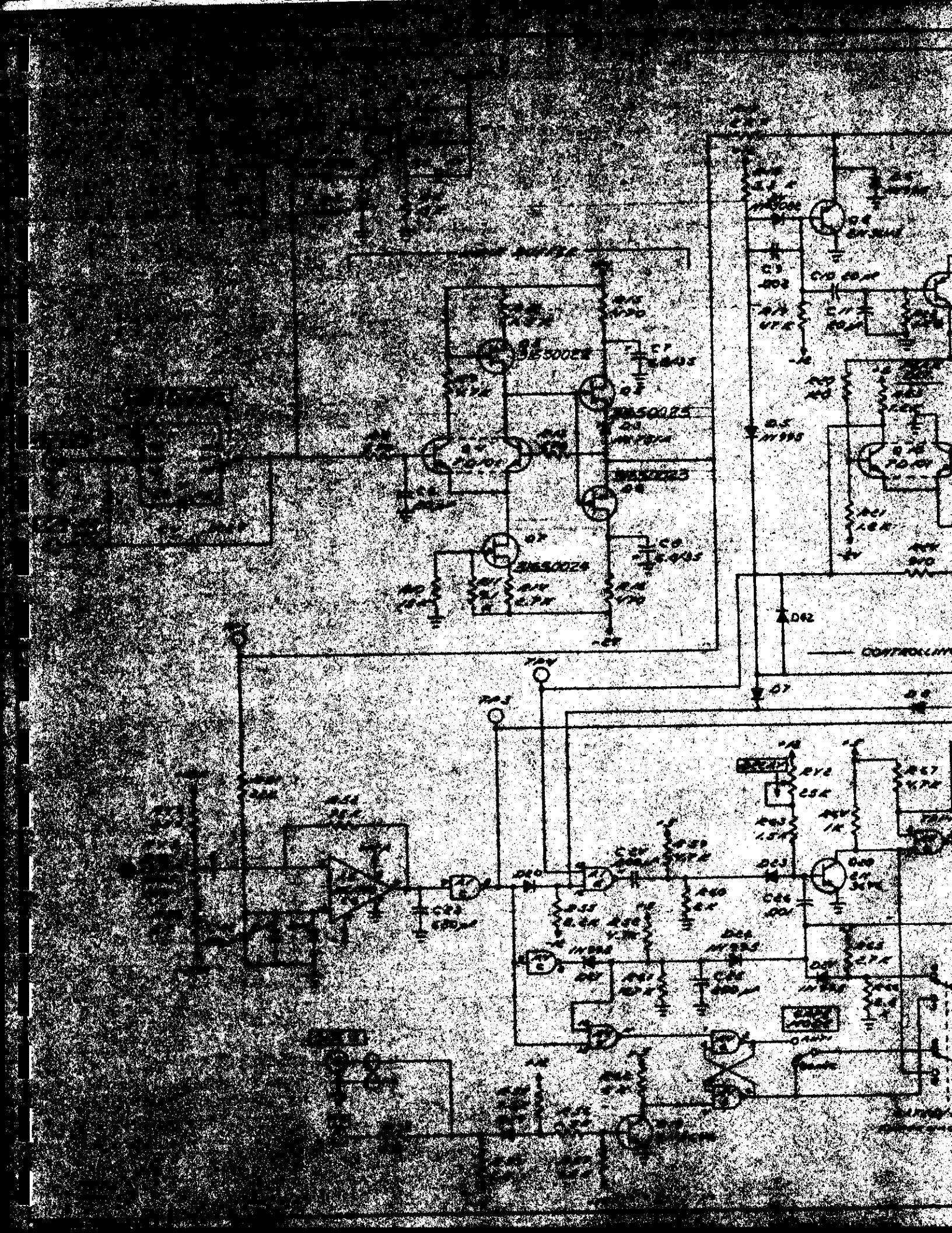
POWER

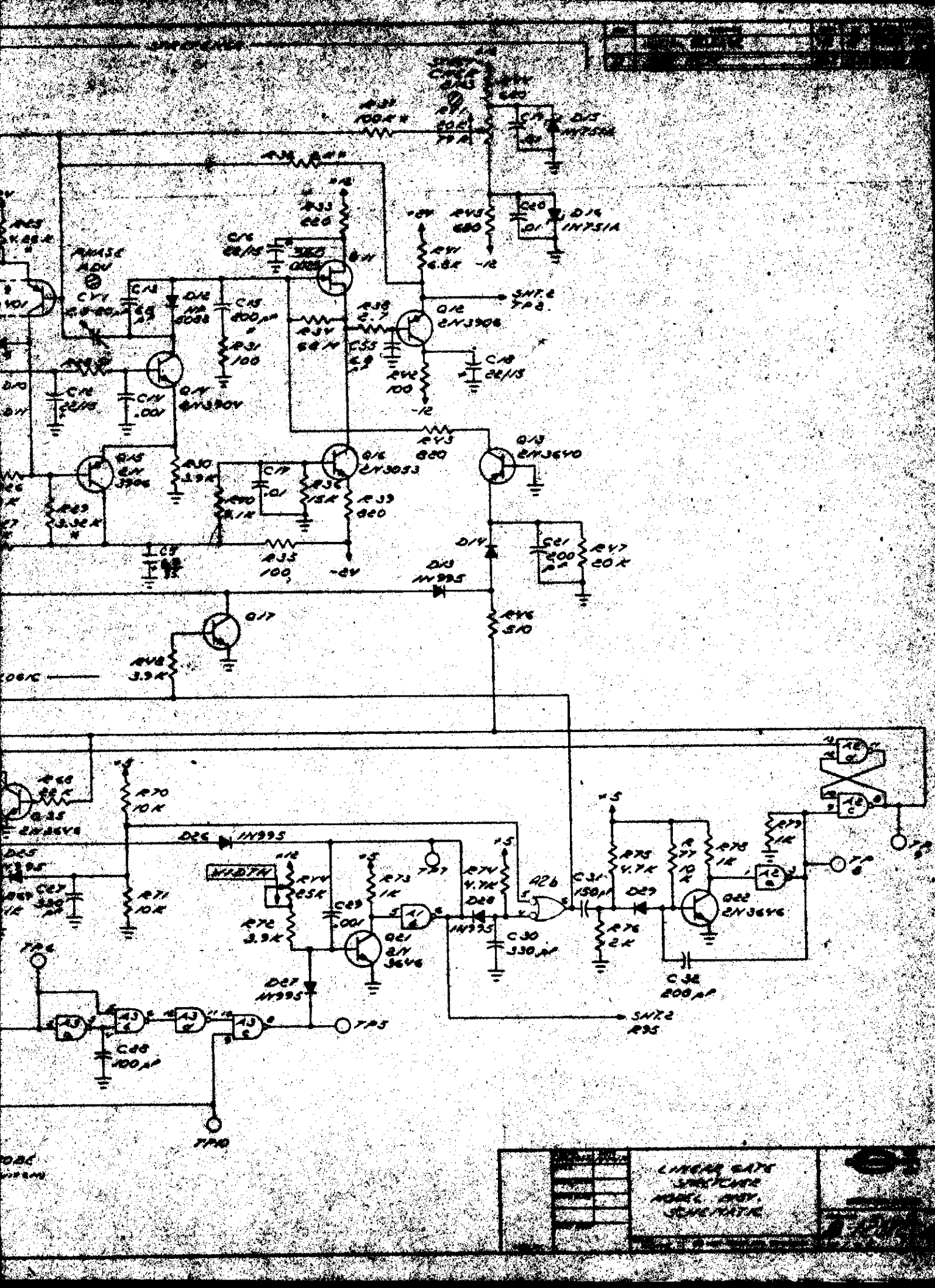
+24V	—	35mA	+12V	—	140mA
- 24V	—	60mA	- 12V	—	75mA

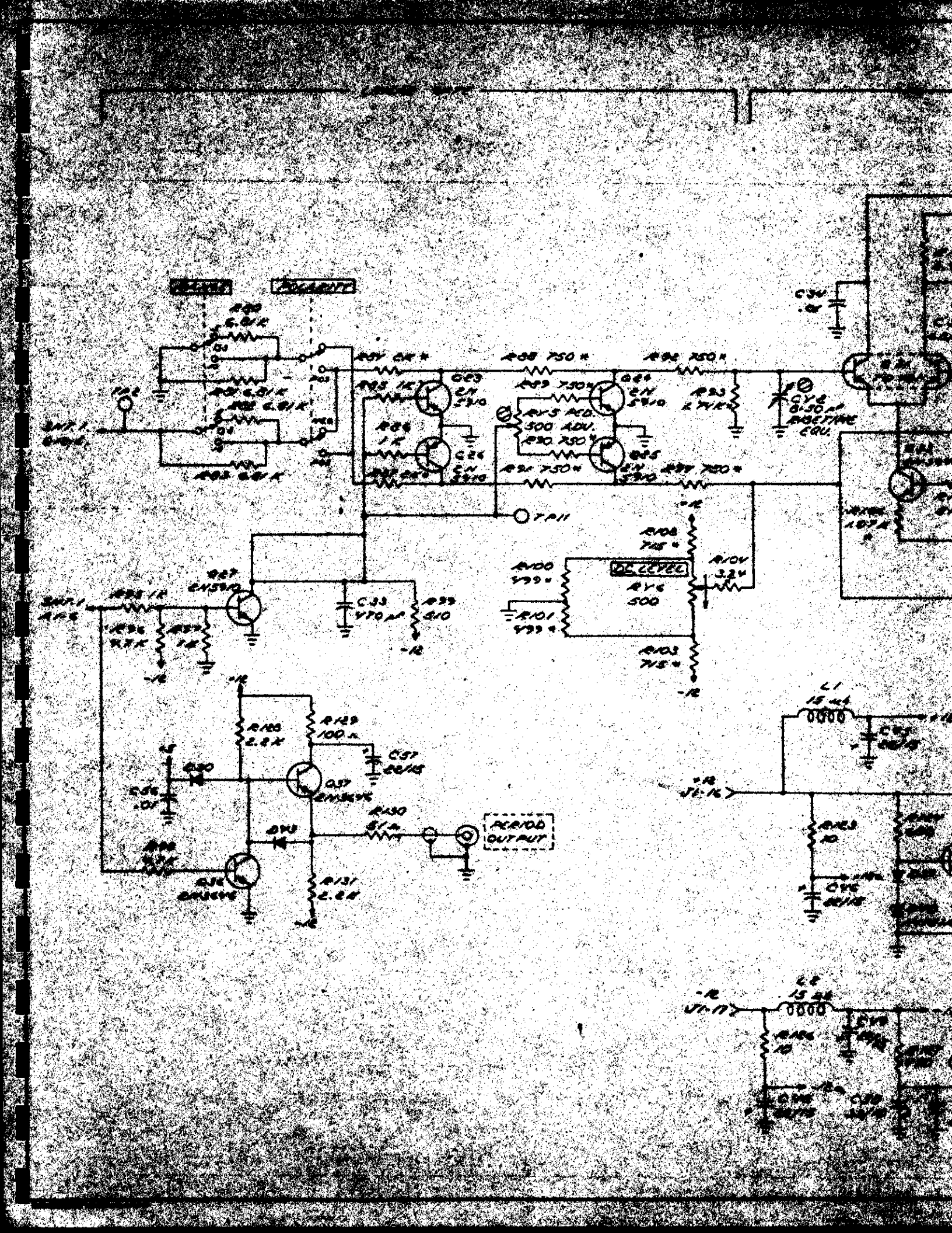
PHYSICAL

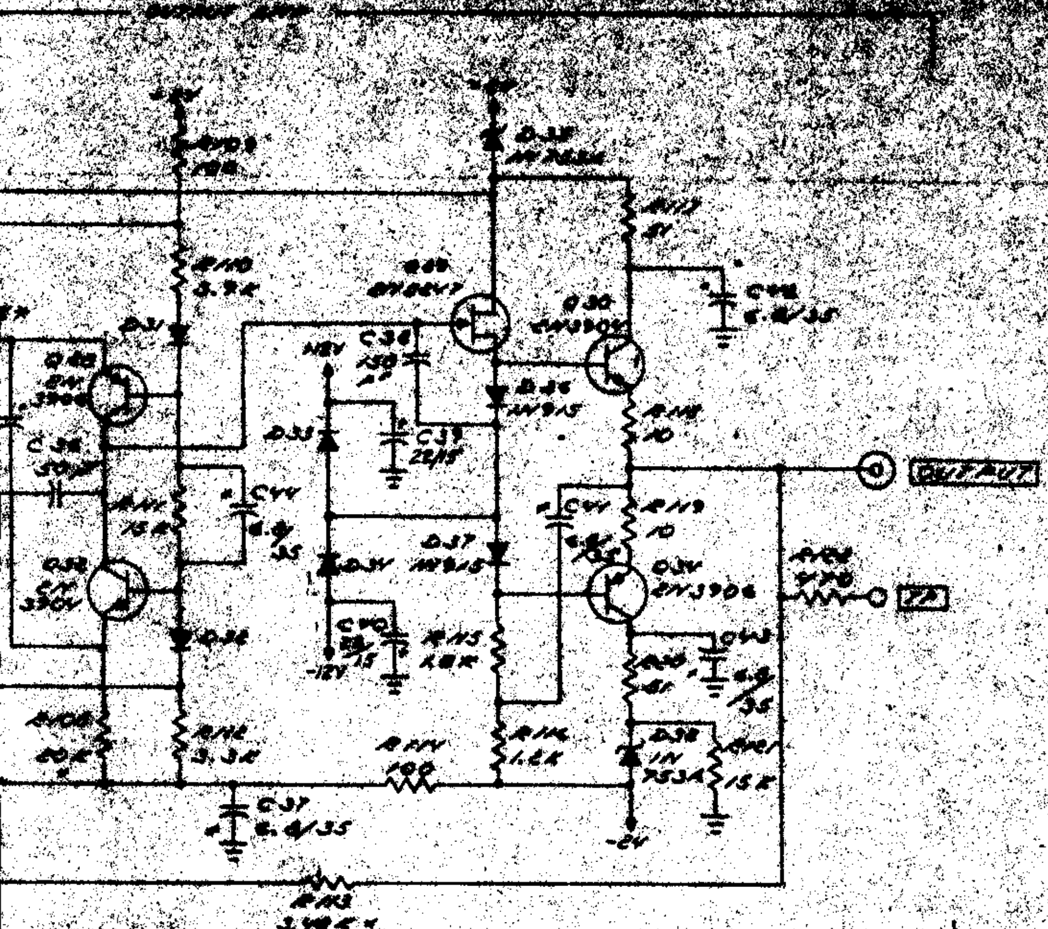
SIZE - standard single-width NIM module (1.35 x 8.714 inches) per TID-20893 (rev.)

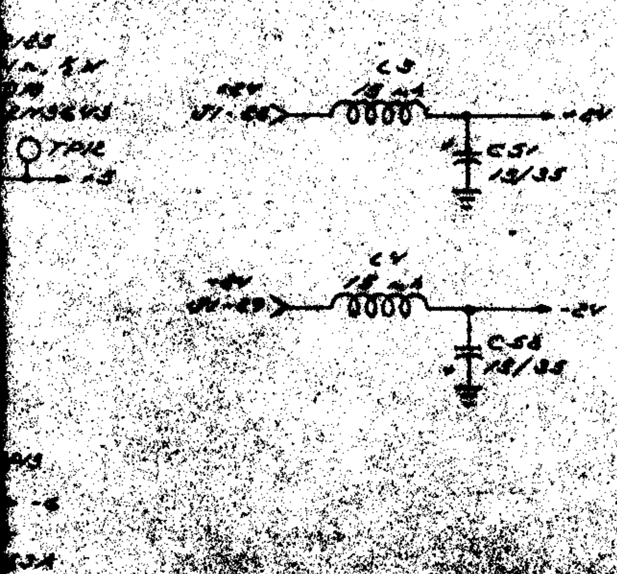
WEIGHT - 2.0 lb. (3.5 lb. shipping weight)




LINEAR GATE SYNCHRONIZER MONO. AMPL. SQUARE WAVE


AC/DC OUTPUT
DC ZERO ADJ.





LAST COMPONENT REFERENCE
RESISTORS - - - - - - - - R [illegible]
CAPACITORS - - - - - - C 57
DIODES - - - - - - - - - D [illegible]
VARI. RESISTORS - - R V [illegible]
VARI. CAPACITORS - - C V [illegible]
TRANSISTORS - - - - - Q 3[illegible]
I. C's - - - - - - - - - - A 5

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   DIODES ARE [illegible] CAPS ARE [illegible]
   RESISTORS ARE ¼ W, 5%, CARBON.
2. SYMBOL INDICATION:
   [illegible]
3. Q5, Q6, [illegible] SELECTED FOR [illegible]
   [illegible]
4. [illegible]