MODEL 8070/8070A

Instruction Manual
February, 1978

CONTENTS

APPENDICES

SECTION 2
SPECIFICATIONS

2.1 INPUTS

ANALOG INPUT	DC coupled; Positive Unipolar, bipolar or positive DC level; 0 to 10V Risetime 0.25 to 30μsec (longer on request) Width 1μsec minimum Input impedance 1.35k Front and Rear panel BNC's Front panel test point
GATE INPUT	Positive logic; pulse or DC level; 2.5 to 7V; width $>$ 100n.s. DC coupled Front and Rear Panel BNC's Front Panel test point

2.2 OUTPUTS

DATA	25 pin Amphenol connector containing signals to memory unit. Compatible with all Canberra and Geoscience storage units
STABILIZER	25 pin Amphenol connector containing signals to parallel input stabilizer such as Canberra Model 8200.
SYSTEM BUSY	Logic Pulse indicates ADC Busy; Logic 1=+4V; Logic 0=0V
SCA	Logic pulse operating on ADC input signal; Output independent of ADC; width $\approx$ 0.5μsec Logic 1: +5V unterminated (normal) +8V unterminated (optional with internal jumper) Logic 0: 0V Z out $\approx$ 51 ohms Front and Rear Panel BNC's; Front Panel test point

2.3 CONTROLS

POWER	Front locking toggle; applies AC power to unit
DIGITAL BASELINE	8 Toggle switches to provide suppression of digital zero; 0 to 8160 in multiples of 32 channels. With conversion gains of 256 and 512, the Digital offset equals the switch setting times 1/4 or 1/2 respectively

GAIN	Six position rotary switch to select full scale resolution of input; selection of 256, 512, 1024, 2048, 4096 or 8192 channels/+10 volt input
RANGE (OVERFLOW)	Six position rotary switch to select full scale addresses of memory group assigned to ADC; selection of 256, 512, 1024, 2048, 4096 or 8192
GATE	Two position toggle switch to select coincidence or Anti-coincidence operation. With no input connected to the Gate in BNC, analysis will be enabled in either position of the switch (Anti or Coinc). If a Coincidence signal is connected, a positive pulse during the Linear Gate Time is necessary to enable conversion: this is called "late" coincidence. In the ANTI position, gating occurs at the time the input signal rises through the LLD crossing (Early). Internal jumpers can be changed to cause coincidence gating to occur on the LLD crossing (Early). Another internal jumper allows analog sampling during the gate time
ANALOG BASELINE(ZERO INTERCEPT)	Ten-turn lockable potentiometer to vary analog zero; Range ± 6% of input range; resolution and resetability < 0.005% of full scale
LOWER LEVEL DISCRIMINATOR (LLD)	Ten-turn lockable potentiometer sets lower limit of ADC and SCA window; 0 to 100% of range Linearity not affected to within 10mV of LLD setting Resolution and resetability < 0.05%
UPPER LEVEL DISCRIMINATOR (ULD)	Ten-turn lockable potentiometer sets upper limit of ADC and SCA window; 0 to 100% of range Resolution and resetability < 0.05%

2.4 INDICATORS

POWER	AC power lamp
CONVERSION	13 LED lamps to indicate converted value
OVERFLOW	LED lamp to indicate overflow conversion (ULD or Range)
INVALID	LED lamp to indicate invalid conversion (Activated for overflow and underflow conditions or gate inputs without recognized analog inputs.)

DEAD TIME METER	Front panel meter indication of average percentage of time the ADC is busy

2.5 PERFORMANCE

2.5.1 ADC

CONVERSION TIME	$2.5 + 0.02\,(n + x)\,\mu$sec (50MHz) $2.5 + 0.01\,(n + x)\,\mu$sec (100MHz) *where*: n=Address x=Effective Digital Baseline [with conversion gains of 256 and 512 the (n + x) value is multiplied by 4 and 2 respectively]
LINEAR GATE TIME	Constant fraction circuitry closes gate after peak roll-over ($\approx$ 90% of Peak)
ADC DEAD TIME	Linear Gate Time + Conversion Time + Memory Cycle Time
INTEGRAL NON-LINEARITY	$<$ ± 0.025% over top 99% of full scale range
DIFFERENTIAL NON-LINEARITY	$<$ ± 0.75% over top 99% of range
DRIFT	GAIN: $<$ ± 0.005% of full scale/1°C ZERO; $<$ ± 0.005% of full scale/1°C LONG TERM: $<$ ± 0.01% of full scale per 24 hours at constant temperature
PEAK SHIFT	$<$ ± 0.025% of full scale at rates to 50KHz
CHANNEL PROFILE	On 8192 gain, flat over $>$ 80% of channel width. On other gains, flat over a minimum of 90% of channel width
AUTOMATIC RELEASE	Internal logic prevents system lock-up; ADC is reset if converted data is not accepted within $\approx$ 10ms by the memory

2.5.2 SCA

TIMING	Output pulse generated when input pulse falls through LLD setting
INTEGRAL NON-LINEARITY	$<$ ± 0.25% of full scale

DRIFT (LLD or ULD)	$<\pm$ 0.05% of full scale/^{o}C $<\pm$ 0.01% of full scale per 24 hours at constant temperature
OFFSET (from ADC window)	$<$ 0.5% of full scale
PULSE PAIR RESOLUTION	$<$ 1μsec

2.6 CONNECTOR TYPES

2.6.1 FRONT PANEL

INPUT	BNC (Isolated), KC-70-67
SCA OUTPUT	BNC, UG-1094/U
GATE	BNC, UG-1094/U

2.6.2 REAR PANEL

DATA (J101)	Amphenol type 17-10250-1
STABILIZER (J102)	Amphenol type 17-10250-1
INPUT	BNC (Isolated), KC-79-67
SYSTEM BUSY	BNC, UG-1094/U
GATE	BNC, UG-1094/U
SCA	BNC, UG-1094/U

2.7 POWER REQUIREMENTS

105 to 125 VAC/200 to 250 VAC (switch selectable);
50 to 400Hz approximately 25 watts

2.8 PHYSICAL

SIZE	Standard 19" rack mount; 3-1/2" high x 19" wide x 18" deep
WEIGHT	Net weight $\approx$ 20 lbs. (9 kg) Shipping weight $\approx$ 35 lbs. (15.8 kg)
OPERATING TEMPERATURE	0 to 45^{o}C with adequate air flow

2.9 CABLES

(1) Four foot cable for connection to Canberra Memory Unit

SECTION 3
CONTROLS, INDICATORS, ADJUSTMENTS AND CONNECTORS

3.1 GENERAL

Complete understanding of the purpose of the various controls and connectors is required for the proper operation of the Model 8070, and it is recommended that this section be read before proceeding with the operation of the instrument.

3.2 FRONT PANEL (Refer to Figure 3-1)

3.3 REAR PANEL (Refer to Fig. 3-2)

3.4 INTERNAL (Refer to Figs. 3-3 & 3-4)

NOTE: All internal adjustments are factory aligned

3.4.1 BOARD # 1 (ADC)

EARLY/LATE COINCIDENCE	The ADC has provision for Early or Late Coincidence. The Model 8070 is shipped with the internal jumper set for Late Coincidence (K to L). To change to Early Coincidence, move jumper wire to connect K to E
ADC SAMPLE	The ADC can be used to sample a DC or slowly changing AC voltage. To do this requires the Early Coincidence position (see EARLY/LATE COINCIDENCE jumpers), the sample jumper J1 inserted, and removing diode D28 located across socket pins Q and P. The jumper *must* be removed and diode re-installed for pulse height analysis
RAMP ADJUST (RV1)	Ramp constant current source adjustment. Aligns ramp slope
SCA REFERENCE (RV2)	Adjustment for LLD & ULD max reference voltages
METER ADJUST (RV3)	Dead Time Meter calibration
DISC. ZERO ADJ. (RV4)	Offset adjustment for LLD & ULD min reference voltages

3.4.2 BOARD # 2 (ADC INTERFACE)

POWER SUPPLIES (PLUGS)	Jumpers which connect the individual supplies to the circuitry
12/28V ADJUST (RV1)	Adjustment for ± 12 and ± 28 volt supplies
5V ADJUST (RV2)	Adjustment for ± 5 volt power supply

POWER
Locking toggle switch which provides AC power to the unit.

POWER INDICATOR
Amber neon lamp which indicates AC power on.

OVFL
LED lamp to indicate an ADC rejection due to a range or ULD overflow.

INV
LED lamp to indicate invalid conversion. The invalid lamp is activated for conversions which do not exceed the digital offset or for gate inputs without recognized analog inputs. Any overflow condition also activates the invalid lamp.

ADC CONVERSION INDICATORS DATA
13 LED lamps which indicate the binary data of the last conversion.

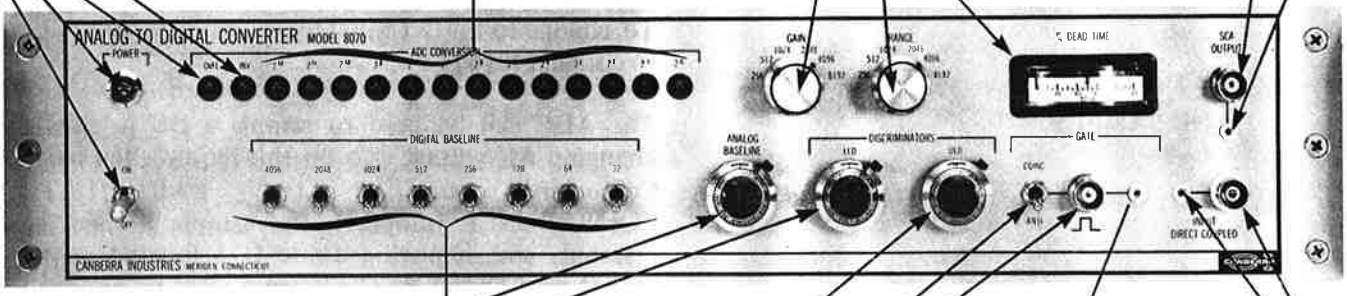
RANGE
Six position rotary switch to select the full scale address of the ADC memory group. The Range setting determines the digital overflow and should correspond to the memory size used. Settings are 256, 512, 1024, 2048, 4096 and 8192.

GAIN
Six position rotary switch to select full scale resolution of input. Gain settings are 256, 512, 1024, 2048, 4096 or 8192 channels per 10V input.

DEAD TIME METER
Indication of average percentage of time the ADC is busy.

SCA TP
Test point for monitoring SCA output.

SCA OUTPUT
Logic pulse operating on the ADC input signal independent of ADC dead time.



DIGITAL BASELINE
8 toggle switches to provide suppression of digital zero. The range of digital offset is 0 to 8160 in multiples of 32 channels. With conversion gains of 256 and 512, the Digital offset equals the switch settings times 1/4 and 1/2 respectively.

ANALOG BASELINE
10-turn locking pot which varies the reference level relative to the level of the input signal. This control is factory set to put zero energy into channel zero of the memory at a reading of ≈5.0 (sec tag attached to unit).

LLD DISCRIMINATOR
Ten turn lockable potentiometer which sets the lower limit of the ADC and SCA window. Inputs falling below the LLD setting will not be accepted by the ADC nor produce an SCA output. The LLD Discriminator has an effective range of 0 to 110% of full scale (10V).

ULD DISCRIMINATOR
Ten turn lockable potentiometer which sets the upper limit of the ADC and SCA window. Inputs exceeding the ULD setting will be rejected by the ADC and an overflow condition will result. The SCA will also sense the ULD crossing and not produce an output. The ULD Discriminator has an effective range of 0 to 110% of full scale (10V).

GATE INPUT
Accepts positive gating pulses for coincidence or anticoincidence operation. With no input connected to the Gate In BNC, analysis will always be enabled.

GATE
Two position toggle switch used to select coincidence or anticoincidence operation.

GATE TP
Test point for monitoring gate input.

INPUT TP
Test point for monitoring analog input.

INPUT
Positive DC coupled signal to ADC and SCA; 0 to 10V.

Figure 3-1
Front Panel, Model 8070/8070A

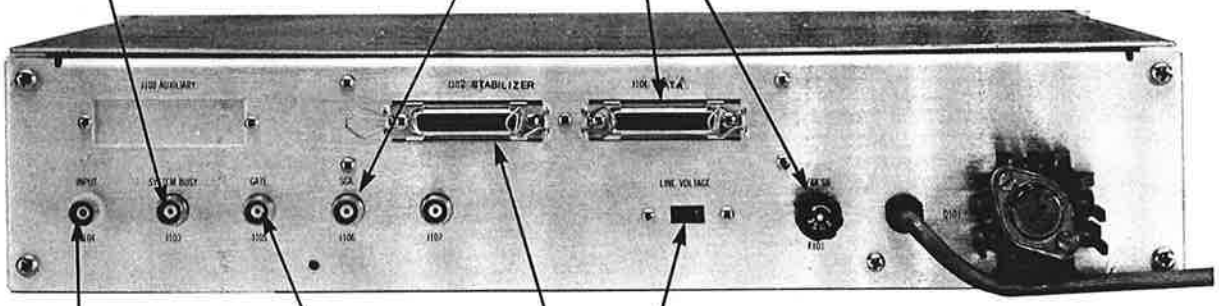


Figure 3-2
Rear Panel, Model 8070/8070A

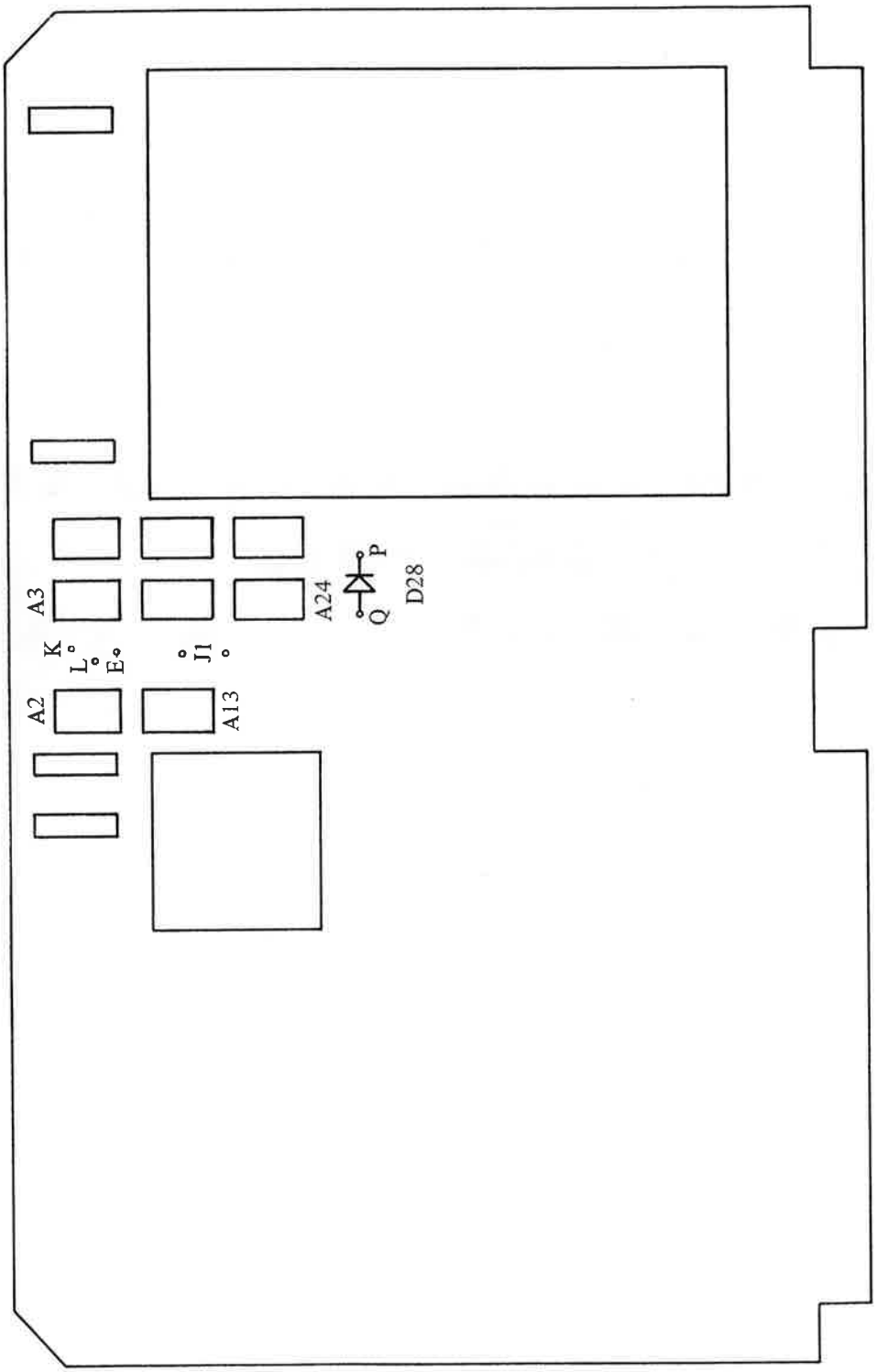


Fig. 3-3 Bd. #1 (ADC)

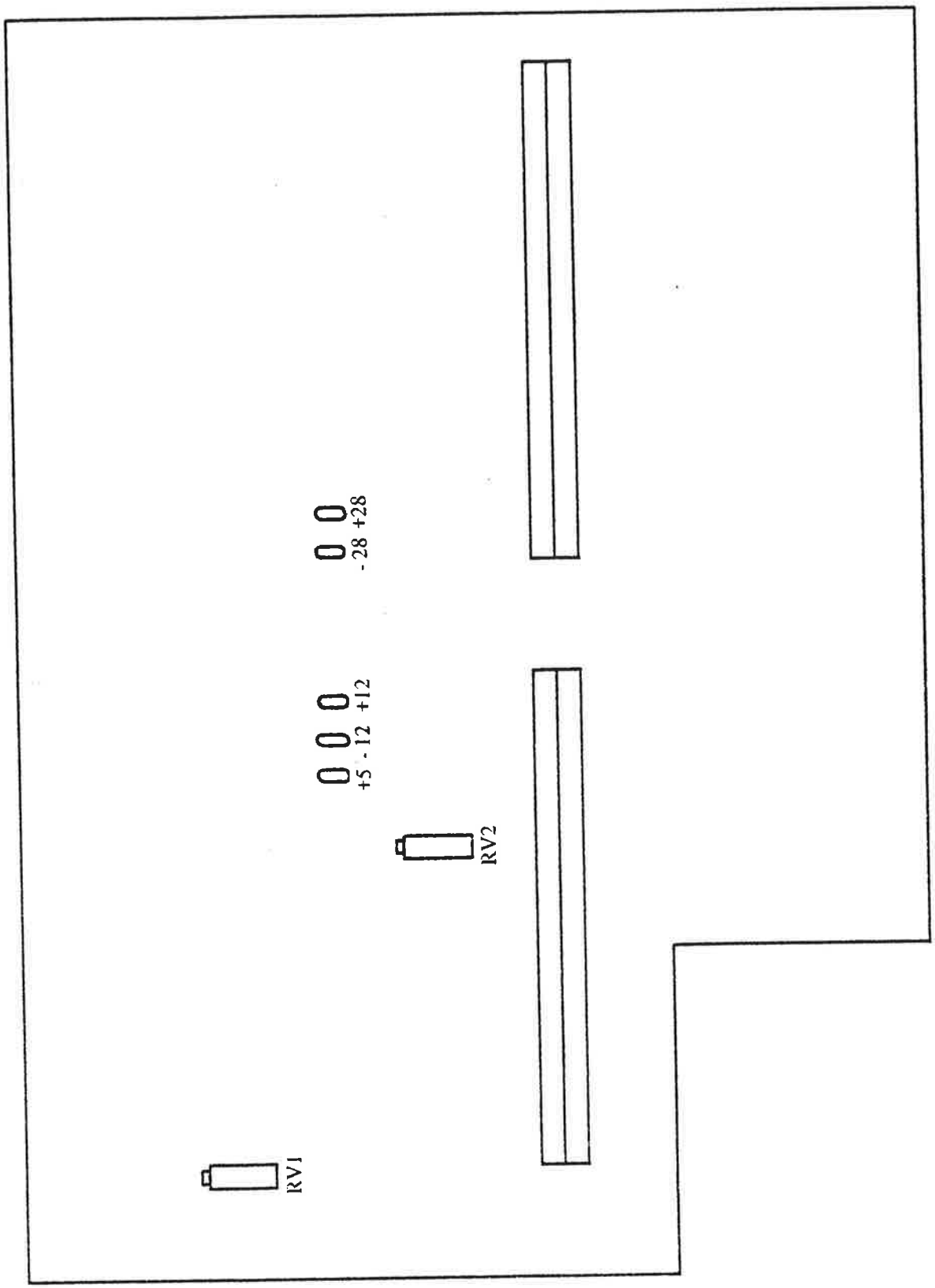


Fig. 3-4 Bd. #2 (ADC Interface)

SECTION 4
OPERATING INSTRUCTIONS

4.1 GENERAL

The purpose of this section is to familiarize the user with the operation of the Model 8070 Analog to Digital Converter and to check that the unit is functioning correctly. Since it is difficult to determine the exact system configuration in which the unit will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand.

4.2 INSTALLATION

The Model 8070 Analog to Digital Converter can be safely operated where the air temperature is between 0°C and +45°C (+120°F maximum). Perforations in the top and sides permit cooling air to circulate through the unit. When rack mounted along with other "heat generating" equipment, adequate clearance should be provided to allow for sufficient air flow through both the perforated top cover and sides of the unit. A rear panel switch is provided on the Model 8070 which should be positioned such that the marking of the voltage used is seen through the hole in the panel.

4.3 OPERATION

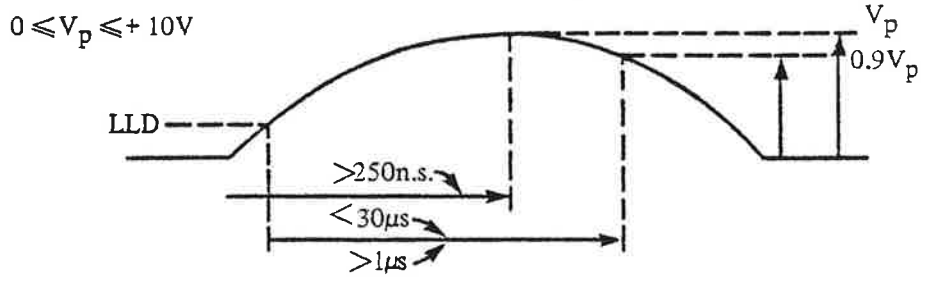
4.3.1 ADC GENERAL

The function of the ADC is to convert the input signal to a digital value proportional to its amplitude. The ADC does this by precisely charging a capacitor to the amplitude of the input and then discharging the storage cap at a constant rate. During the discharge time, a crystal controlled pulse train is counted in a register. When the ramp has returned to the baseline, the number in the register will represent the height of the input signal.

4.3.2 INPUT

If an oscilloscope is available, the ADC IN test point can be used during set-up. The amplifier gain feeding the input is adjusted to give an output of +10V. It will operate linearly to +11 volts, however. The pulse shape requirement of the ADC is quite broad, allowing pulses with rollover widths of up to 30 microseconds to be analyzed with no adjustments. The linear gate automatically ends when the input signal falls below 90% of the peak amplitude. Longer width pulses (for instance, from X-ray detectors, amplifiers) can be accepted by changing a capacitor, C49 (3000 pf), on the ADC board.

ADC PULSE INPUT REQUIREMENT



4.3.3 CONVERSION GAIN

The Conversion Gain controls the resolution of the ADC; i.e., the number of pieces into which the 10 volt input signal can be divided. On the upper ranges (1024 through 8192), the constant current controlling the storage cap discharge time is changed. On the two lower ranges, 256 and 512, the gain division is made digitally because changing the ramp rate over a range of greater than 8 to 1 will cause unnecessary non-linearity.

4.3.4 RANGE

The digital range (overflow) of the ADC should be set to match the memory group assigned to the ADC. For example, if an 8192 memory group were available, the ADC Range should be set at 8192 to utilize the full memory. If, however the memory group were only 4096 and the ADC Range was set to 8192, both halves of the ADC conversions would be summed in the available 4096 memory.

4.3.5 BASELINE

The Baseline controls of the ADC (Analog and Digital offset) vary the intercept of the ADC conversion function. Their effect is to slide the spectrum in the memory (left or right). See the Baseline figure for examples. The Analog Baseline is used as a fine adjustment when it is necessary to have a particular peak have its centroid at a predetermined channel address; A setting of ≈ 5.0 sets the ADC for zero energy in channel zero. The Digital Offset makes precise shifts of the spectrum. Because of noise and non-linearity problems associated with this general type of ADC, the lower 1% of the input range is not useable. With Digital Baseline, the zero can be suppressed, allowing the entire memory to be used.

Digital Baseline is advantageous when taking high resolution spectra in a small memory. For example, if a Ge(Li) detector is used with a 1024 channel memory for a gamma ray experiment, it would normally be run for the highest resolution to allow accurate separation and determination of peak positions; by using the Digital Offset, any part of the spectrum can be stored in memory groups as small as 256 channels.

The following calibration procedure is necessary when the Analog Baseline control is to have channel zero correspond with zero energy (a tag has been attached to this unit which gives the setting for the 1024 and 8192 Conversion Gain ranges):

1. Connect a Model 8210 Precision Pulse Generator or equivalent to the ADC IN connector.

2. Set Conversion Gain to the desired resolution. For 256 and 512, the Baseline should be set at 1024 gain.

3. Set Range to 8192.

4. Shut off all Digital Baseline switches.

5. Set all Binary switches on the pulser to the ON position and adjust its Coarse and Fine Amplitude controls for maximum conversion. Use LED lamps to determine max conversion.

6. For 1024 Gain the maximum conversion is Channel 1023; for 8192 it is Channel 8191. Set the most significant toggle switches on Pulser to OFF. Conversion should be in the equivalent channel: for example, on 8192 set toggles 1/2, 1/4, 1/8, 1/16, 1/32, and 1/64 to off and storage should be in channel 127. If not, adjust the ADC Analog Baseline Control. For optimum intercept calibration, the pulser should be stored at:

Gain		Channel	
	8192		127
	4096		63
	2048		31
	1024		15

7. Repeat steps 5 and 6 until no further adjustments are necessary to Pulser amplitude or Baseline controls.

8. Record Baseline setting for future use.

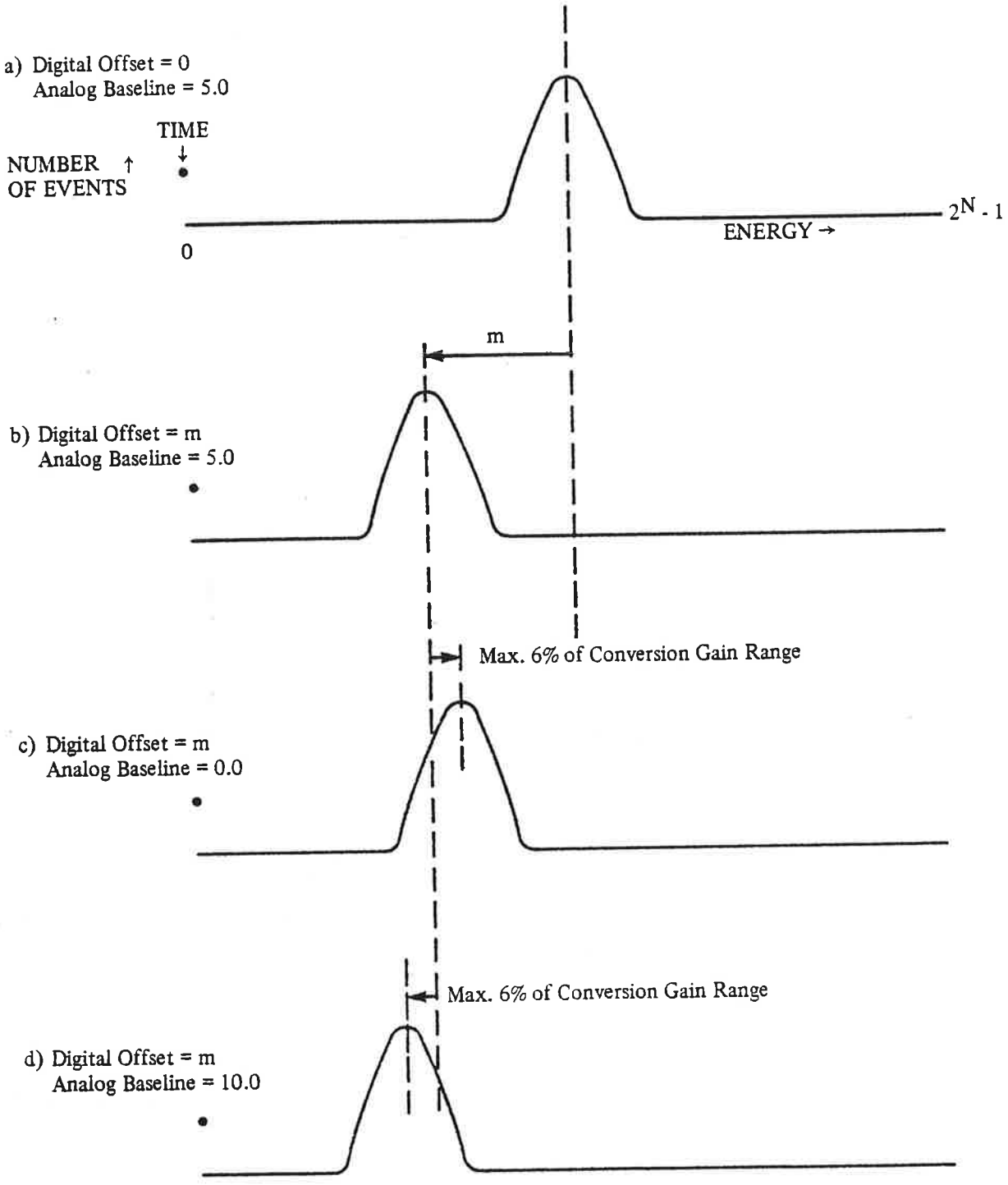


Figure 4-1 Baseline Variation - Examples of Effect on Spectrum

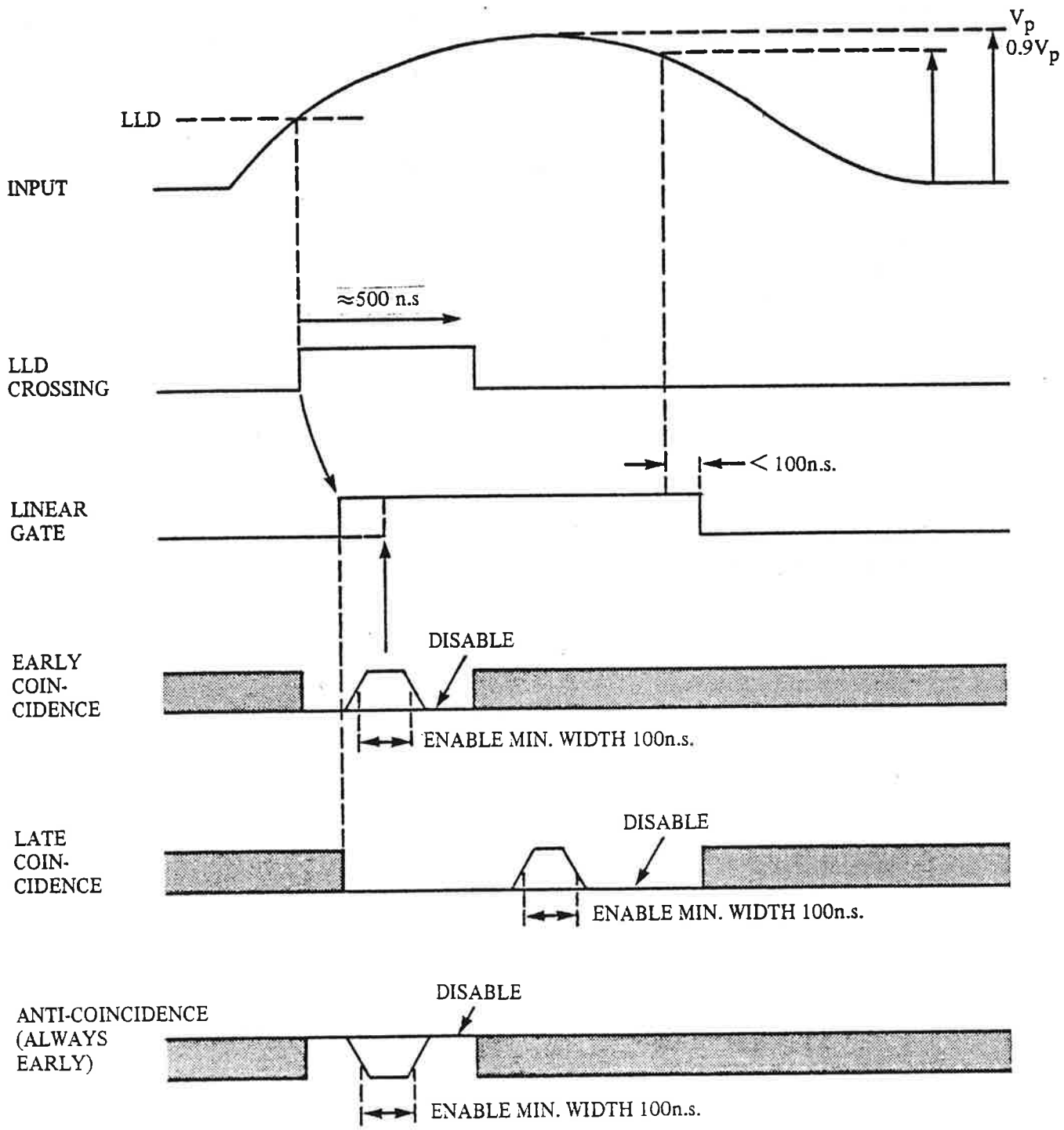


Figure 4-2. Coincidence Timing

4.3.6 COINCIDENCE

Coincidence functions to gate the processing of the linear input signal. The ADC has provision for Early or Late Coincidence. The ADC is shipped with * the internal jumper set for Late Coincidence: this requires a positive logic pulse of at least 100 nanosecond width during the linear gate time to enable conversion: if the Coincidence Gate Input is low during this entire time the pulse stored on the stretcher capacitor will be reset quickly and the memory will not be incremented. If the jumper is moved to the Early Coincidence position the gating is done at the time that the linear signal crosses the Lower Level setting: a low during this time will prevent the linear gate from opening and charging the storage cap. Early coincidence is preferable when a high count rate is being gated because of the appreciable dead time introduced in Late. However, Late Coincidence gating is easier to do since a delay amplifier is not needed. The added cost and degradation of the linear signal by the delay amplifier must be considered. In the Anti-Coincidence position, the logic sense of the Early Coincidence signal is inverted; that is, a Low will enable and High will disable. Anti-Coincidence is not used with Late; in Anti-Coincidence, the logic is always set for Early, regardless of jumper position.

4.3.7 SAMPLE VOLTAGE ANALYSIS

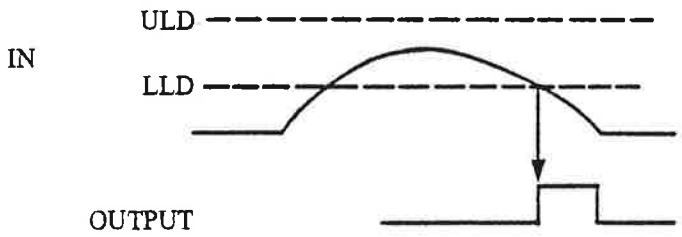
Analog voltages (DC or slowly changing AC voltages) can be sampled by the ADC. The result will be an amplitude distribution curve. The input signal must be a 0 to +10 volt signal. The SCA window is used to allow conversion of signals which are between the LLD and ULD settings. The Gate Input supplies the sampling signal; it must be at least 1/2 microseconds and less than 30 microseconds wide to allow enough sampling time for the ADC storage capacitor. At the end of the coincidence input, the voltage on the capacitor is converted to its digital value.

It is necessary that the program jumpers * on the ADC be set for Early Coincidence and for Sample.

4.3.8 SCA

The SCA sets a window on the ADC input signal. The lower limit is set by the LLD, while the ULD sets the upper level threshold. Both are independently adjustable from 0 to 110% of range. If a pulse falls within this window, a logic pulse is generated at a rear panel connector. The LLD must be set above the baseline of the input signal.

SCA TIMING



The SCA operates independently of the ADC processing. Although the ADC input pulse must meet the window requirements of the SCA, the SCA can continue to examine inputs while the ADC section is busy converting a previous input. Thus, SCA outputs can be compared to conversions to determine how many pulses are being rejected.

*See Section 3.3.1

4.3.9 ADC CONVERSION INDICATORS

Visual feedback of ADC operation is provided by the 13 data and two status LED lamps. Input activity can be estimated over a visual data range and the operator may be alerted to change set-up parameters based on numerous or constant overflow/invalid indications. Since the Model 8070 has a built-in automatic release feature, a memory storage unit is not needed for check-out or calibration. The ADC will continually convert inputs and display its data at the automatic release frequency (≈ 10msec.)

4.3.10 INTERFACING

Data connector (J101) supplies data and necessary control signals to interface to any Canberra or Geoscience memory storage unit. A block diagram of the output logic is provided in Appendix B.

The 13 data lines originate from open collector TTL drivers gated by the ENABLE DATA input. Data is active low (logic 1) and pulled-up to +5V through individual 4.7K resistors for logic 0. This greatly simplifies the hardware necessary for interfacing to most memories. For long data paths, additional pull-up resistors should terminate the data lines. The DATA READY signals that the data is available; an automatic release feature will reset the ADC if the DATA READY is not acknowledged within approximately 10ms. The ADC acknowledge signal is the DATA ACCEPT input pulse which should be at least 0.5μsec wide. A DEAD TIME signal is brought out to enable live timing circuitry to control storage periods. The ENABLE CONVERTER input can be used to gate the ADC on or off, however, any conversion in progress will be allowed to finish.

The OVERFLOW and INVALID signals are useful when multiparameter experiments are run. The OVERFLOW signal is given for all inputs which start a conversion but are beyond the digital range or for inputs which are not converted because they exceed the upper level discriminator setting. When the Overflow pulse (~ 2μsec) is given, the INVALID flag is set; INVALID may also be set if with a coincidence input the linear signal is not large enough to cause a conversion. The INVALID flag is reset by a DATA ACCEPT pulse. It does not contribute to the dead time.

The INHIBIT ADD ONE and INTENSIFY signals are from the stabilizer. The INHIBIT is used to prevent storage of a reference peak from a pulser. The INTENSIFY is used to aid in determining proper settings of the peak and window controls of the stabilizer.

Stabilizer connector (J102) provides conversion data and control signals to a Model 8200 Digital Stabilizer. Analog correction signals from the Stabilizer can vary the ADC gain or zero by ± 1% of full scale. Two Stabilizers can be made to track both gain and zero for complete drift free analysis.

APPENDIX A
CONNECTOR SIGNAL LISTS

A.1 J101 DATA

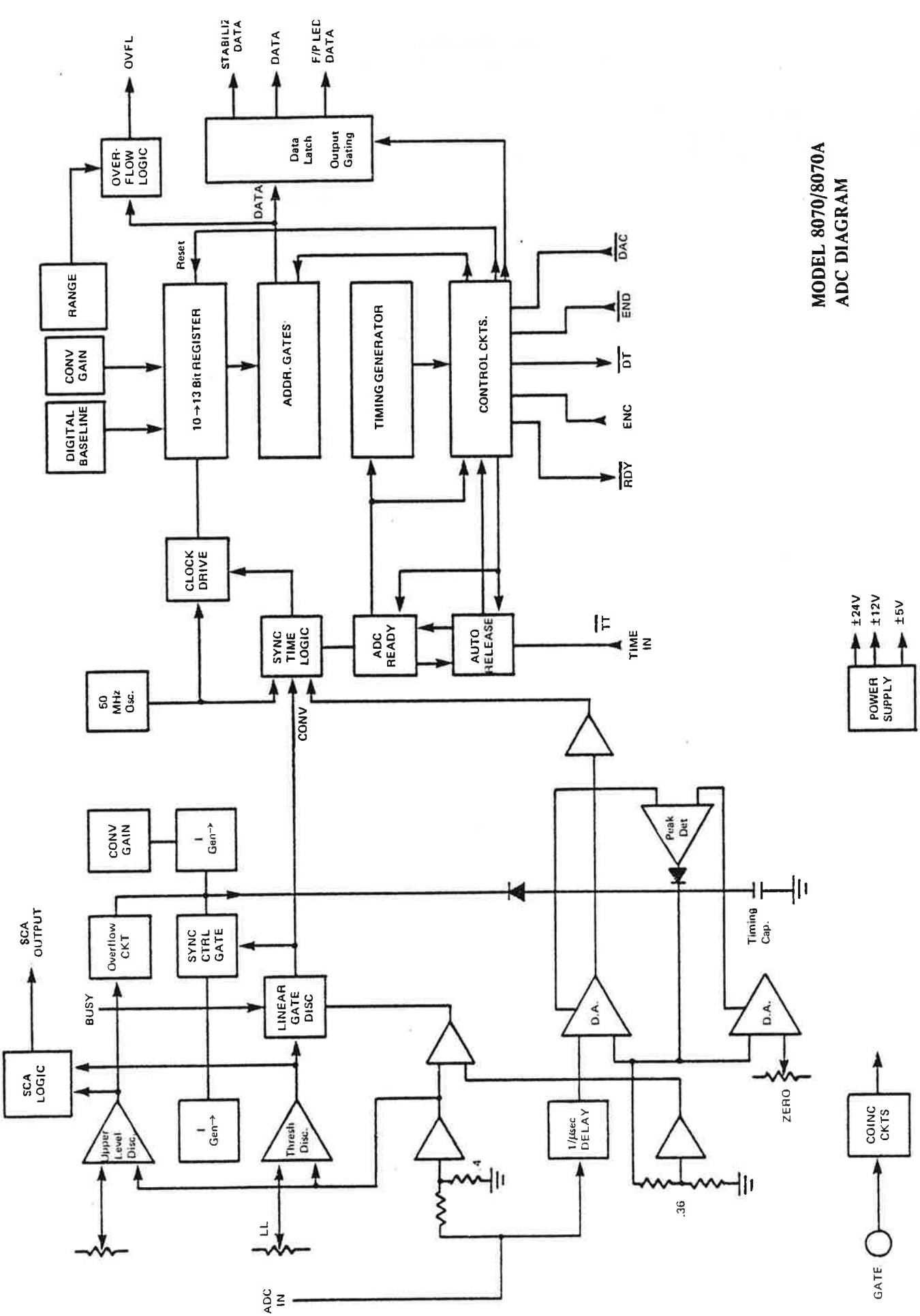
Pin	Mneomonic	Signal Description
1	$\overline{20}$	Gated Binary Address Data Logic 1 = 0V Logic 0 = 5V - Open Collector TTL output with 4.7K pull-up resistors to +5.
2	$\overline{21}$	
3	$\overline{22}$	
4	$\overline{23}$	
5	$\overline{24}$	
6	$\overline{25}$	
7	$\overline{26}$	
8	$\overline{27}$	
9	$\overline{28}$	
10	$\overline{29}$	
11	$\overline{210}$	
12	$\overline{211}$	
13	$\overline{212}$	
14	$\overline{\text{DRDY}}$	Data Ready - signals external memory storage unit that a conversion is complete (Active LOW)
15	N/C	No connection
16	$\overline{\text{INHAD}}$	Inhibit Add - signal originating from a Digital Stabilizer and passed directly to the memory storage unit. The INHAD signal is used to prevent storage of a reference peak from a pulser. (Active LOW)
17	$\overline{\text{DAC}}$	Data Accept - feedback signal from the memory storage unit that acknowledges data acceptance. This pulse resets the ADC and clears the Invalid flag if set. (Active LOW)
18	ENC	Enable Converter - used to gate the ADC on or off. Pulses in progress prior to termination of ENC will be allowed to continue and finish the output sequence but further pulses will be ignored. (Active HIGH)
19	$\overline{\text{OVFL}}$	Overflow - a 2μsec pulse given for all inputs which start a conversion but are beyond the digital range or for inputs which are not converted because they exceed the ULD setting. (Active LOW)
20	$\overline{\text{INV}}$	Invalid - set by OVFL or for when the converted value is less than the Digital Offset. Invalid may also be set if with a coincidence input the linear signal is not large enough to cause conversion. The INV signal is reset by DAC. (Active LOW)
21	DT	Dead Time - signal used to enable live time circuitry to control storage periods (Active HIGH)
22	$\overline{\text{END}}$	Enable Data - used to gate the 13 bit data onto the output lines. (Active LOW)

23	$\overline{\text{INT}}$	Intensify - signal originating from a Digital Stabilizer and passed directly to the memory storage unit. The INT signal is used to aid in determining proper settings of the peak and window controls of the stabilizer. (Active LOW)
24	GND	Ground
25	N/C	No Connection

A.2 J102 STABILIZER

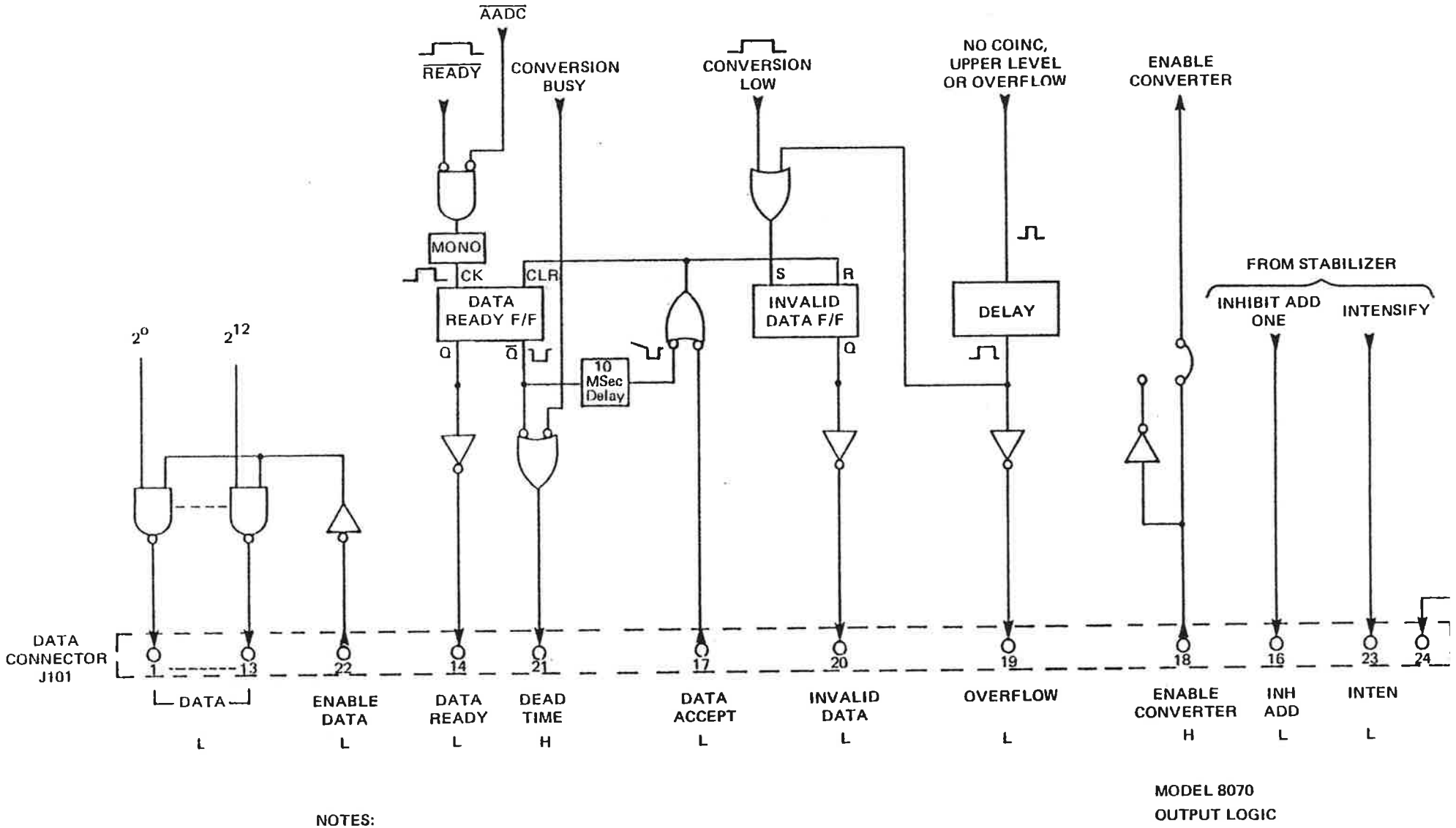
Pin	Mnemonic	Signal Description
1	$\overline{20}$	
2	$\overline{21}$	
3	$\overline{22}$	
4	$\overline{23}$	
5	$\overline{24}$	Binary Address Data
6	$\overline{25}$	Logic 1 = 0V
7	$\overline{26}$	Logic 0 = 4V
8	$\overline{27}$	
9	$\overline{28}$	
10	$\overline{29}$	
11	$\overline{210}$	
12	$\overline{211}$	
13	$\overline{212}$	
14	N/C	No Connection
15	N/C	No Connection
16	$\overline{\text{INHAD}}$	Inhibit Add - signal from the Digital Stabilizer and routed to the memory stostorage unit to prevent storage of a reference peak from a pulser. (Active LOW)
17	N/C	No Connection
18	N/C	No Connection
19	$\overline{\text{INT}}$	Intensify - signal from the Digital Stabilizer and routed to the memory storage unit to aid in determining proper settings of the peak and window controls of the stabilizer. (Active LOW)
20	GS	Gain Correction - analog voltage from the stabilizer used to correct gain drifts (input impedance ~ 250K; ± 5V in yields a gain change of ~ ± 1% of full scale)
21	ZS	Zero Correction - analog voltage from the stabilizer used to correct zero drifts (input impedance ~ 1K; ± 2.5V in yields a zero change of ~ ± 1% of full scale)
22	N/C	No Connection
23	$\overline{\text{SRDY}}$	Stabilizer Trigger - approximately 2μsec. trigger pulse to indicate a conversion is complete.
24	GND	Ground
25	N/C	No Connection

APPENDIX B
DIAGRAMS AND SCHEMATICS



MODEL 8070/8070A
ADC DIAGRAM

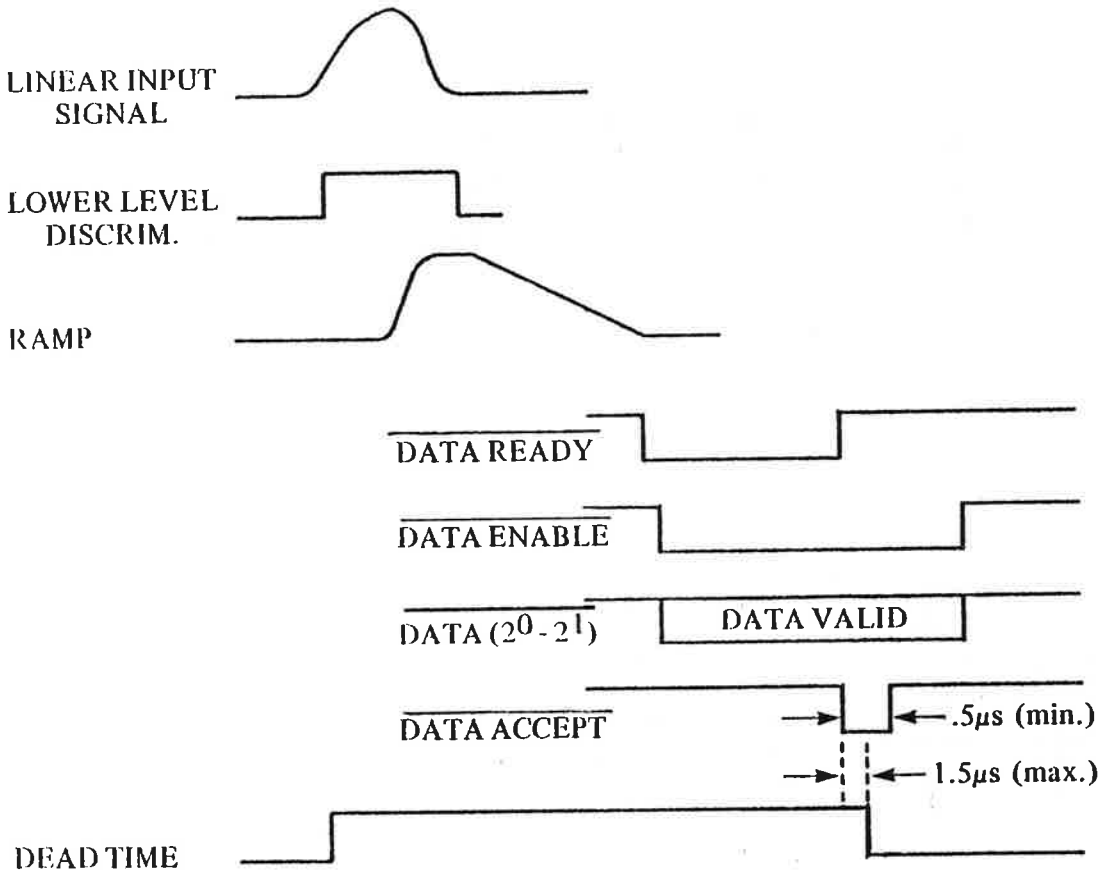
Figure 1



NOTES:
1. H INDICATES ACTIVE STATE HIGH
2. L INDICATES ACTIVE STATE LOW

MODEL 8070
OUTPUT LOGIC

Figure B-2



If $\overline{\text{DATA ENABLE}}$ is held low or left disconnected the Data Lines will output the last valid conversion.

Data is available immediately following the falling edge of $\overline{\text{DATA READY}}$.

Model 8070/8070A
Output Timing

ure

WARRANTY

Canberra-Manufactured Equipment

Equipment manufactured by Canberra Industries, Inc. is warranted against defects in materials and workmanship for a period of twelve months from date of shipment, provided that the equipment has been used in a proper manner as detailed in the instruction manuals. During the warranty period repairs or replacement will be made at Canberra's option, but the transportation cost to and from Canberra is the responsibility of the Customer. For defects discovered upon initial operation, shipping expense to Canberra is to be paid by the customer; shipping expense to return the repaired equipment will be paid by Canberra.

The customer must obtain shipping instructions, including an *Authorized Return Number* (ARN), before returning any equipment to the Canberra factory. Compliance with this provision by the customer shall be a condition of this warranty. In giving shipping instructions, Canberra shall not, therefore, assume any liability in connection with the shipment. If, upon receipt of the equipment, Canberra determines that such equipment is not defective within the terms of this warranty, the customer shall pay to Canberra upon invoice, the cost of all transportation and cost of repairs at the then prevailing Canberra repair rate.

This warranty shall not apply to equipment that has been modified or serviced by other than Canberra service personnel, or to failures caused by defective equipment not supplied by Canberra.

This warranty applies only to equipment manufactured by Canberra. On other equipment supplied by Canberra, the full warranty, and only that warranty offered by the original manufacturer, will be passed on to the customer.

WARRANTY ON EQUIPMENT NOT MANUFACTURED BY CANBERRA

Canberra's basic one-year warranty applies only to equipment manufactured by Canberra. Although Canberra may frequently supply, as part of systems, equipment manufactured by other companies, the only warranty that shall apply to such non-Canberra equipment is that warranty offered by the original manufacturer.

Canberra will, upon request, state what warranties are offered by the original manufacturers of such items as computers, teletype machines, printers, plotters, and other non-Canberra equipment which may be supplied as part of a Canberra system. In no case, however, will Canberra assume any liability for such equipment other than to pass on to its customer whatever warranty is supplied by the original manufacturer.

WARRANTY ON SOFTWARE

Canberra will warrant system operation with *Canberra Laboratory Automated Software Systems* (CLASS) only. If the customer decides to use software other than CLASS, Canberra assumes *no* responsibility. Engineering assistance, however, for non-CLASS software is available to the user and should be contracted separately if desired.

ON-SITE WARRANTY OPTION

The basic Canberra warranty applies only to equipment manufactured by Canberra which is *returned to the factory*. If equipment must be repaired at the customer's site, the actual repair labor and parts will be provided at no charge during the warranty period. However, travel expenses to and from the customer's site, and living expenses while on site, shall be paid by the customer unless an on-site warranty option has been purchased. This option may only be purchased prior to shipment of the equipment to the customer.

The on-site warranty option provides for free on-site warranty work (Canberra pays all travel and living expenses) within the first 60 days after delivery of equipment to the customer. If installation is ordered from Canberra, the 60 day period commences upon completion of the initial installation. After the 60 day period, labor and materials used on site will still be covered by the basic warranty, but the customer shall pay for all travel and living expenses incurred for any on-site service.

The on-site warranty option is available only within the contiguous forty-eight (48) United States and Canada.

After the 60 days on-site warranty period, or after initial installation of the equipment, a maintenance contract may be purchased. This is to be contracted through Canberra's Customer Service Department. Contact the factory for details concerning warranty options and maintenance contracts.

INSTALLATION

Installation of equipment purchased from Canberra shall be the sole responsibility of the customer unless it is specifically contracted for at the prevailing Canberra field service rates. To insure timely installation after receipt of equipment, it is recommended that installation be contracted for at the time the equipment is ordered.

REPAIRS

Any Canberra-manufactured instrument no longer in its warranty period may be returned, freight prepaid, to our factory for repair and realignment. When returning instruments for repair, contact the factory for shipping instructions and an *Authorized Return Number* (ARN).

All correspondence concerning repairs should include Model Number and a description of the problem observed.

Once repaired, all equipment passes through our normal pre-shipment checkout procedure, and will meet or surpass its original specifications when returned. Return shipping expense on out-of-warranty repairs will be charged to the customer.

For instruments out of warranty, the customer must supply a purchase order number for the repair before the item will be returned.

SHIPPING DAMAGE

Shipments should be carefully examined when received for evidence of damage caused by shipping. If damage is found, immediately notify Canberra and the carrier making delivery, as the carrier is normally responsible for damage caused in shipment. Carefully preserve all documentation to establish your claim. Canberra will provide all possible assistance in damage claims.